

MOSFET - Power, Dual N-Channel

60 V, 38 mΩ, 18 A

NVLJWD040N06CL

Features

- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	$T_C = 25^\circ\text{C}$	I_D	A
		18	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	$T_C = 100^\circ\text{C}$	13	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	$T_A = 25^\circ\text{C}$	P_D	W
		24	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	$T_A = 100^\circ\text{C}$	12	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	A
		54	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C
Source Current (Body Diode)	I_S	20	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 0.9\text{ A}$)	E_{AS}	27	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	°C

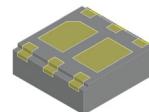
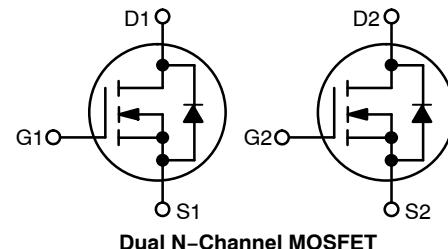
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	6.3	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	69	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	38 mΩ @ 10 V	18 A
	50 mΩ @ 4.5 V	



MARKING DIAGRAM



WDFNW6 (2.2x2.3)
CASE 515AS

040N = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVLJWD040N06CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				25		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25 °C			10	μA
			T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 13 μA		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.4		mV/°C
Drain-to-Source On Resistance	R _{DSON}	V _{GS} = 10 V	I _D = 5 A		31	38	mΩ
		V _{GS} = 4.5 V	I _D = 5 A		40	50	
Forward Transconductance	g _F	V _{DS} = 10 V, I _D = 5 A			14		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		340		pF
Output Capacitance	C _{OSS}			145		
Reverse Transfer Capacitance	C _{rss}			3		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 5 A		3		nC
Total Gate Charge	Q _{G(TOT)}			6		
Threshold Gate Charge	Q _{G(TH)}			0.7		
Gate-to-Source Charge	Q _{GS}			1.3		
Gate-to-Drain Charge	Q _{GD}			0.6		
Plateau Voltage	V _{GP}			3		
						V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 5 A, R _G = 6 Ω		4.8		ns
Rise Time	t _r			1.4		
Turn-Off Delay Time	t _{d(OFF)}			12.1		
Fall Time	t _f			1.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5 A	T _J = 25°C		0.88	1.2	V
			T _J = 125°C		0.77		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 5 A			20		ns
Charge Time	t _a				11		
Discharge Time	t _b				9		
Reverse Recovery Charge	Q _{RR}				10		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

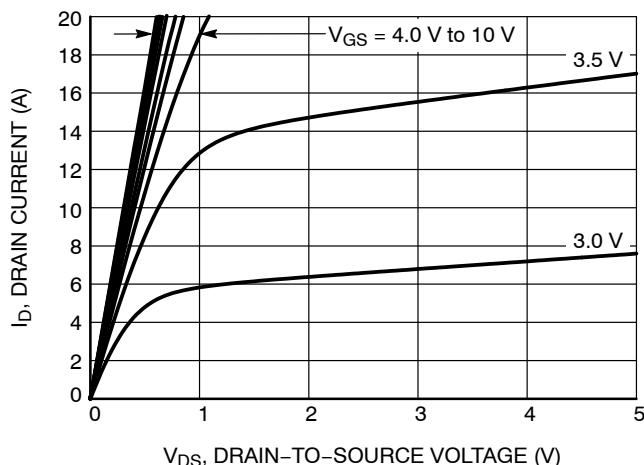


Figure 1. On-Region Characteristics

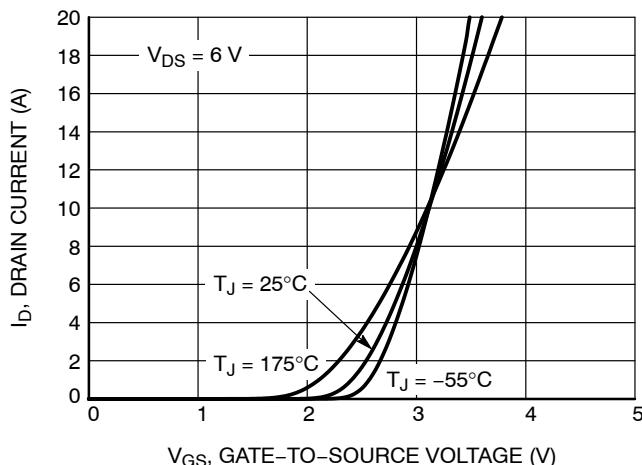


Figure 2. Transfer Characteristics

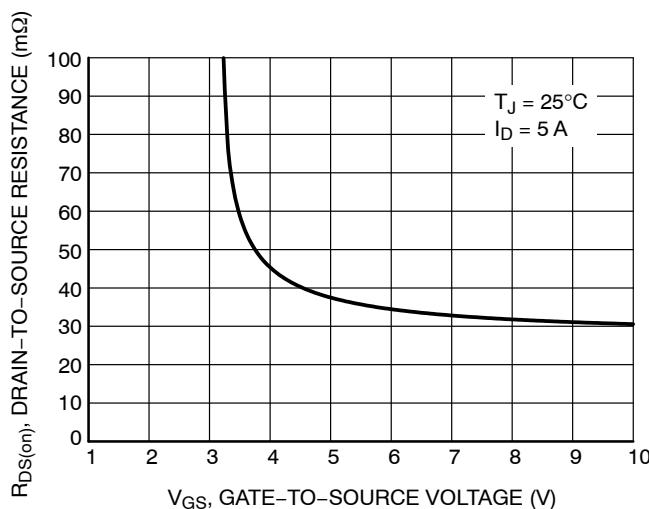


Figure 3. On-Resistance vs. Gate-to-Source Voltage

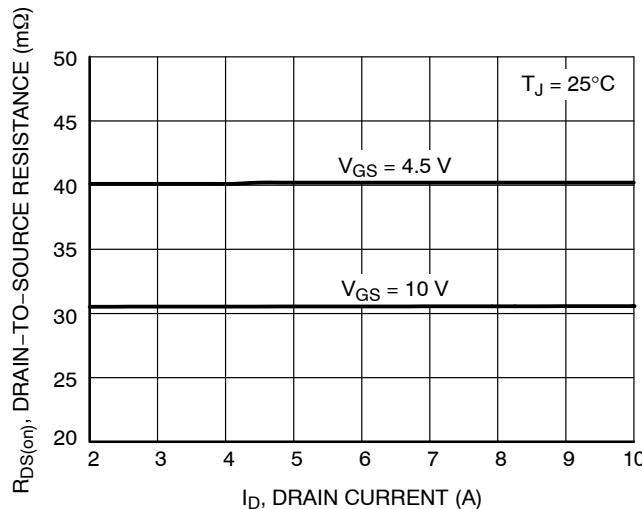


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

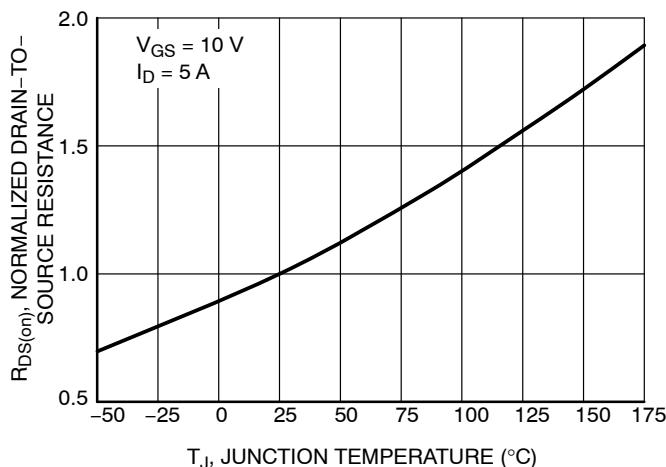


Figure 5. On-Resistance Variation with Temperature

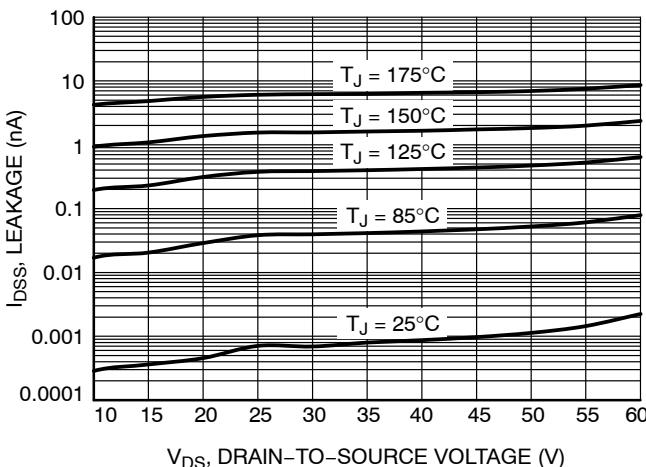


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

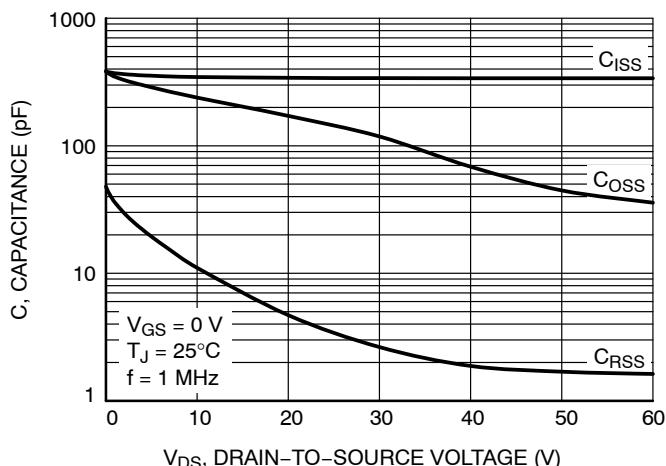


Figure 7. Capacitance Variation

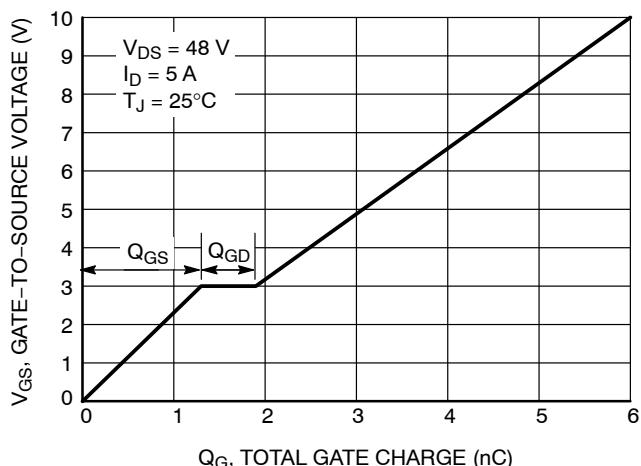


Figure 8. Gate-to-Source vs. Total Charge

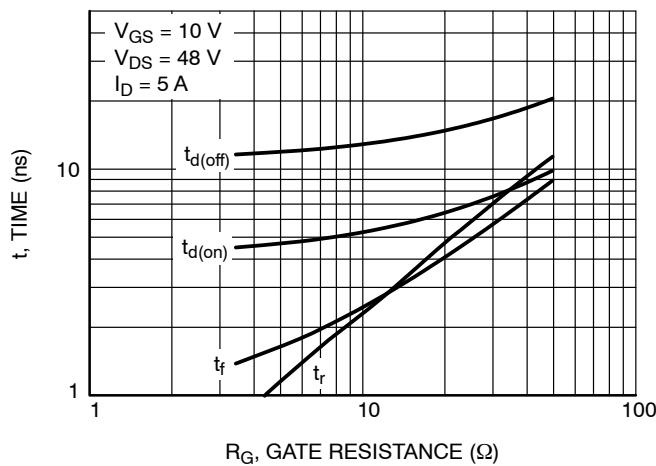


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

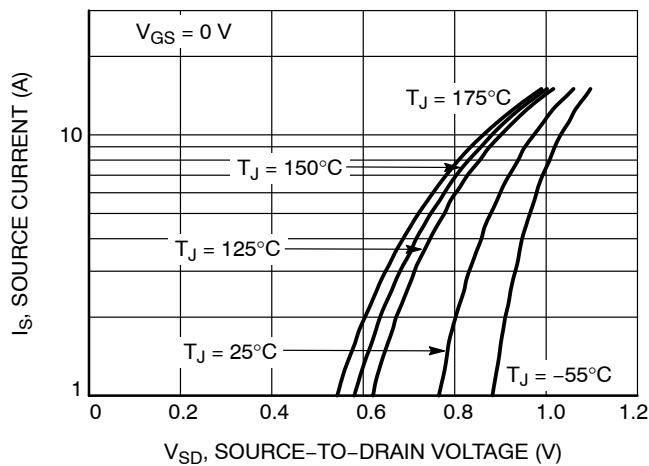


Figure 10. Diode Forward Voltage vs. Current

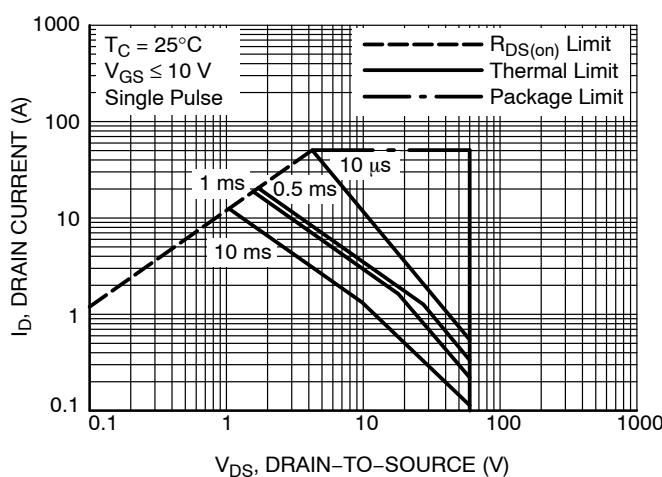
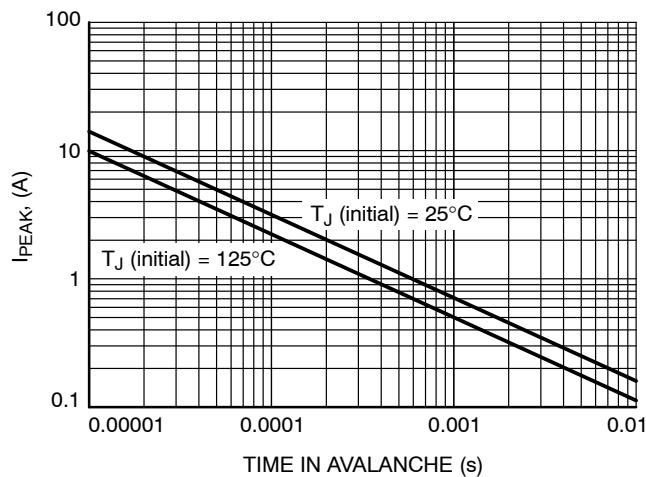


Figure 11. Safe Operating Area

Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

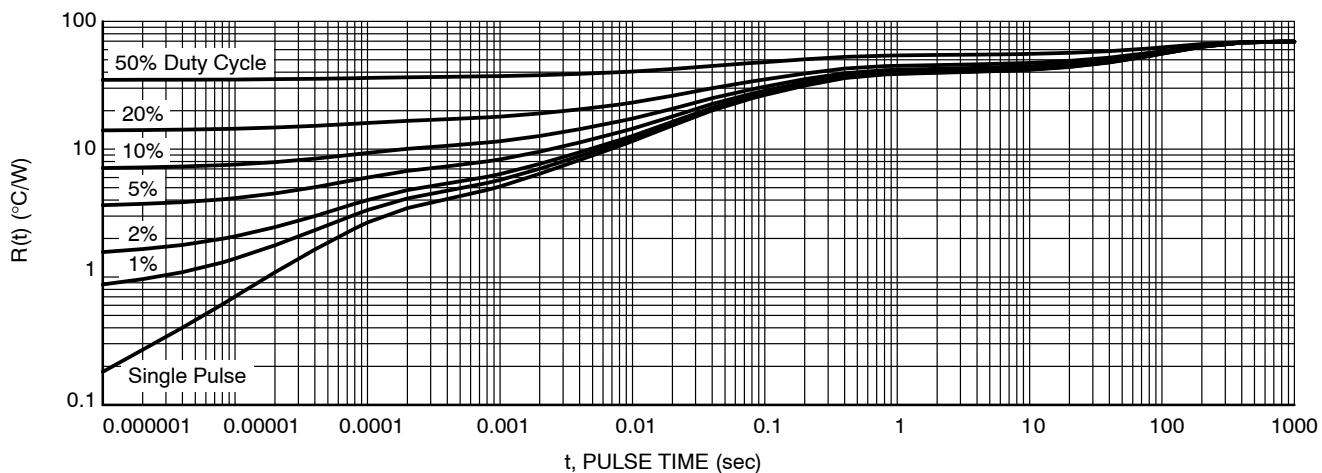


Figure 13. Transient Thermal Response Curve

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVLJWD040N06CLTWG	040N	WDFNW6 (Pb-Free, Wettable Flanks)	3000 / Tape & Reel

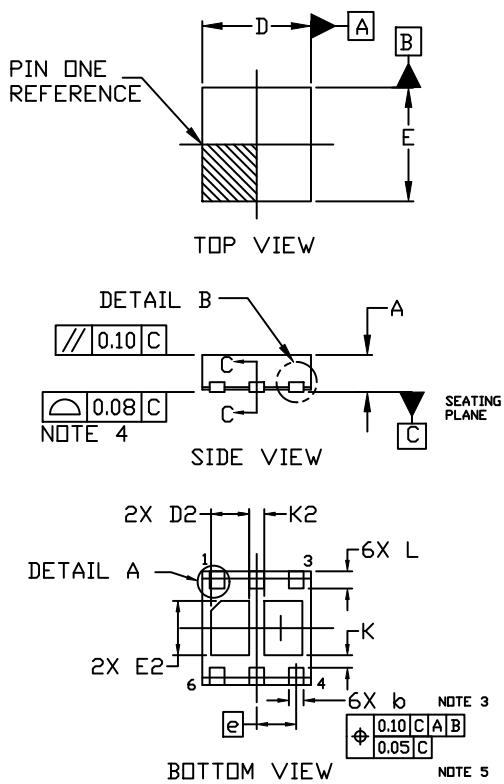
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WDFNW6 2.2x2.3, 0.8P

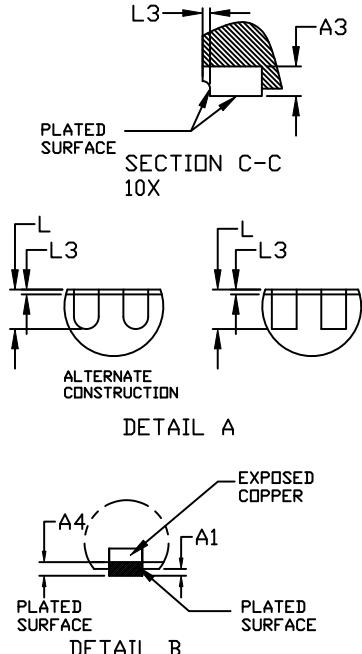
CASE 515AS

ISSUE O

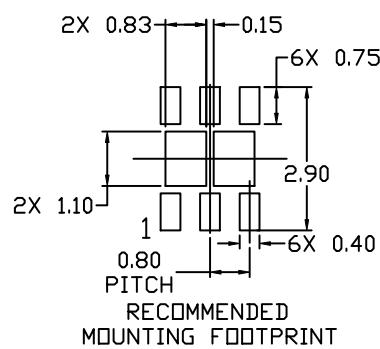


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3 0.20 REF			
A4	0.10	---	---
b	0.25	0.30	0.35
D	2.10	2.20	2.30
D2	0.72	0.77	0.82
E	2.20	2.30	2.40
E2	1.05	1.10	1.15
e	0.80 BSC		
K	0.25 REF		
K2	0.30 REF		
L	0.30	0.35	0.40
L3	---	---	0.09



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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