

3-Level NPC Inverter Module

NXH450N65L4Q2F2S1G

The NXH450N65L4Q2F2S1G is a power module containing a I-type neutral point clamped three-level inverter. The integrated field stop trench IGBTs and FRDs provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Neutral Point Clamped Three-Level Inverter Module
- 650 V Field Stop 4 IGBTs
- Low Inductive Layout
- Solderable Pins
- Thermistor
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Solar Inverters
- Uninterruptable Power Supplies Systems

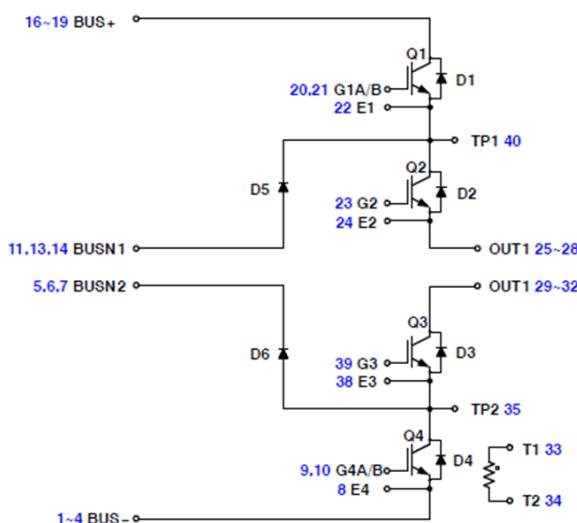
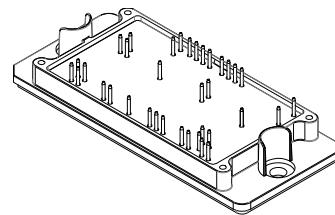
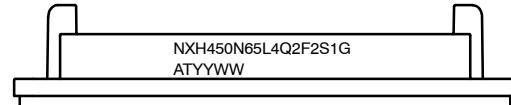


Figure 1. Schematic Diagram



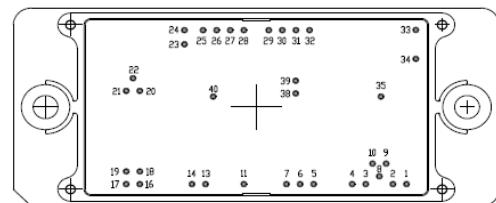
PIM40, 107.2x47
CASE 180BE

MARKING DIAGRAM



NXH450N65L4Q2F2S1G = Specific Device Code
G = Pb-Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

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MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
OUTER IGBT (Q1–1, Q1–2, Q4–1, Q4–2)			
V_{CES}	Collector–Emitter Voltage	650	V
V_{GE}	Gate–Emitter Voltage Positive Transient Gate–Emitter Voltage ($t_{pulse} = 5$ s, $D < 0.10$)	± 20 30	V
I_C	Continuous Collector Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	167	A
I_{Cpulse}	Pulsed Collector Current ($T_J = 175^\circ\text{C}$)	501	A
P_{tot}	Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	365	W
T_{JMAX}	Maximum Operating Junction Temperature	175	$^\circ\text{C}$

INNER IGBT (Q2, Q3)

V_{CES}	Collector–Emitter Voltage	650	V
V_{GE}	Gate–Emitter Voltage Positive Transient Gate–Emitter Voltage ($t_{pulse} = 5$ s, $D < 0.10$)	± 20 30	V
I_C	Continuous Collector Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	280	A
I_{Cpulse}	Pulsed Collector Current ($T_J = 175^\circ\text{C}$)	840	A
P_{tot}	Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	633	W
T_{JMAX}	Maximum Operating Junction Temperature	175	$^\circ\text{C}$

NEUTRAL POINT DIODE (D5, D6)

V_{RRM}	Peak Repetitive Reverse Voltage	650	V
I_F	Continuous Forward Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	211	A
I_{FRM}	Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$)	633	A
P_{tot}	Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	500	W
T_{JMAX}	Maximum Operating Junction Temperature	175	$^\circ\text{C}$

INVERSE DIODES (D1, D2, D3, D4)

V_{RRM}	Peak Repetitive Reverse Voltage	650	V
I_F	Continuous Forward Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	93	A
I_{FRM}	Repetitive Peak Forward Current ($t_p = 1$ ms)	279	A
P_{tot}	Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	231	W
T_{JMAX}	Maximum Operating Junction Temperature	175	$^\circ\text{C}$

THERMAL PROPERTIES

T_{stg}	Storage Temperature Range	-40 to 150	$^\circ\text{C}$
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INSULATION PROPERTIES

V_{is}	Isolation Test Voltage, $t = 1$ s, 50 Hz	4000	V_{rms}
	Creepage Distance	12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
T_J	Module Operating Junction Temperature	-40	T_{JMAX}	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OUTER IGBT (Q1-1, Q1-2, Q4-1, Q4-2)						
I_{CES}	Collector-Emitter Cutoff Current	$V_{GE} = 0 \text{ V}$, $V_{CE} = 650 \text{ V}$	—	—	300	μA
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	$V_{GE} = 15 \text{ V}$, $I_C = 225 \text{ A}$, $T_J = 25^\circ\text{C}$	—	1.49	2.2	V
		$V_{GE} = 15 \text{ V}$, $I_C = 225 \text{ A}$, $T_J = 175^\circ\text{C}$	—	1.68	—	
$V_{GE(\text{TH})}$	Gate-Emitter Threshold Voltage	$V_{GE} = V_{CE}$, $I_C = 2.75 \text{ mA}$	3.1	4.1	5.2	V
I_{GES}	Gate Leakage Current	$V_{GE} = 20 \text{ V}$, $V_{CE} = 0 \text{ V}$	—	—	600	nA
$t_{d(\text{on})}$	Turn-On Delay Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 10 \Omega$	—	162	—	ns
t_r	Rise Time		—	49	—	
$t_{d(\text{off})}$	Turn-off Delay Time		—	642	—	
t_f	Fall Time		—	52	—	
E_{on}	Turn-On Switching Loss per Pulse		—	4.4	—	mJ
E_{off}	Turn Off Switching Loss per Pulse		—	4.8	—	
$t_{d(\text{on})}$	Turn-On Delay Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 10 \Omega$	—	150	—	ns
t_r	Rise Time		—	57	—	
$t_{d(\text{off})}$	Turn-off Delay Time		—	692	—	
t_f	Fall Time		—	70	—	
E_{on}	Turn-on Switching Loss per Pulse		—	6.2	—	mJ
E_{off}	Turn Off Switching Loss per Pulse		—	5.1	—	
C_{ies}	Input Capacitance	$V_{CE} = 20 \text{ V}$, $V_{GE} = 0 \text{ V}$, $f = 10 \text{ kHz}$	—	14630	—	pF
C_{oes}	Output Capacitance		—	230	—	
C_{res}	Reverse Transfer Capacitance		—	64	—	
Q_g	Total Gate Charge	$V_{CE} = 480 \text{ V}$, $I_C = 225 \text{ A}$, $V_{GE} = \pm 15 \text{ V}$	—	452	—	nC
R_{thJH}	Thermal Resistance – Chip-to-Heatsink	Thermal grease, Thickness = 2 Mil $\pm 2\%$, $A = 2.8 \text{ W/mK}$	—	0.45	—	$^\circ\text{C/W}$
R_{thJC}	Thermal Resistance – Chip-to-Case		—	0.26	—	$^\circ\text{C/W}$

NEUTRAL POINT DIODE (D5, D6)

V_F	Diode Forward Voltage	$I_F = 250 \text{ A}$, $T_J = 25^\circ\text{C}$	—	2.45	3.1	V
		$I_F = 250 \text{ A}$, $T_J = 175^\circ\text{C}$	—	1.87	—	
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 10 \Omega$	—	37	—	ns
Q_{rr}	Reverse Recovery Charge		—	1.6	—	
I_{RRM}	Peak Reverse Recovery Current		—	69	—	
di/dt	Peak Rate of Fall of Recovery Current		—	3225	—	
E_{rr}	Reverse Recovery Energy		—	0.31	—	
t_{rr}	Reverse Recovery Time		—	71	—	
Q_{rr}	Reverse Recovery Charge	$T_J = 125^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 10 \Omega$	—	6	—	$^\circ\text{C}$
I_{RRM}	Peak Reverse Recovery Current		—	138	—	
di/dt	Peak Rate of Fall of Recovery Current		—	2987	—	
E_{rr}	Reverse Recovery Energy		—	1.28	—	
R_{thJH}	Thermal Resistance – Chip-to-Heatsink		—	0.32	—	$^\circ\text{C/W}$
R_{thJC}	Thermal Resistance – Chip-to-Case		—	0.19	—	$^\circ\text{C/W}$

INNER IGBT (Q2, Q3)

I_{CES}	Collector-Emitter Cutoff Current	$V_{GE} = 0 \text{ V}$, $V_{CE} = 650 \text{ V}$	—	—	300	μA
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	$V_{GE} = 15 \text{ V}$, $I_C = 375 \text{ A}$, $T_J = 25^\circ\text{C}$	—	1.49	2.2	V
		$V_{GE} = 15 \text{ V}$, $I_C = 375 \text{ A}$, $T_J = 175^\circ\text{C}$	—	1.73	—	
$V_{GE(\text{TH})}$	Gate-Emitter Threshold Voltage	$V_{GE} = V_{CE}$, $I_C = 3.75 \text{ mA}$	3.1	4.1	5.2	V
I_{GES}	Gate Leakage Current	$V_{GE} = 20 \text{ V}$, $V_{CE} = 0 \text{ V}$	—	—	1000	nA

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
INNER IGBT (Q2, Q3)							
$t_{d(on)}$	Turn-On Delay Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 15 \Omega$	—	188	—	ns	
t_r	Rise Time		—	67	—		
$t_{d(off)}$	Turn-Off Delay Time		—	749	—		
t_f	Fall Time		—	48	—		
E_{on}	Turn-On Switching Loss per Pulse		—	4.8	—	mJ	
E_{off}	Turn Off Switching Loss per Pulse		—	6.5	—		
$t_{d(on)}$	Turn-On Delay Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 15 \Omega$	—	175	—	ns	
t_r	Rise Time		—	76	—		
$t_{d(off)}$	Turn-Off Delay Time		—	814	—		
t_f	Fall Time		—	50	—		
E_{on}	Turn-On Switching Loss per Pulse		—	5.68	—	mJ	
E_{off}	Turn Off Switching Loss per Pulse		—	6.59	—		
C_{ies}	Input Capacitance	$V_{CE} = 20 \text{ V}$, $V_{GE} = 0 \text{ V}$, $f = 10 \text{ kHz}$	—	24383	—	pF	
C_{oes}	Output Capacitance		—	383	—		
C_{res}	Reverse Transfer Capacitance		—	105	—		
Q_g	Total Gate Charge	$V_{CE} = 480 \text{ V}$, $I_C = 375 \text{ A}$, $V_{GE} = \pm 15 \text{ V}$	—	753	—	nC	
R_{thJH}	Thermal Resistance – Chip-to-Heatsink	Thermal grease, Thickness = 2 Mil $\pm 2\%$, $A = 2.8 \text{ W/mK}$	—	0.31	—	°C/W	
R_{thJC}	Thermal Resistance – Chip-to-Case		—	0.15	—	°C/W	
INVERSE DIODES (D1, D2, D3, D4)							
V_F	Diode Forward Voltage	$I_F = 100 \text{ A}$, $T_J = 25^\circ\text{C}$	—	2.25	3.1	V	
		$I_F = 100 \text{ A}$, $T_J = 175^\circ\text{C}$	—	1.69	—		
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 15 \Omega$	—	24.4	—	ns	
			—	0.49	—		
Q_{rr}	Reverse Recovery Charge		—	32	—	°C	
			—	2365	—		
I_{RRM}	Peak Reverse Recovery Current		—	0.096	—	mJ	
			—	104	—		
di/dt	Peak Rate of Fall of Recovery Current	$T_J = 125^\circ\text{C}$ $V_{CE} = 400 \text{ V}$, $I_C = 200 \text{ A}$ $V_{GE} = -5 \text{ V to } +15 \text{ V}$, $R_G = 15 \Omega$	—	2.54	—	°C	
			—	58	—		
E_{rr}	Reverse Recovery Energy		—	2116	—	A/μs	
			—	0.608	—		
t_{rr}	Reverse Recovery Time		—	0.57	—	°C/W	
			—	0.41	—		
Q_{rr}	Reverse Recovery Charge		—	0.41	—	°C/W	
			—	104	—		
I_{RRM}	Peak Reverse Recovery Current		—	58	—	A	
			—	2.54	—		
di/dt	Peak Rate of Fall of Recovery Current		—	2116	—	A/μs	
			—	0.608	—		
E_{rr}	Reverse Recovery Energy		—	0.608	—	mJ	
			—	104	—		
R_{thJH}	Thermal Resistance – Chip-to-Heatsink		—	0.57	—	°C/W	
			—	0.41	—		
THERMISTOR PROPERTIES							
R_{25}	Nominal Resistance	$T = 25^\circ\text{C}$	—	22	—	kΩ	
R_{100}	Nominal Resistance	$T = 100^\circ\text{C}$	—	1486	—	Q	
R/R	Deviation of R_{25}		-5	—	5	%	
P_D	Power Dissipation		—	200	—	mW	
	Power Dissipation Constant		—	2	—	mW/K	
	B-value	B (25/50), tolerance $\pm 3\%$	—	3950	—	K	
	B-value	B (25/100), tolerance $\pm 3\%$	—	3998	—	K	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS – IGBT Q1-1, Q1-2, Q4-1, Q4-2 AND DIODE D1, D4

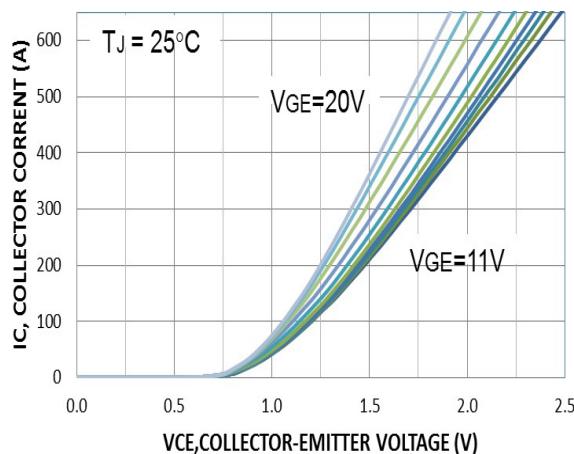


Figure 2. Typical Output Characteristics

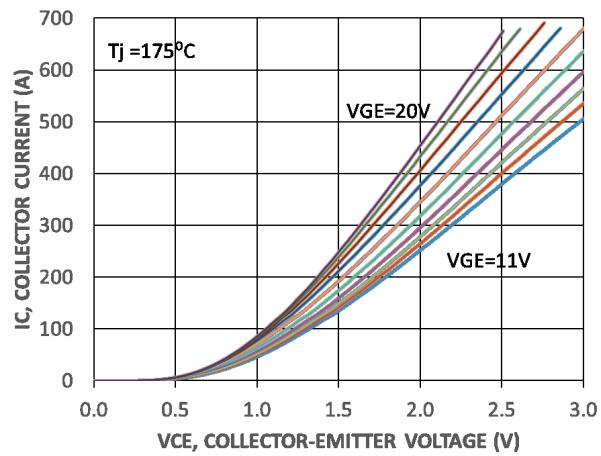


Figure 4. Typical Output Characteristics

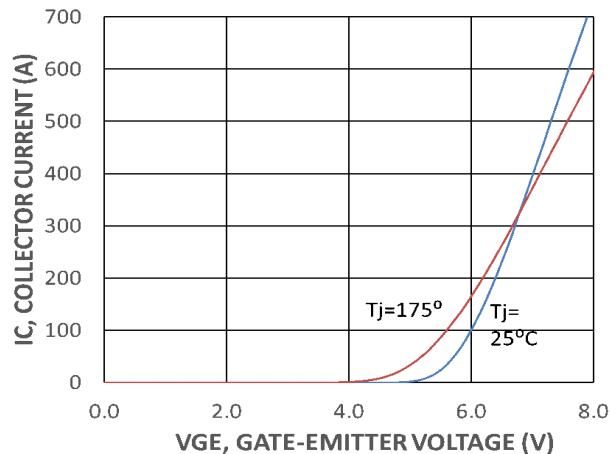


Figure 3. Typical Transfer Characteristics

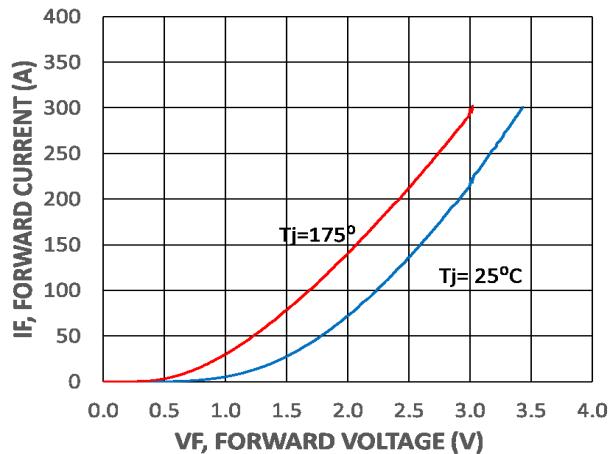


Figure 5. Typical Transfer Characteristics

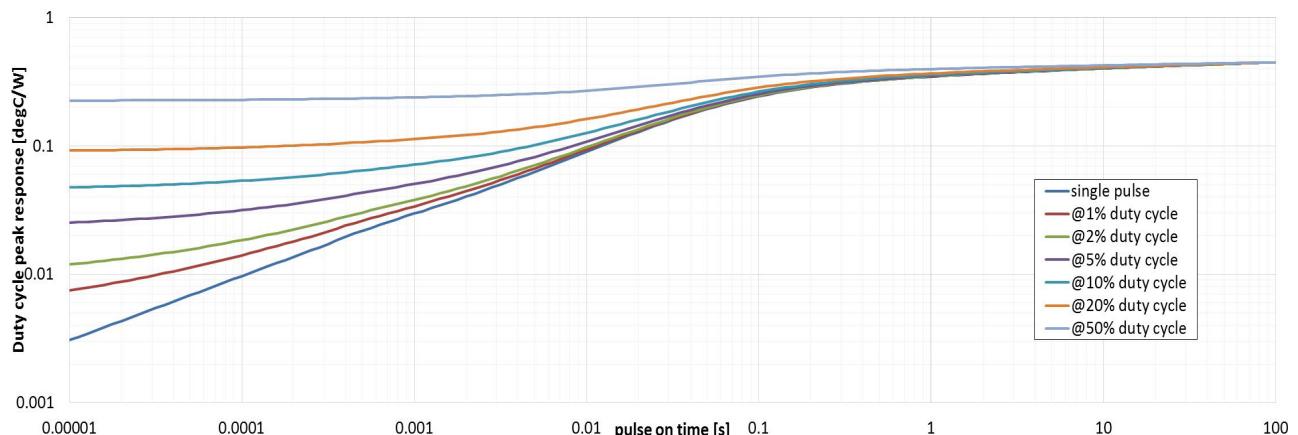


Figure 6. Transient Thermal Impedance (Q1-1, Q1-2, Q4-1, Q4-2)

TYPICAL CHARACTERISTICS – IGBT Q1-1, Q1-2, Q4-1, Q4-2 AND DIODE D1, D4 (continued)

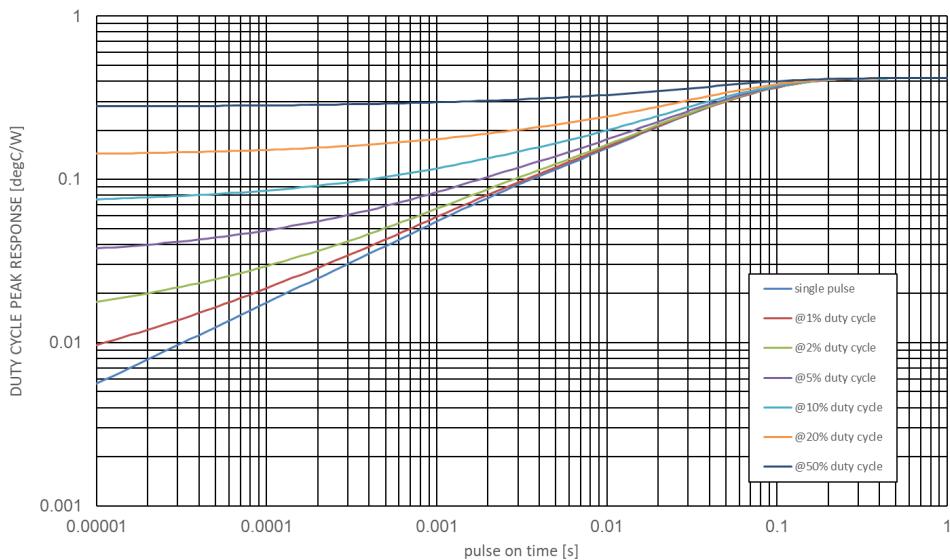


Figure 7. Transient Thermal Impedance (D1, D4)

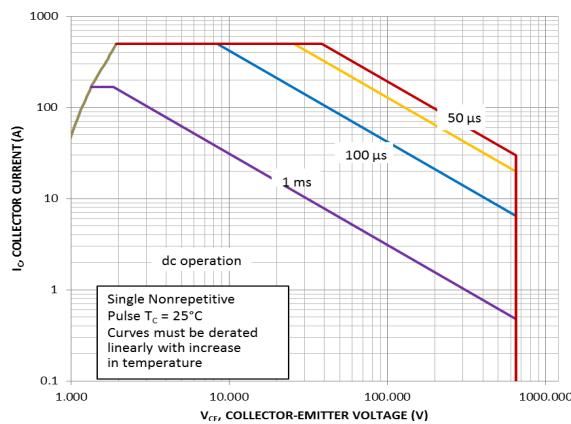


Figure 8. FBSOA (Q1-1, Q1-2, Q4-1, Q4-2)

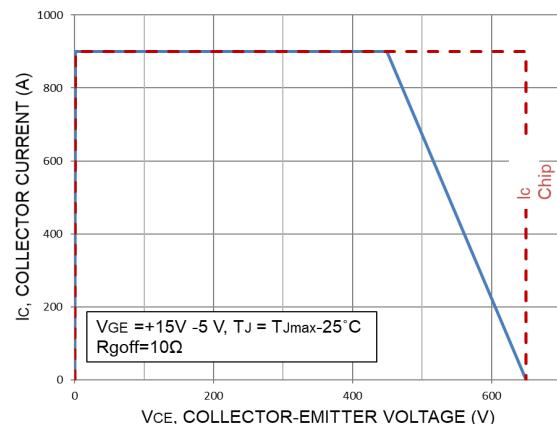


Figure 9. RBSOA (Q1, Q4)

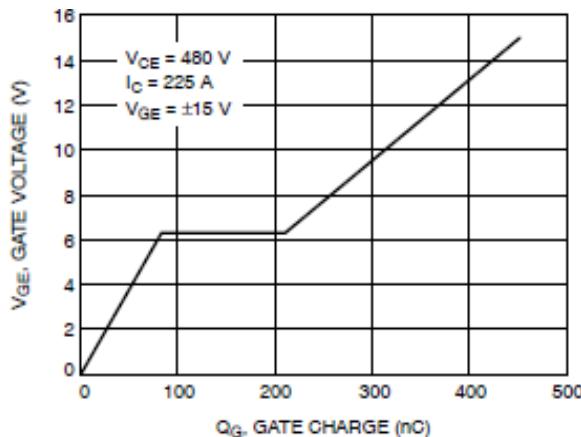


Figure 10. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3

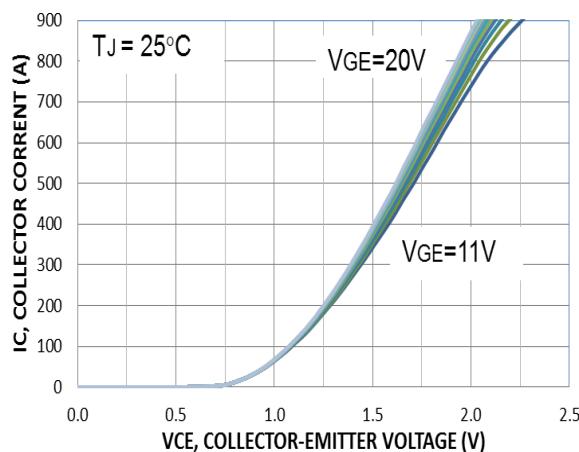


Figure 11. Typical Output Characteristics

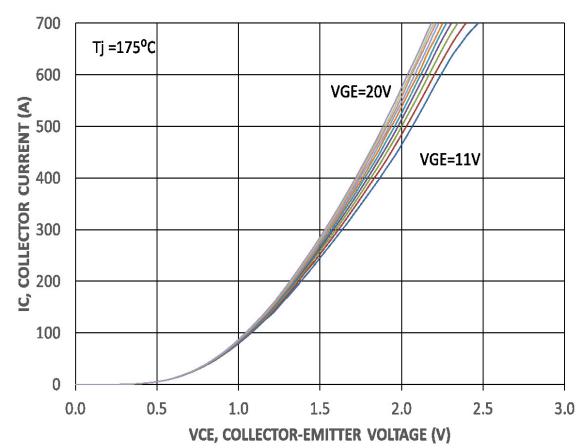


Figure 12. Typical Output Characteristics

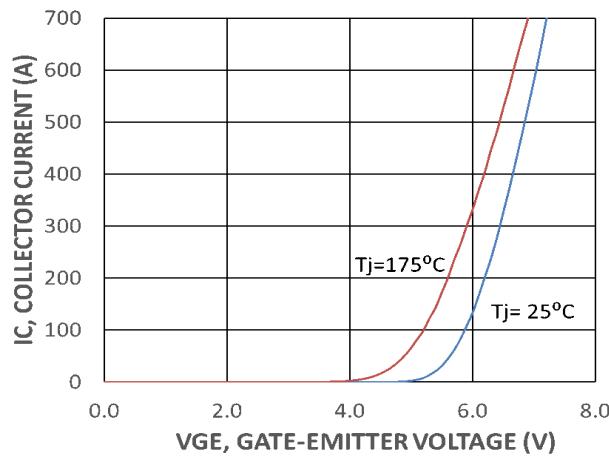


Figure 13. Typical Transfer Characteristics

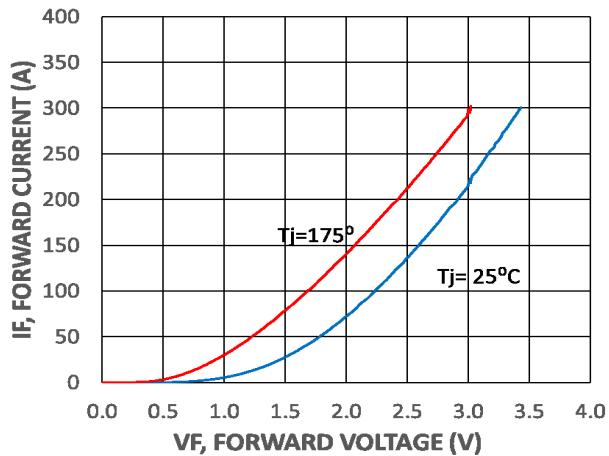


Figure 14. Typical Transfer Characteristics

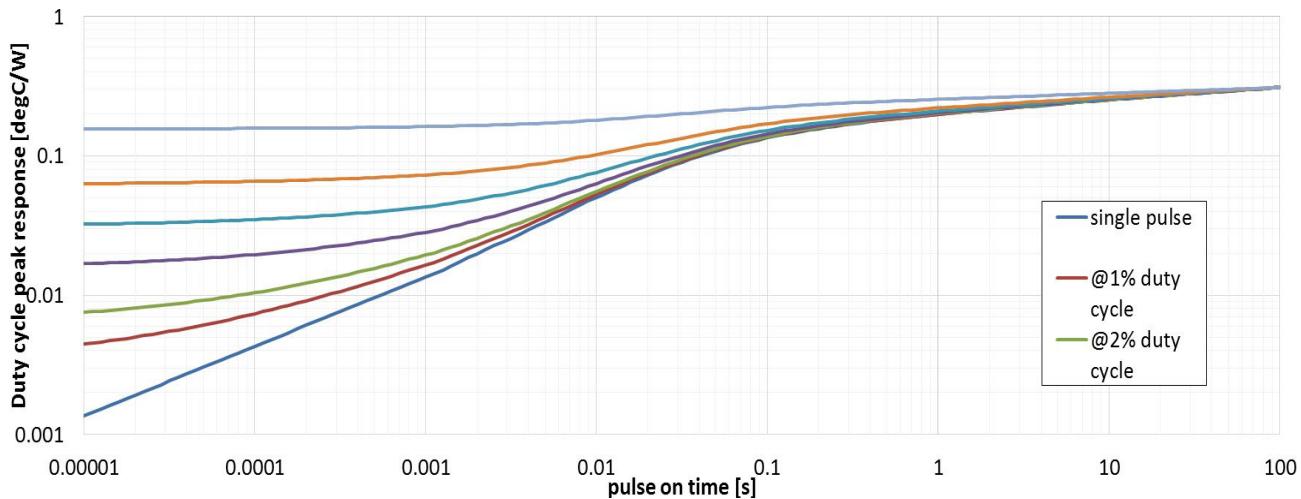


Figure 15. Transient Thermal Impedance (Q2, Q3)

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3 (continued)

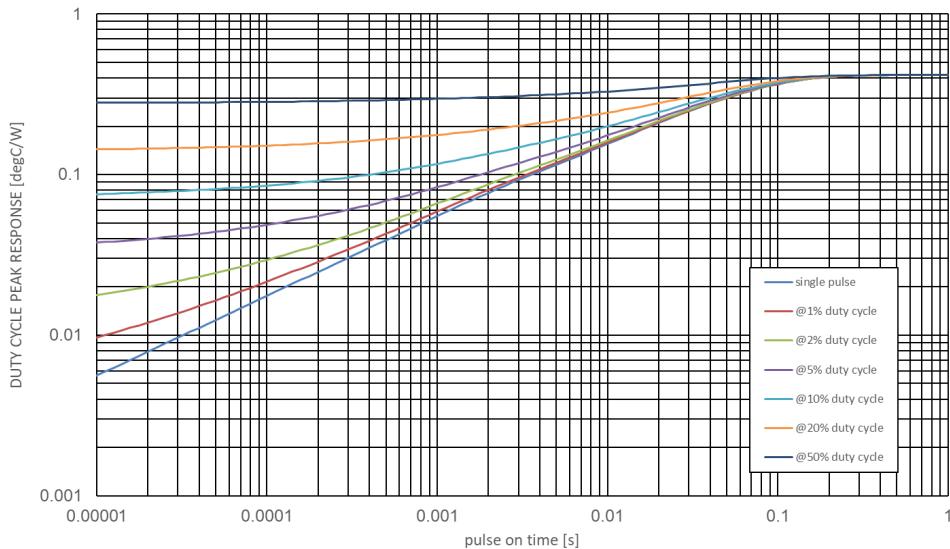


Figure 16. Transient Thermal Impedance (D2, D3)

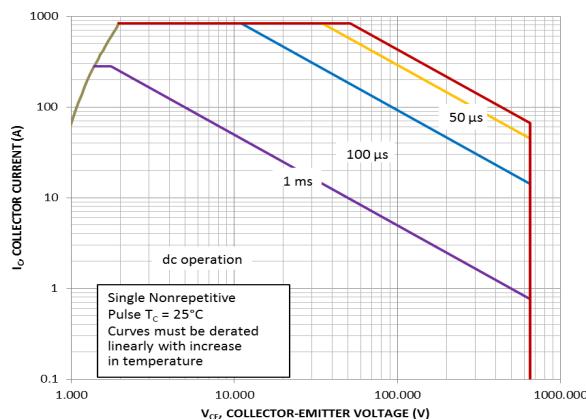


Figure 17. FBSOA (Q2, Q3)

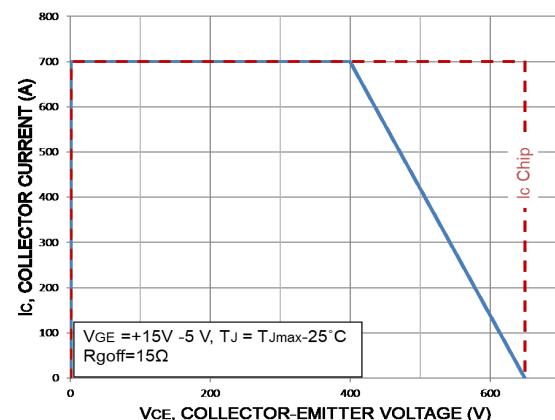


Figure 18. RBSOA (Q2, Q3)

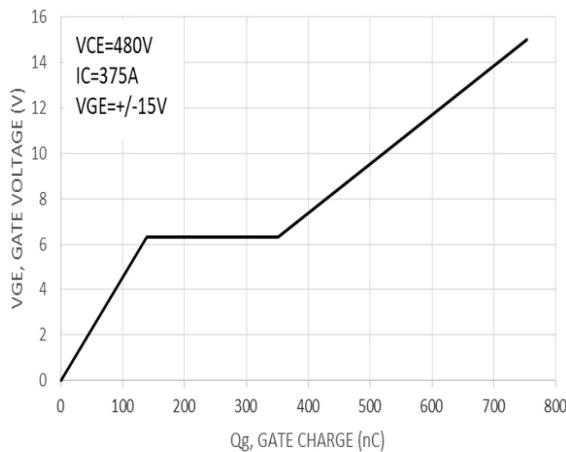
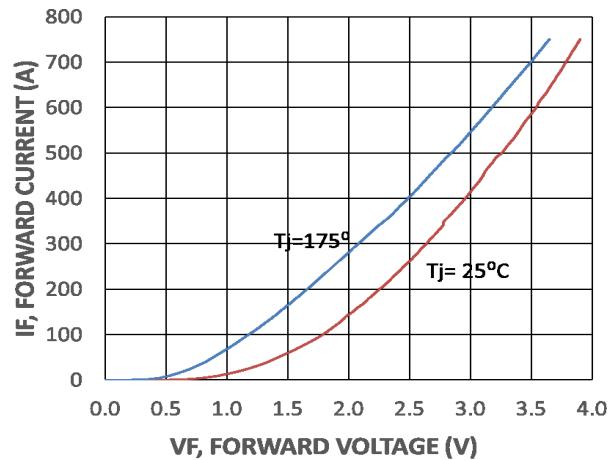
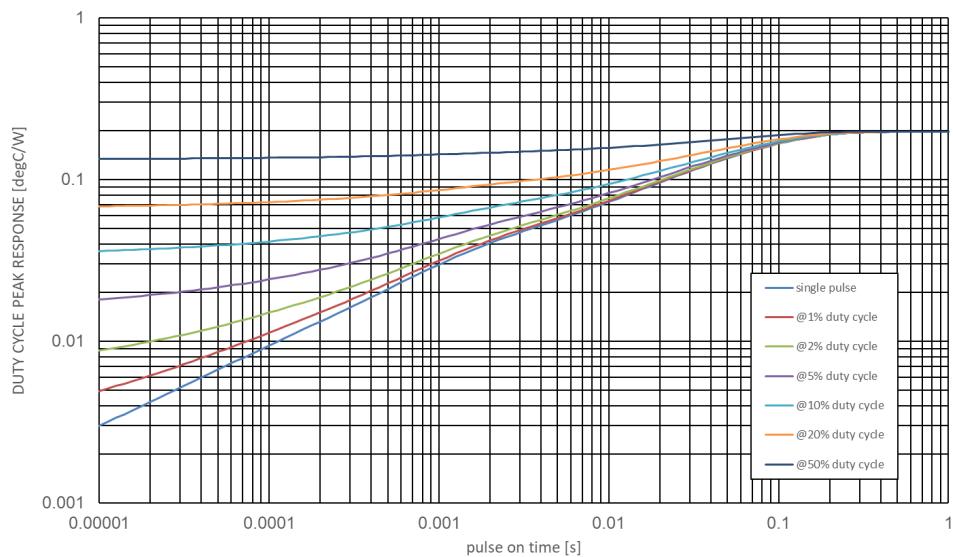
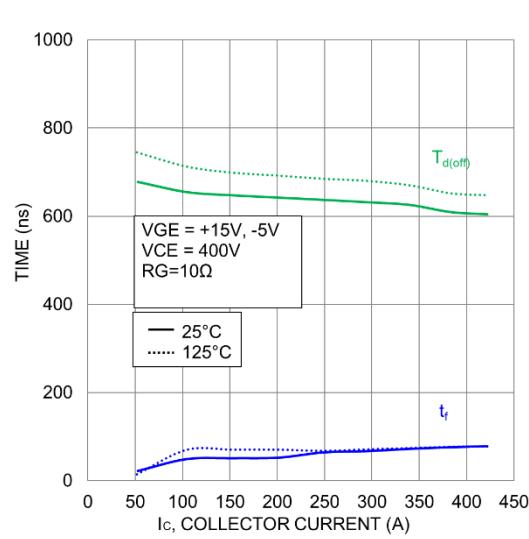
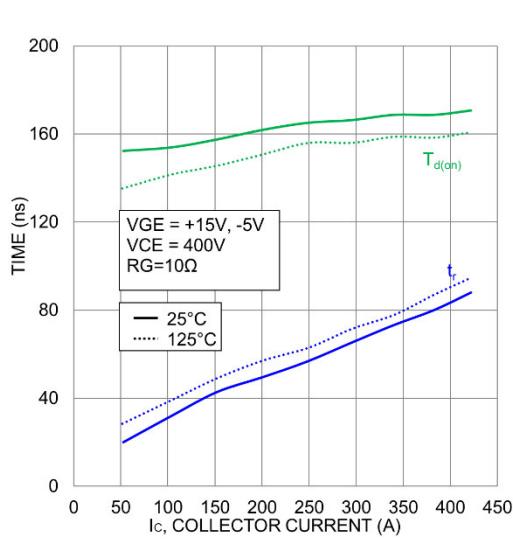
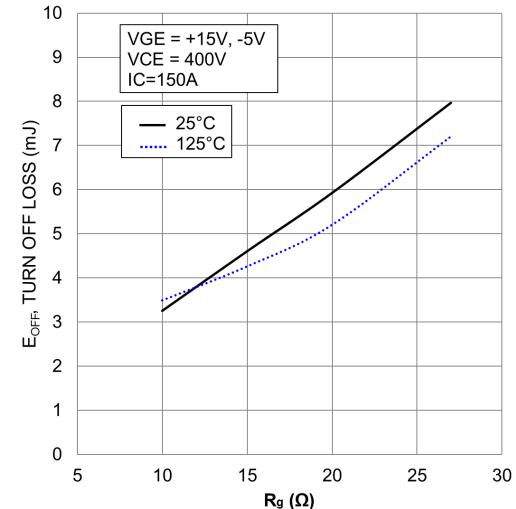
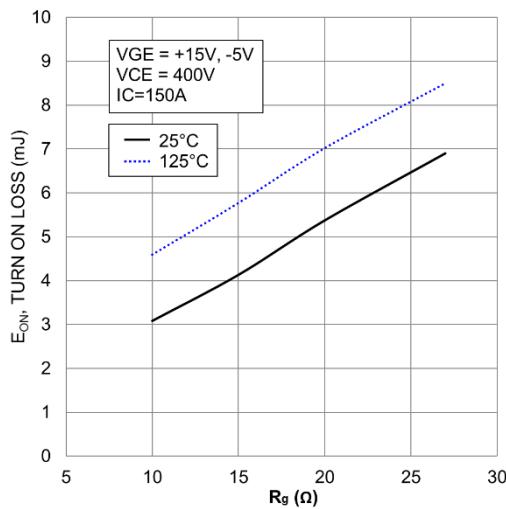
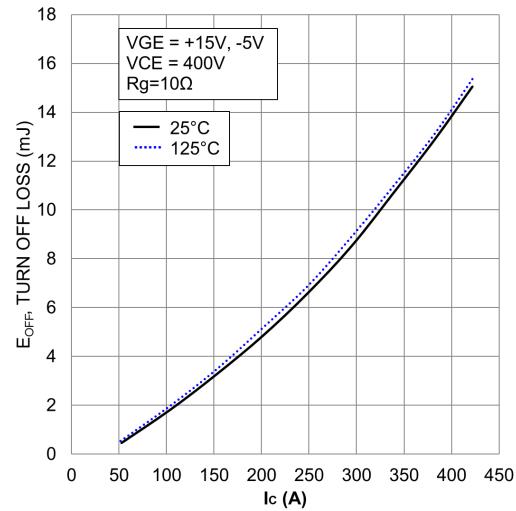
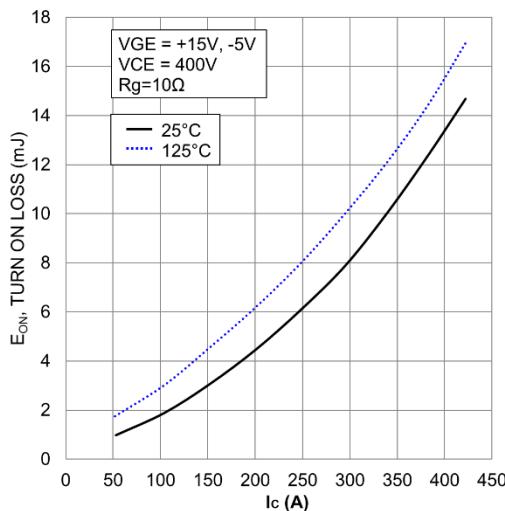


Figure 19. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – DIODE D5, D6**Figure 20. Diode Forward Characteristics****Figure 21. Transient Thermal Impedance (D5, D6)**

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE



TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE (continued)

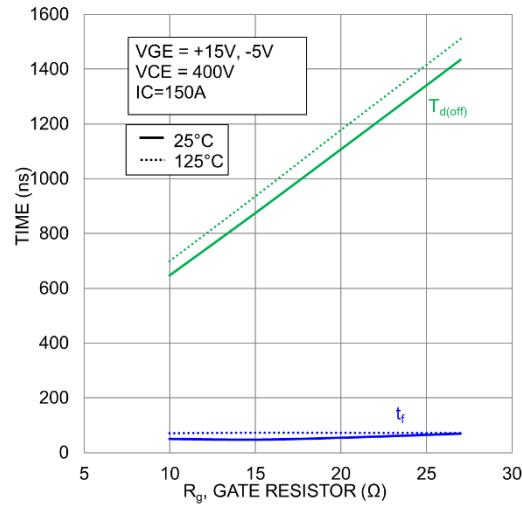
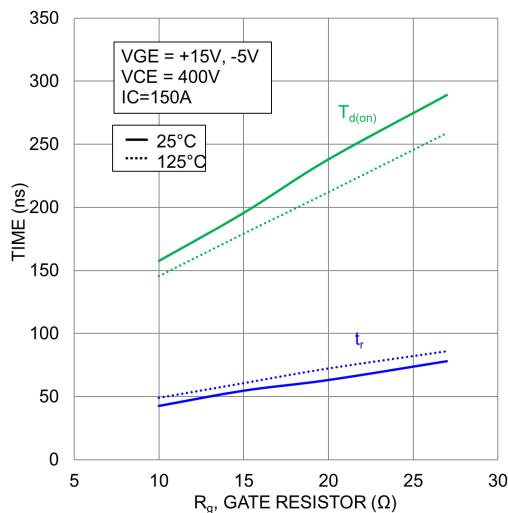


Figure 28. Typical Switching Time $T_{d(on)}$ vs. R_G

Figure 29. Typical Switching Time $T_{d(off)}$ vs. R_G

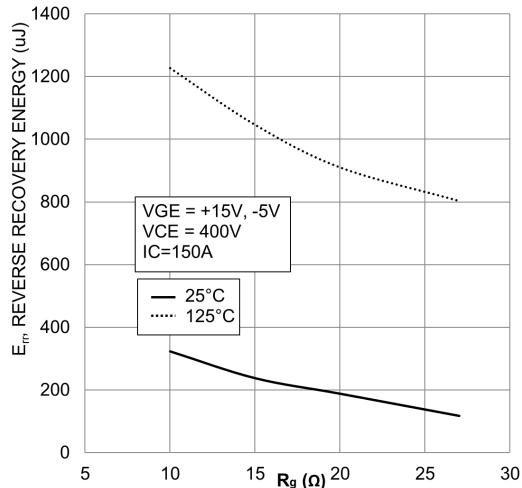
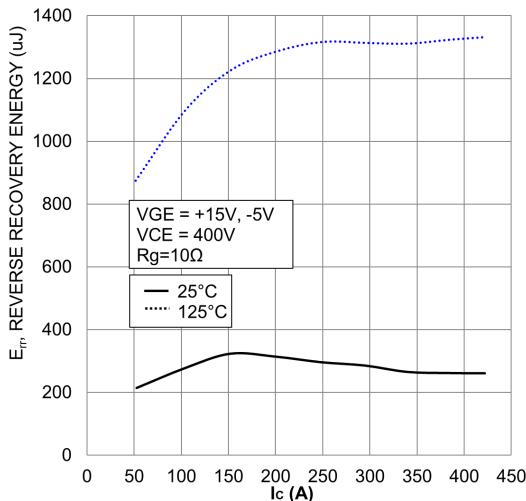


Figure 30. Typical Reverse Recovery Energy vs. IC

Figure 31. Typical Reverse Recovery Energy vs. RG

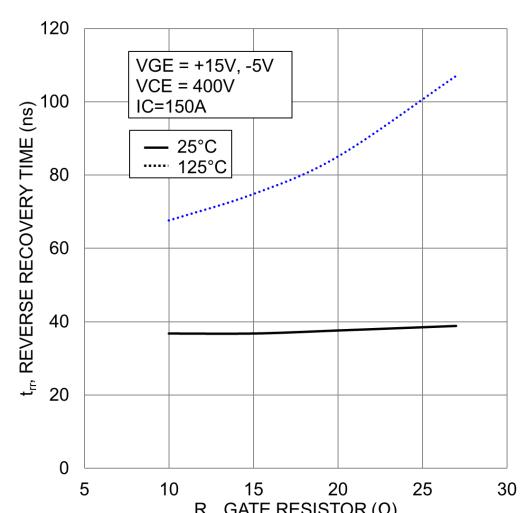
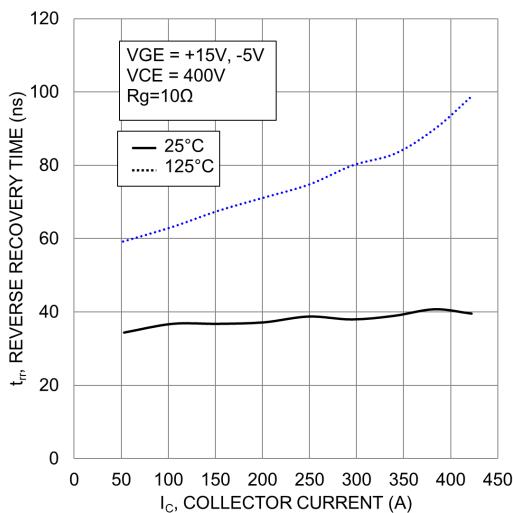
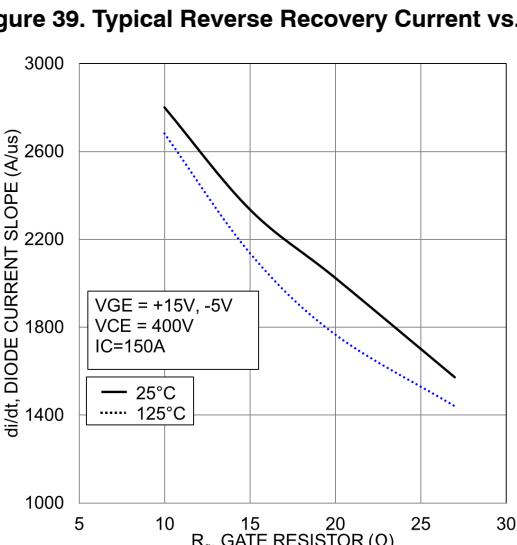
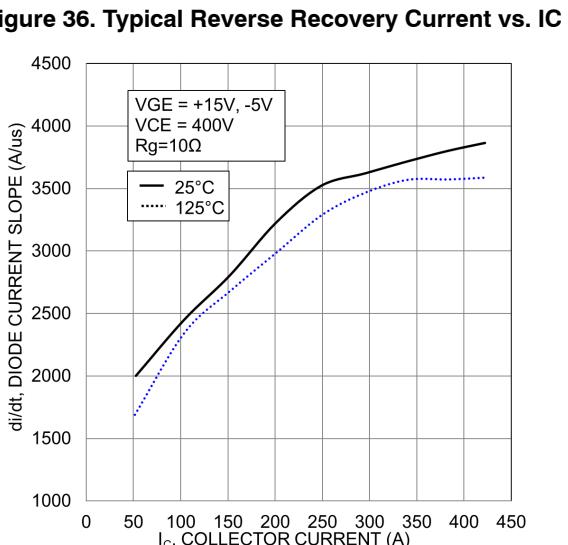
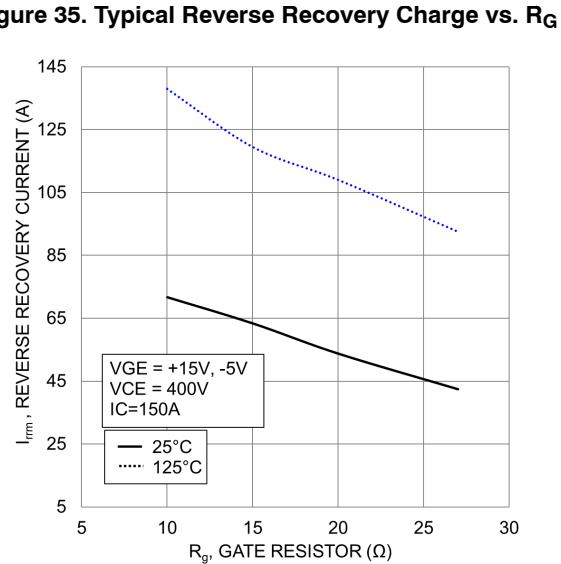
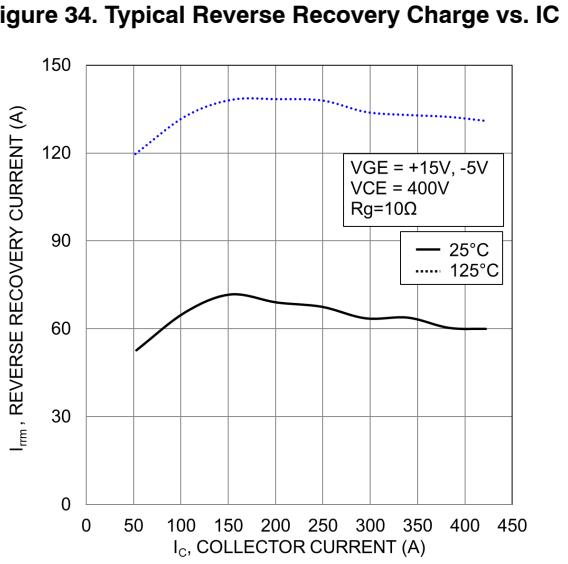
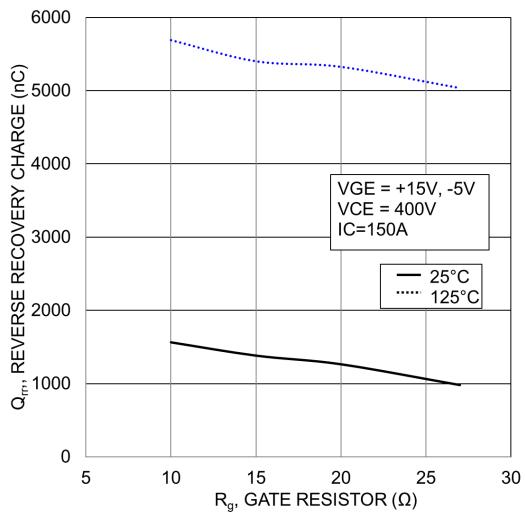
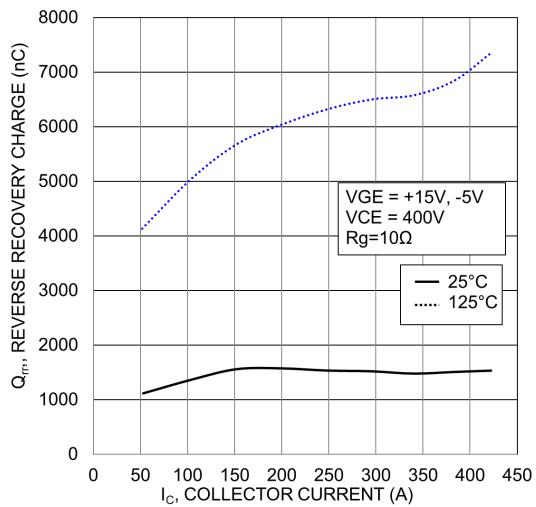


Figure 32. Typical Reverse Recovery Time vs. IC

Figure 33. Typical Reverse Recovery Time vs. RG

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE (continued)



TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE

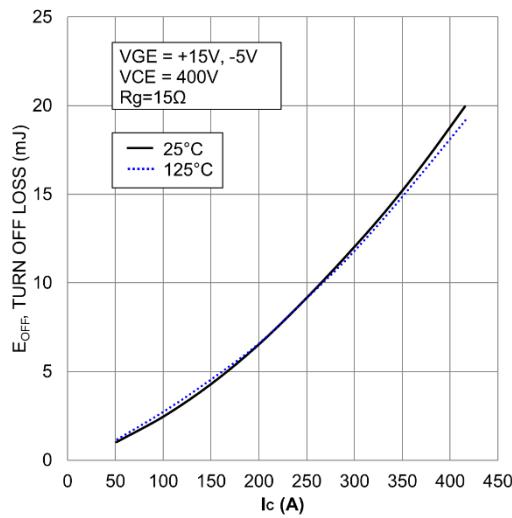
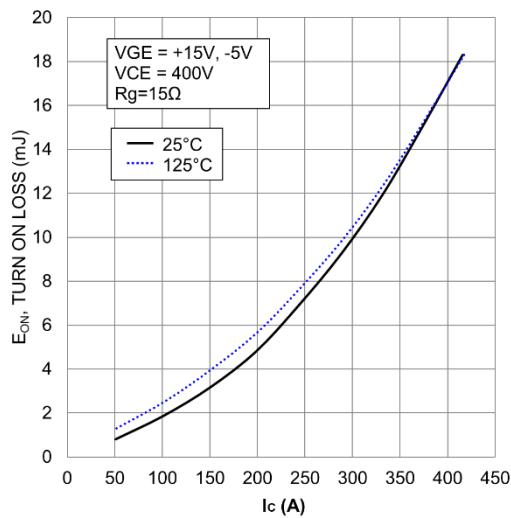


Figure 40. Typical Switching Loss E_{ON} vs. IC

Figure 45. Typical Switching Loss E_{OFF} vs. IC

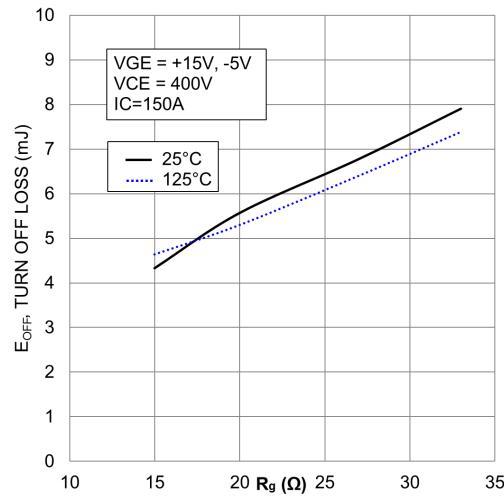
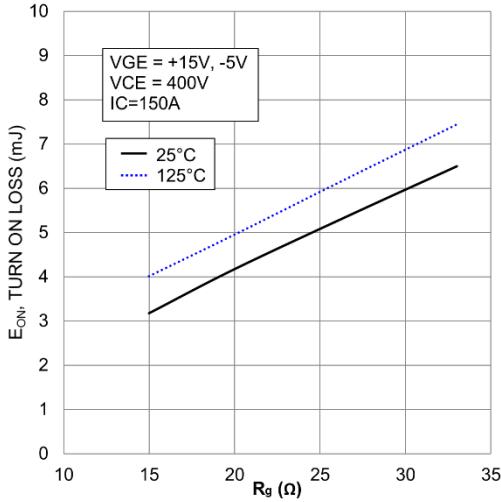


Figure 41. Typical Switching Loss E_{ON} vs. R_G

Figure 42. Typical Switching Loss E_{OFF} vs. R_G

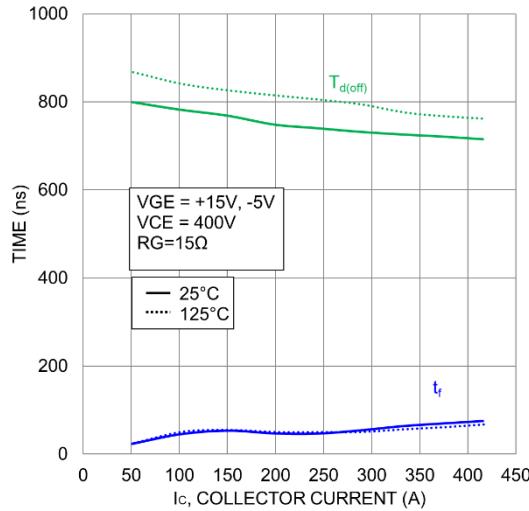
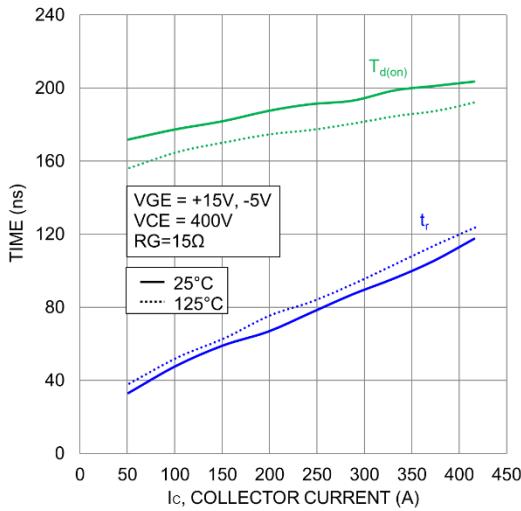


Figure 43. Typical Turn-On Switching Time vs. IC

Figure 44. Typical Turn-Off Switching Time vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE (continued)

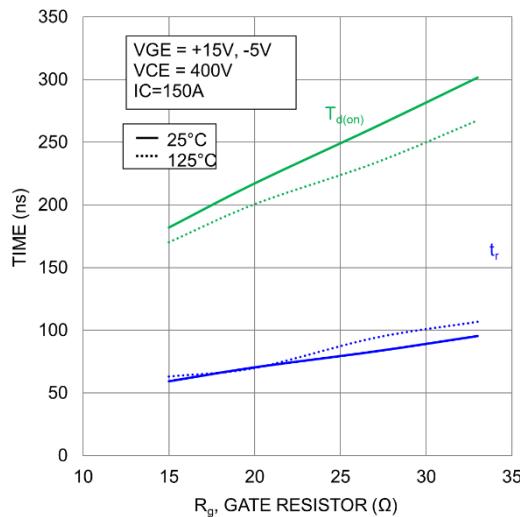


Figure 46. Typical Turn-On Switching Time vs. R_g

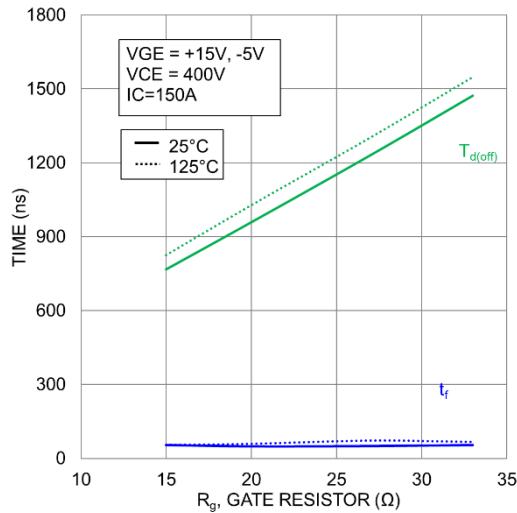


Figure 47. Typical Turn-Off Switching Time vs. R_g

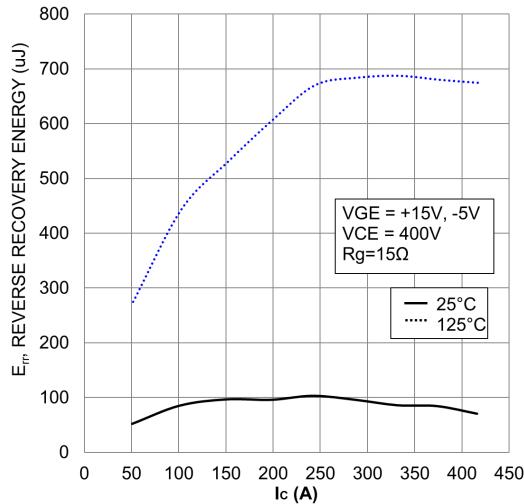


Figure 48. Typical Reverse Recovery Energy Loss vs. IC

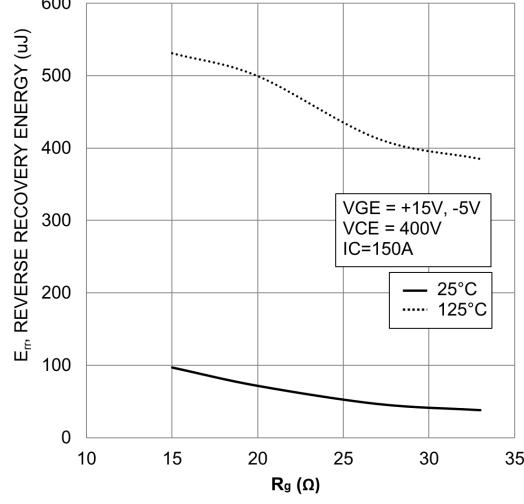


Figure 51. Typical Reverse Recovery Energy Loss vs. R_g

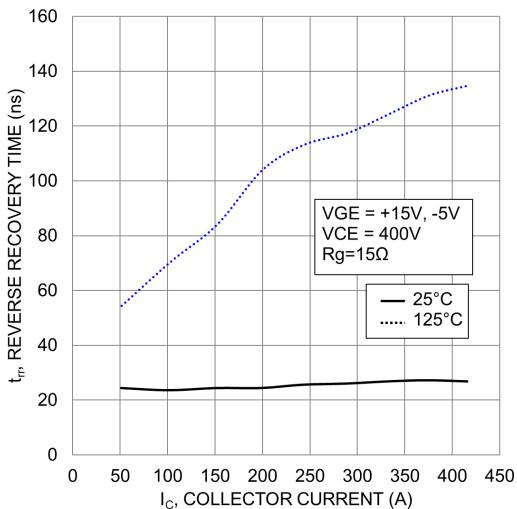


Figure 49. Typical Reverse Recovery Time vs. IC

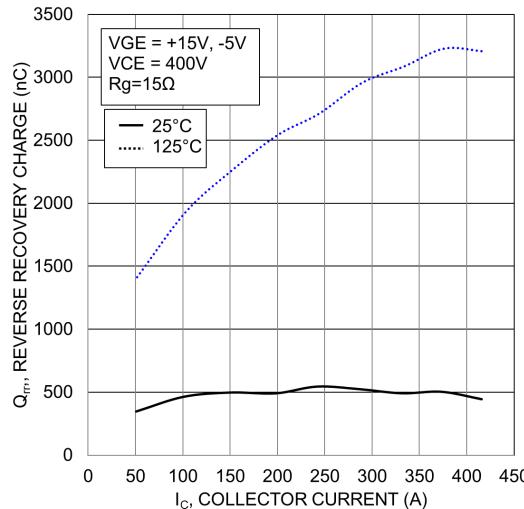
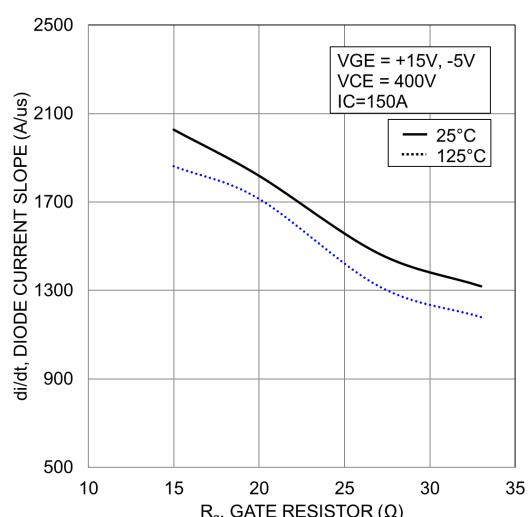
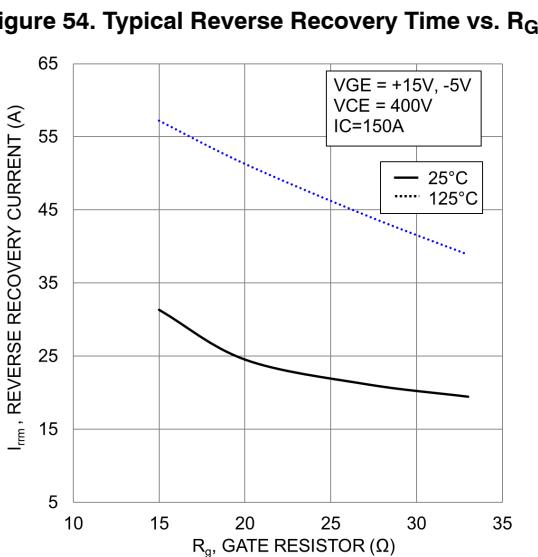
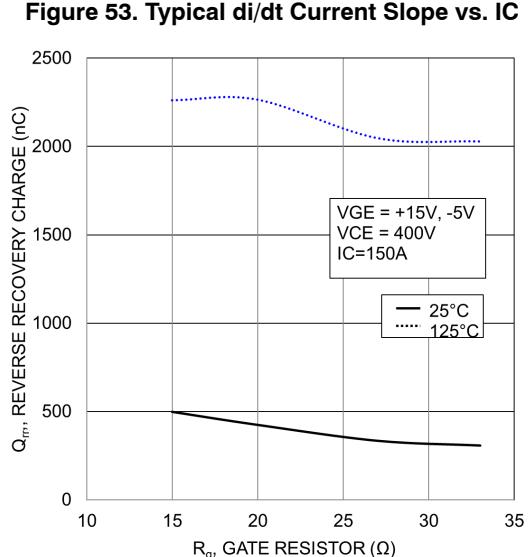
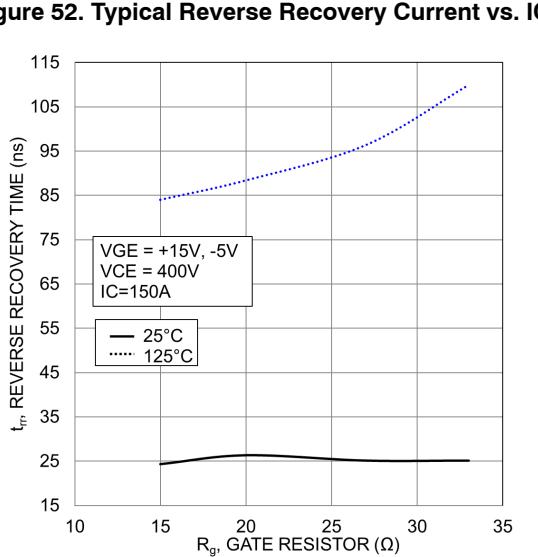
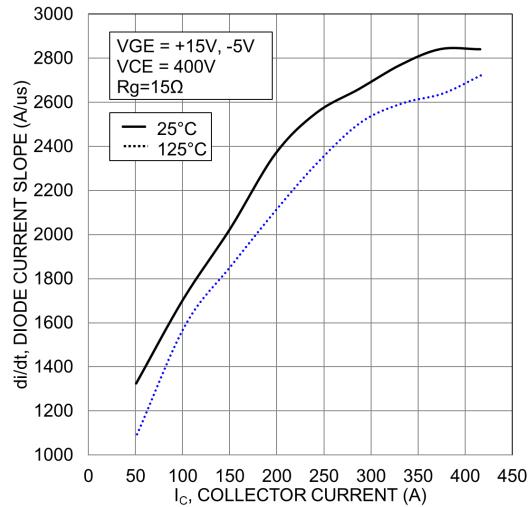
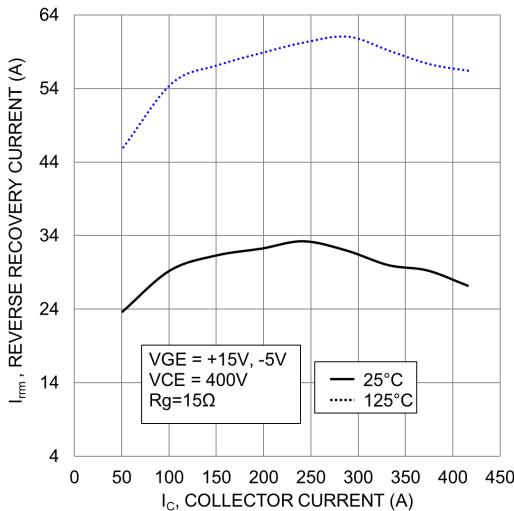


Figure 50. Typical Reverse Recovery Charge vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE (continued)



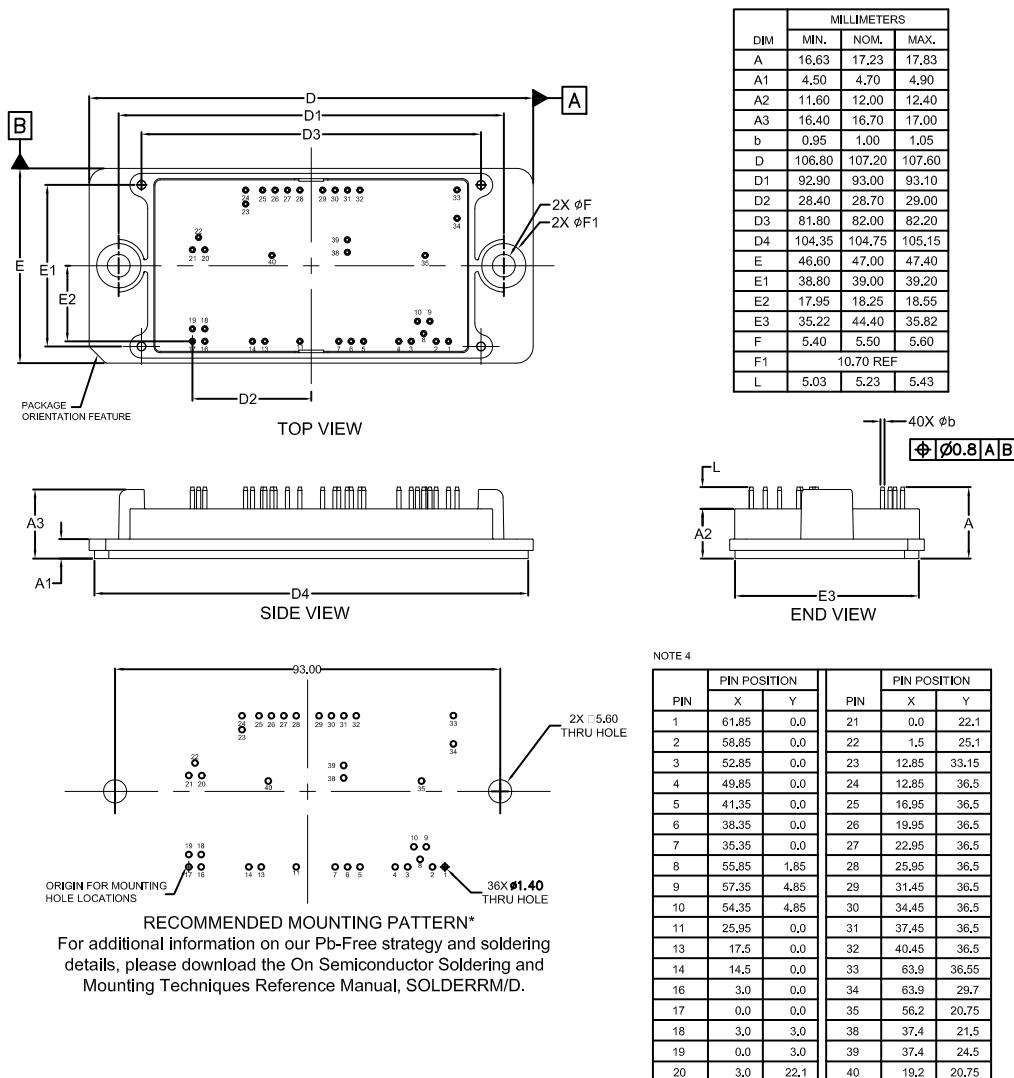
NXH450N65L4Q2F2S1G

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH450N65L4Q2F2S1G	NXH450N65L4Q2F2S1G	PIM40, Q2PACK (Pb-Free and Halide-Free)	12 Units / Blister Tray

PACKAGE DIMENSIONS

PIM40, 107.2x47
CASE 180BE
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b APPLY TO THE PLATED TERMINALS AND ARE MEASURED WHERE THE PIN EXITS THE PACKAGE BODY.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM PIN 17. POSITIONAL TOLERANCE, AS NOTED IN THE DRAWING, APPLIES TO EACH TERMINAL.

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