ISL95712

Multiphase PWM Regulator for AMD Fusion™ Desktop CPUs Using SVI 2.0

FN8566
Rev 1.00
November 2, 2015

The ISL95712 is fully compliant with AMD Fusion™ SVI 2.0 and provides a complete solution for microprocessor and graphics processor core power. The ISL95712 controller supports two Voltage Regulators (VRs) for Core and Northbridge outputs. The Core VR can be configured for 4-, 3-, 2-, or 1-phase operation while the Northbridge VR supports 3-, 2- or 1-phase configurations for maximum flexibility. The two VRs share a serial control bus to communicate with the AMD CPU and achieve lower cost and smaller board area compared with two-chip solutions.

The PWM modulator is based on Intersil's Robust Ripple Regulator R3™ Technology. Compared to traditional modulators, the R3™ modulator can automatically change switching frequency for faster transient settling time during load transients and improved light load efficiency.

The ISL95712 has several other key features. Both outputs support DCR current sensing with a single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. They also utilize remote voltage sense, adjustable switching frequency, OC protection and power-good indicators.

Applications

- AMD Fusion CPU/GPU core power
- Desktop computers

Features

- Supports AMD SVI 2.0 serial data bus interface and PMBus
  - Serial VID clock frequency range 100kHz to 25MHz
- Dual output controller with 12V integrated core gate drivers
- Precision voltage regulation
  - 0.5% system accuracy over-temperature
  - 0.5V to 1.55V in 6.25mV steps
  - Enhanced load line accuracy
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Programmable 1-, 2-, 3- or 4-phase for the core output and 1- , 2- or 3-phase for the Northbridge output
- Adaptive body diode conduction time reduction
- Superior noise immunity and transient response
- Output current and voltage telemetry
- Differential remote voltage sensing
- High efficiency across entire load range
- Programmable slew rate
- Programmable VID offset and droop on both outputs
- Programmable switching frequency for both outputs
- Excellent dynamic current balance between phases
- Protection: OCP/WOC, OVP, PGOOD and thermal monitor
- Small footprint 52 Ld 6x6 QFN package
  - Pb-free (RoHS compliant)

Performance

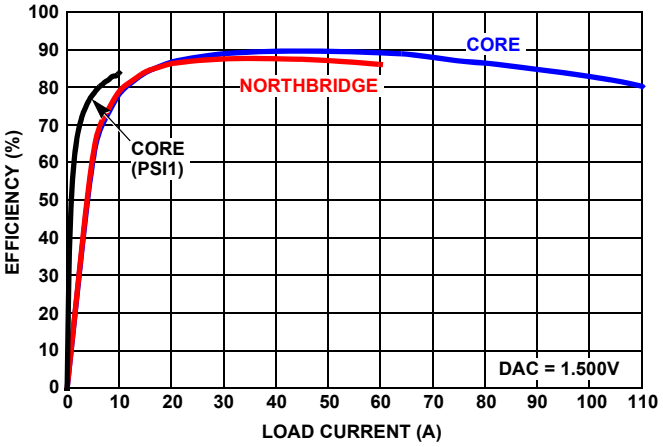

FIGURE 1. EFFICIENCY vs LOAD

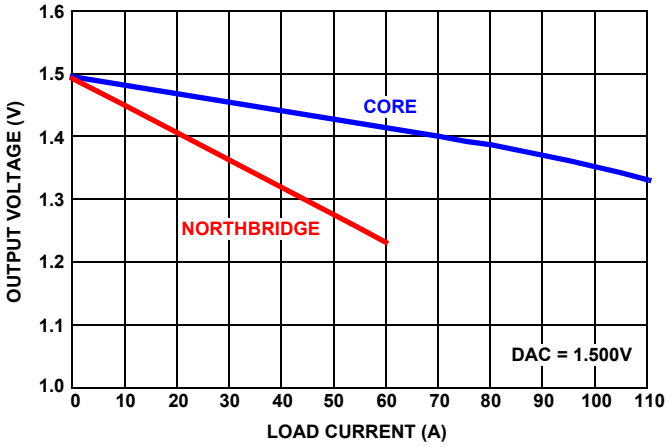

FIGURE 2. V_{OUT} vs LOAD

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Simplified Application Circuit for High Power CPU Core

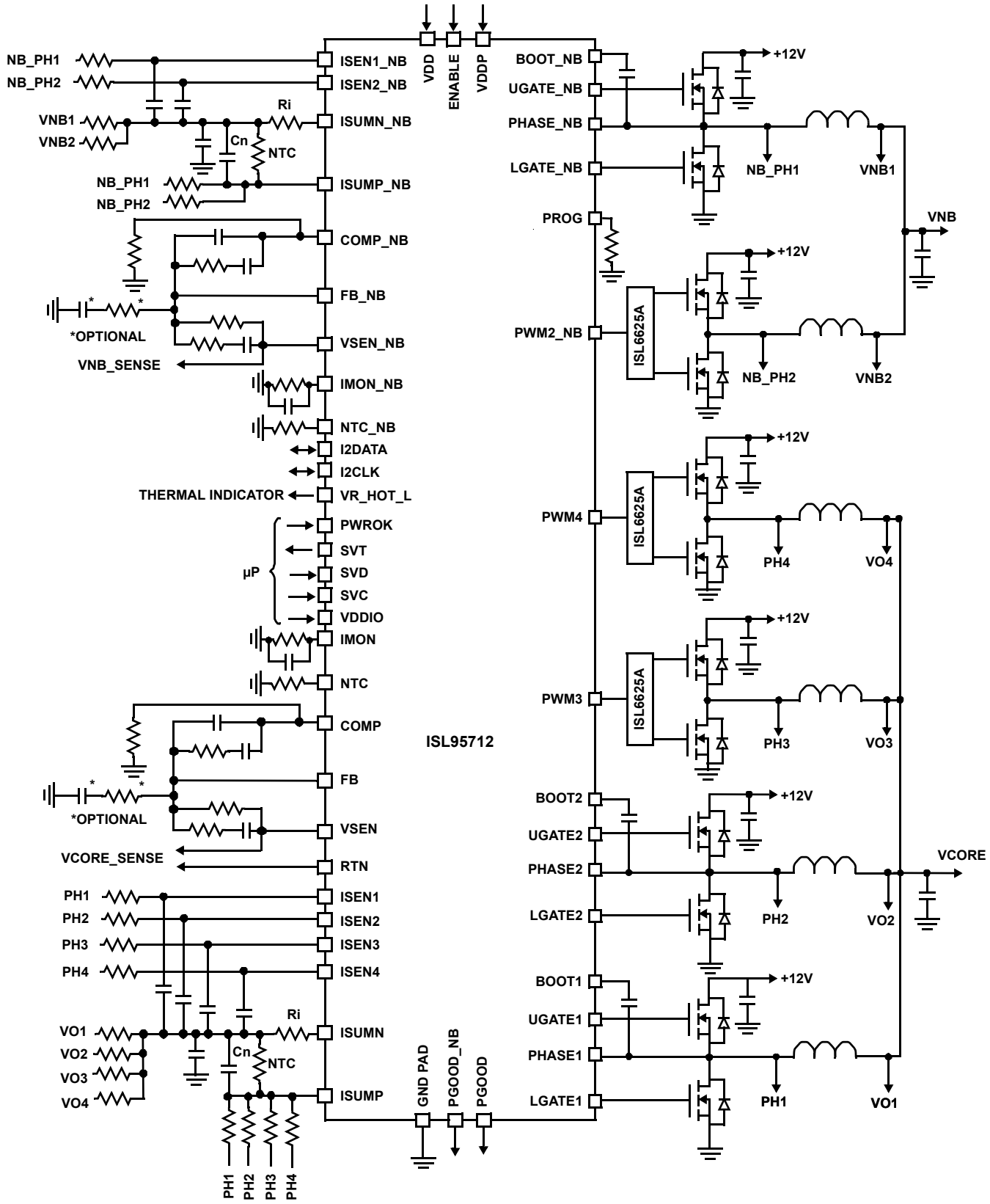
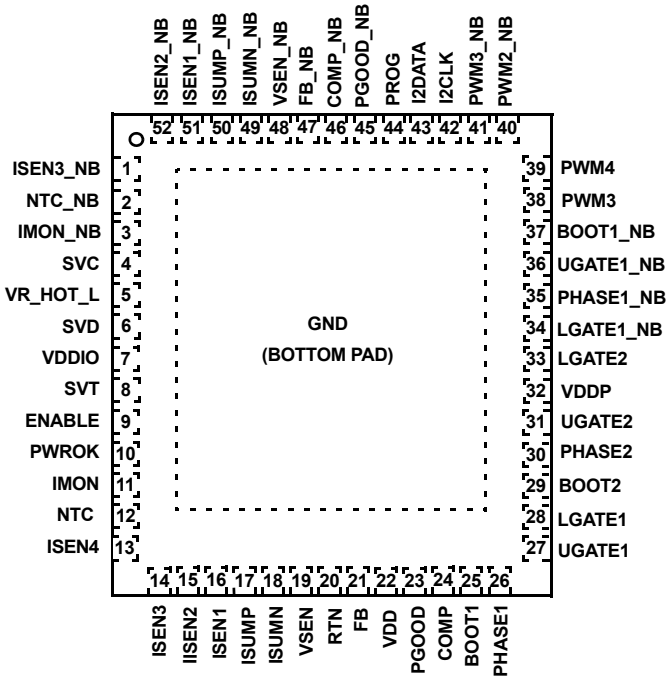


FIGURE 3. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Pin Configuration

ISL95712
(52 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	ISEN3_NB	Individual current sensing for Channel 3 of the Northbridge VR. When ISEN3_NB is pulled to +5V, the controller will disable Channel 3 and the Northbridge VR will run 2-phase.
2	NTC_NB	Thermistor input to VR_HOT_L circuit to monitor Northbridge VR temperature.
3	IMON_NB	Northbridge output current monitor. A current proportional to the Northbridge VR output current is sourced from this pin.
4	SVC	Serial VID clock input from the CPU processor master device.
5	VR_HOT_L	Thermal indicator signal to AMD CPU. Thermal overload open-drain output indicator active LOW.
6	SVD	Serial VID data bidirectional signal from the CPU processor master device to the VR.
7	VDDIO	VDDIO is the processor memory interface power rail and this pin serves as the reference to the controller IC for this processor I/O signal level.
8	SVT	Serial VID Telemetry (SVT) data line input to the CPU from the controller IC. Telemetry and VID-on-the-fly complete signal provided from this pin.
9	ENABLE	Enable input. A high level logic on this pin enables both VRs.
10	PWROK	System power-good input. When this pin is high, the SVI 2 interface is active and the I^2C protocol is running. While this pin is low, the SVC and SVD input states determine the pre-PWROK metal VID. This pin must be low prior to the ISL95712 PGOOD output going high per the AMD SVI 2.0 Controller Guidelines.
11	IMON	Core output current monitor. A current proportional to the Core VR output current is sourced from this pin.
12	NTC	Thermistor input to VR_HOT_L circuit to monitor Core VR temperature.
13	ISEN4	ISEN4 is the individual current sensing for Channel 4 of the Core VR. When ISEN4 is pulled to +5V, the controller disables Channel 4, and the Core VR runs in three-phase mode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
14	ISEN3	ISEN3 is the individual current sensing for Channel 3 of the Core VR. When ISEN3 is pulled to +5V, the controller disables Channel 3, and the Core VR runs in two-phase mode.
15	ISEN2	Individual current sensing for Channel 2 of the Core VR. When ISEN2 is pulled to +5V, the controller disables Channel 2, and the Core VR runs in single-phase mode.
16	ISEN1	Individual current sensing for Channel 1 of the Core VR. If ISEN2 is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1 is tied to +5V, the Core portion of the IC is shut down.
17	ISUMP	Noninverting input of the transconductance amplifier for current monitor and load line of Core output.
18	ISUMN	Inverting input of the transconductance amplifier for current monitor and load line of Core output.
19	VSEN	Output voltage sense pin for the Core controller. Connect to the +sense pin of the microprocessor die.
20	RTN	Output voltage sense return pin for both Core VR and Northbridge VR. Connect to the -sense pin of the microprocessor die.
21	FB	Output voltage feedback to the inverting input of the Core controller error amplifier.
22	VDD	5V bias power. A resistor [2Ω] and a decoupling capacitor should be used from the +5V supply. A high quality, X7R dielectric MLCC capacitor is recommended.
23	PGOOD	Open-drain output to indicate the Core output is ready to supply regulated voltage. Pull-up externally to VDD or 3.3V through a resistor.
24	COMP	Core controller error amplifier output. A resistor from COMP to GND sets the Core VR offset voltage.
25	BOOT1	Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT1 pin, each time the PHASE1 pin drops below VDDP minus the voltage dropped across the internal boot diode.
26	PHASE1	Current return path for the Phase 1 high-side MOSFET gate driver of VR1. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 1.
27	UGATE1	Output of the Phase 1 high-side MOSFET gate driver of the Core VR. Connect the UGATE1 pin to the gate of the Phase 1 high-side MOSFET(s).
28	LGATE1	Output of the Phase 1 low-side MOSFET gate driver of the Core VR. Connect the LGATE1 pin to the gate of the Phase 1 low-side MOSFET(s).
29	BOOT2	Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT2 pin, each time the PHASE2 pin drops below VDDP minus the voltage dropped across the internal boot diode.
30	PHASE2	Current return path for the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 2.
31	UGATE2	Output of the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the UGATE2 pin to the gate of the Phase 2 high-side MOSFET(s).
32	VDDP	Input voltage bias for the internal gate drivers. Connect +12V to the VDDP pin. Decouple with at least 1µF of capacitance to GND. A high quality, X7R dielectric MLCC capacitor is recommended.
33	LGATE2	Output of the Phase 2 low-side MOSFET gate driver of the Core VR. Connect the LGATE2 pin to the gate of the Phase 2 low-side MOSFET(s).
34	LGATE1_NB	Output of Northbridge Phase 1 low-side MOSFET gate driver. Connect the LGATE1_NB pin to the gate of the Northbridge VR Phase 1 low-side MOSFET(s).
35	PHASE1_NB	Current return path for Northbridge VR Phase 1 high-side MOSFET gate driver. Connect the PHASE1_NB pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Northbridge Phase 1.
36	UGATE1_NB	Output of the Phase 1 high-side MOSFET gate driver of the Northbridge VR. Connect the UGATE1_NB pin to the gate of the Northbridge VR Phase 1 high-side MOSFET(s).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
37	BOOT1_NB	Connect an MLCC capacitor across the BOOT1_NB and PHASE1_NB pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT1_NB pin, each time the PHASE1_NB pin drops below VDDP minus the voltage dropped across the internal boot diode.
38	PWM3	PWM output of Channel 3 of the Core VR. Disabled if ISEN3 is tied to +5V.
39	PWM4	PWM output of Channel 4 of the Core VR. Disabled if ISEN4 is tied to +5V.
40	PWM2_NB	PWM output for Channel 2 of the Northbridge VR. Disabled when ISEN2_NB is tied to +5V.
41	PWM3_NB	PWM output for Channel 3 of the Northbridge VR. Disabled when ISEN3_NB is tied to +5V.
42, 43	I2CLK, I2DATA	SMBus/PMBus/I^2C interface used for additional communication with the controller outside of the SVI2 pins. Tie to VCC with 4.7kΩ pull-up resistor when not used.
44	PROG	A resistor from the PROG pin to GND programs the switching frequency.
45	PGOOD_NB	Open-drain output to indicate the Northbridge output is ready to supply regulated voltage. Pull-up externally to VDD or 3.3V through a resistor.
46	COMP_NB	Northbridge VR error amplifier output. A resistor from COMP_NB to GND sets the Northbridge VR offset voltage and is used to set the switching frequency for the Core VR and Northbridge VR.
47	FB_NB	Output voltage feedback to the inverting input of the Northbridge controller error amplifier.
48	VSEN_NB	Output voltage sense pin for the Northbridge controller. Connect to the +sense pin of the microprocessor die.
49	ISUMN_NB	Inverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
50	ISUMP_NB	Noninverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
51	ISEN1_NB	Individual current sensing for Channel 1 of the Northbridge VR. If ISEN1_NB is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1_NB is tied to +5V, the Northbridge portion of the IC is shutdown.
52	ISEN2_NB	Individual current sensing for Channel 2 of the Northbridge VR. When ISEN2_NB is pulled to +5V, the controller will disable Channels 2 and 3 and the Northbridge VR will run 1-phase.
	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL95712HRZ	95712 HRZ	-10 to +100	52 Ld 6x6 QFN	L52.6x6A
ISL95712IRZ	95712 IRZ	-40 to +100	52 Ld 6x6 QFN	L52.6x6A

NOTES:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95712. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.3V to +7V
Input Supply Voltage . . . . . +15V
Gate Driver Supply Voltage, V_{DDP}. . . . . -0.3V to + 15V
Boot Voltage (V_{BOOT}) . . . . . -0.3V to V_{DDP} + 15V
UGATE Voltage (V_{UGATE}). . . . . V_{PHASE} - 0.3V_{DC} to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
LGATE Voltage (V_{LGATE}) . . . . . GND - 0.3V_{DC} to V_{DDP} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{DDP} + 0.3V
PHASE Voltage (V_{PHASE}) . . . . . GND - 0.3V_{DC} to 25V_{DC}
GND - 8V (>400ns Pulse Width, 20µ) to 30V (<200ns)
Open-Drain Outputs, PGOOD, PGOOD_NB, VR_HOT_L. . . . . -0.3V to +7V
All Other Pins . . . . . -0.3V to VDD + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
52 Ld QFN Package (Notes 4, 5)	28	2.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Input Supply and Gate Drive Voltages, V_{DDP} . . . . . +12V ±5%
Ambient Temperature
HRZ. . . . . -10°C to +100°C
IRZ . . . . . -40°C to +100°C
Junction Temperature
HRZ. . . . . -10°C to +125°C
IRZ . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	ENABLE = 1V		12.5	**14.0**	mA
		ENABLE = 0V			**125**	µA
POWER-ON-RESET THRESHOLDS						
VDD POR Threshold	VDD_POR_r	V_{DD} rising		4.35	**4.50**	V
	VDD_POR_f	V_{DD} falling	**4.00**	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V	-0.5		+0.5	%
		VID = 0.25V to 0.74375V	-10		+10	mV
	IRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V	**-0.8**		**+0.8**	%
		VID = 0.25V to 0.74375V	**-12**		**+12**	mV
Maximum Output Voltage	$V_{OUT(max)}$	VID = [00000000]		1.55		V
Minimum Output Voltage	$V_{OUT(min)}$	VID = [11111111]		0		V
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$		**280**	300	**320**	kHz
Adjustment Range			**300**		**450**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset	HRZ	I_{FB} = 0A	-0.15		+0.15	mV
	IRZ	I_{FB} = 0A	**-0.20**		**+0.20**	mV
Error Amp DC Gain	A_{v0}			119		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz
ISEN						
Input Bias Current				20		nA

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER-GOOD (PGOOD AND PGOOD_NB) AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA			**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	**-1**		**1**	µA
PWROK High Threshold				750		mV
VR_HOT_L Pull-Down				11		Ω
PWROK Leakage Current					**1**	µA
VR_HOT_L Leakage Current					**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA source current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2		A
UGATE Sink Resistance	R_{UGPD}	250mA sink current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA source current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2		A
LGATE Sink Resistance	R_{LGPD}	250mA sink current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		59		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		37		ns
PROTECTION						
Overvoltage Threshold	OV_{TH}	VSEN rising above setpoint for >1µs	**275**	325	**375**	mV
Undervoltage Threshold	UV_{TH}	VSEN falls below setpoint for >1µs	**275**	325	**375**	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Way Overcurrent Trip Threshold [IMONx Current Based Detection]	$IMONx_{WOC}$	All states, I_{DROOP} = 60µA, R_{IMON} = 135kΩ		15		µA
Overcurrent Trip Threshold [IMONx Voltage Based Detection]	V_{IMONx_OCP}	All states, I_{DROOP} = 45µA, I_{IMONx} = 11.25µA, R_{IMON} = 135kΩ	**1.485**	1.510	**1.535**	V
LOGIC THRESHOLDS						
ENABLE Input Low	V_{IL}				**1**	V
ENABLE Input High	V_{IH}	HRZ	**1.6**			V
	V_{IH}	IRZ	**1.65**			V
ENABLE Leakage Current	I_{ENABLE}	ENABLE = 0V	**-1**	0	1	µA
		ENABLE = 1V			**1**	µA
SVT Impedance				50		Ω
SVC, SVD Input Low	V_{IL}	% of VDDIO			**30**	%
SVC, SVD Input High	V_{IH}	% of VDDIO	**70**			%
SVC, SVD Leakage		ENABLE = 0V, SVC, SVD = 0V and 1V	**-1**		**1**	µA
		ENABLE = 1V, SVC, SVD = 1V	**-5**		**1**	µA
		ENABLE = 1V, SVC, SVD = 0V	**-35**	-20	**-5**	µA
PWM						
PWM Output Low	V_{OL}	Sinking 5mA			**1**	V
PWM Output High	V_{OH}	Sourcing 5mA	**3.5**			V
PWM Tri-State Leakage		PWM = 2.5V			**0.5**	µA
THERMAL MONITOR						
NTC Source Current		NTC = 0.6V	**27**	30	**33**	µA
NTC Thermal Warning Voltage			**600**	640	**680**	mV

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
NTC Thermal Warning Voltage Hysteresis				20		mV
NTC Thermal Shutdown Voltage			**530**	580	**630**	mV
SLEW RATE						
VID-on-the-Fly Slew Rate		Maximum Programmed	**16**	20	**24**	mV/µs
		Minimum Programmed	**8**	10	**12**	mV/µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram

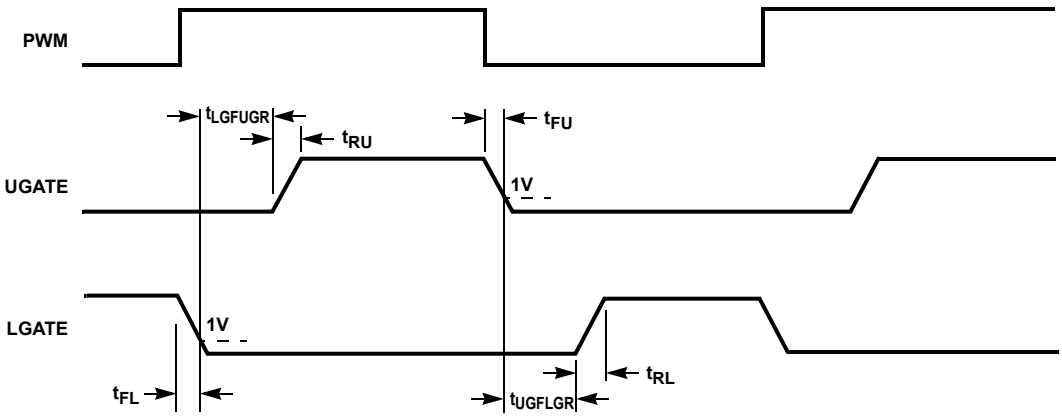


FIGURE 4. GATE DRIVER TIMING DIAGRAM

Theory of Operation

Multiphase R3™ Modulator

The ISL95712 is a multiphase regulator implementing two voltage regulators, CORE VR and Northbridge (NB) VR, on one chip controlled by AMD's™ SVI2™ protocol. The CORE VR can be programmed for 1-, 2-, 3- or 4-phase operation. The Northbridge VR can be configured for 1-, 2-, or 3-phase operation. Both regulators use the Intersil patented R3™ (Robust Ripple Regulator) modulator. The R3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 5 conceptually shows the multiphase R3™ modulator circuit, and Figure 6 shows the operation principles.

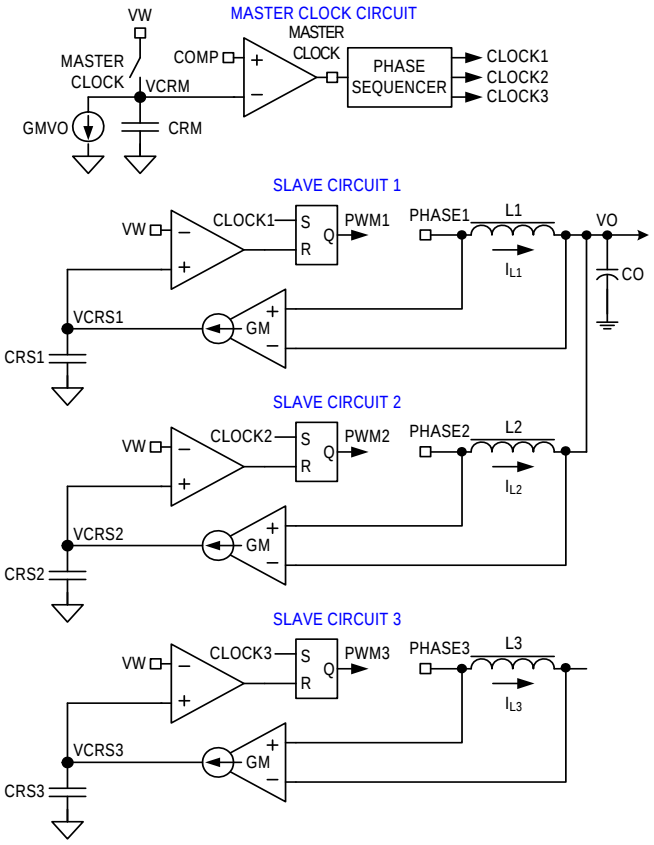


FIGURE 5. R3™ MODULATOR CIRCUIT

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage V_{CRM} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the Core VR is in 4-phase mode, the master clock signal is distributed to the four phases, and the Clock 1~4 signals will be 90° out-of-phase. If the Core VR is in 3-phase mode, the master clock signal is distributed to the three phases, and the Clock 1~3 signals will be 120° out-of-phase. If the Core VR is in 2-phase mode, the master clock signal is distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If the Core VR is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and will be the Clock1 signal.

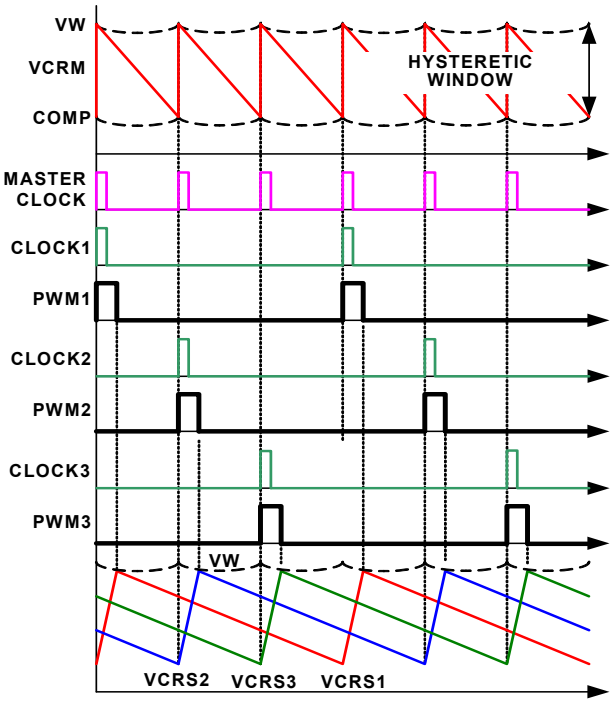


FIGURE 6. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

Each slave circuit has its own ripple capacitor C_{RS}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{RS}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{RS}. When C_{RS} voltage V_{CRS} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{RS}.

Since the controller works with V_{CRS}, which are large amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the error amplifier allows the ISL95712 to maintain a 0.5% output voltage accuracy.

Figure 7 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency. This allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL95712 excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

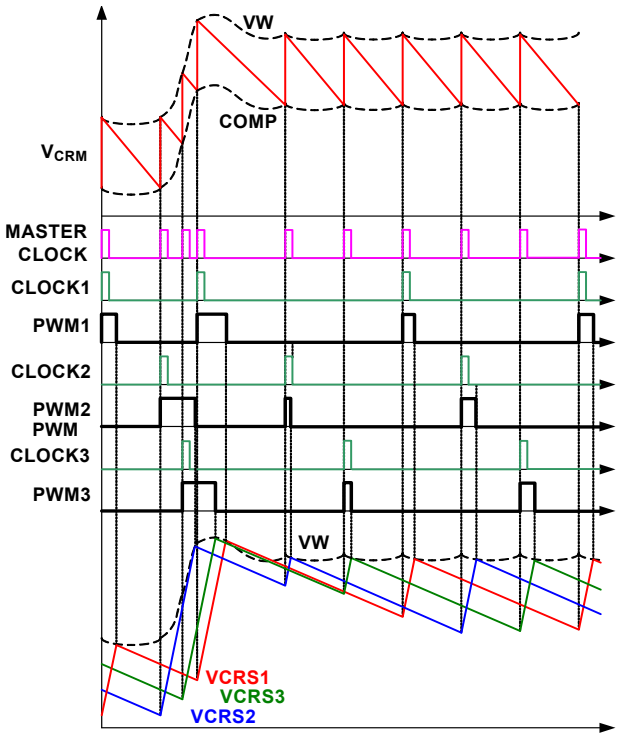


FIGURE 7. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

Diode Emulation and Period Stretching

The ISL95712 can operate in Diode Emulation (DE) mode to improve light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, thus emulating a diode. Figure 8 shows when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL95712 monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

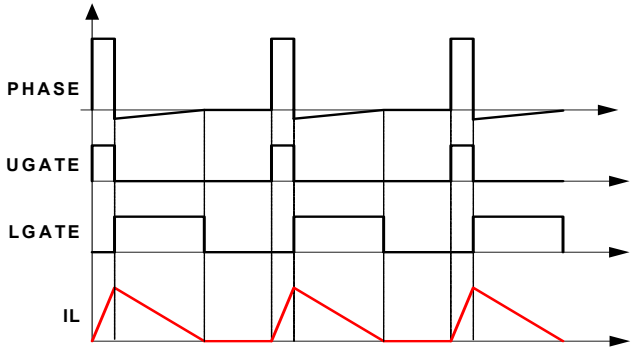


FIGURE 8. DIODE EMULATION

If the load current is light enough, as Figure 8 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM, although the controller is in DE mode.

Figure 9 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in each of the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in each of the three cases. The ISL95712 clamps the ripple capacitor voltage V_{CRS} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{CRS}, naturally stretching the switching period. The inductor current triangles move farther apart, such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

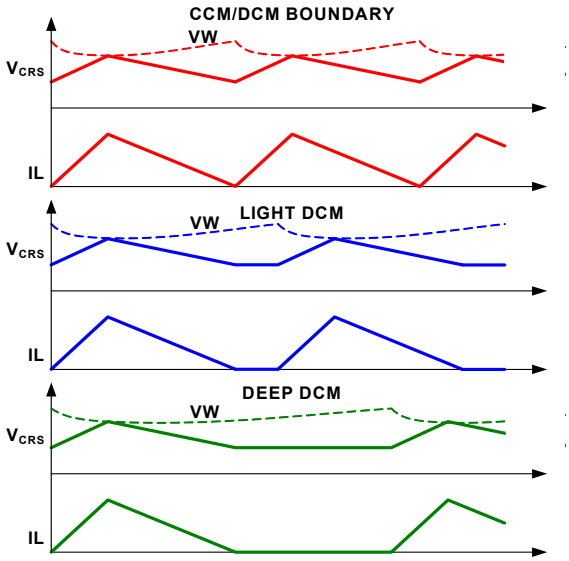


FIGURE 9. PERIOD STRETCHING

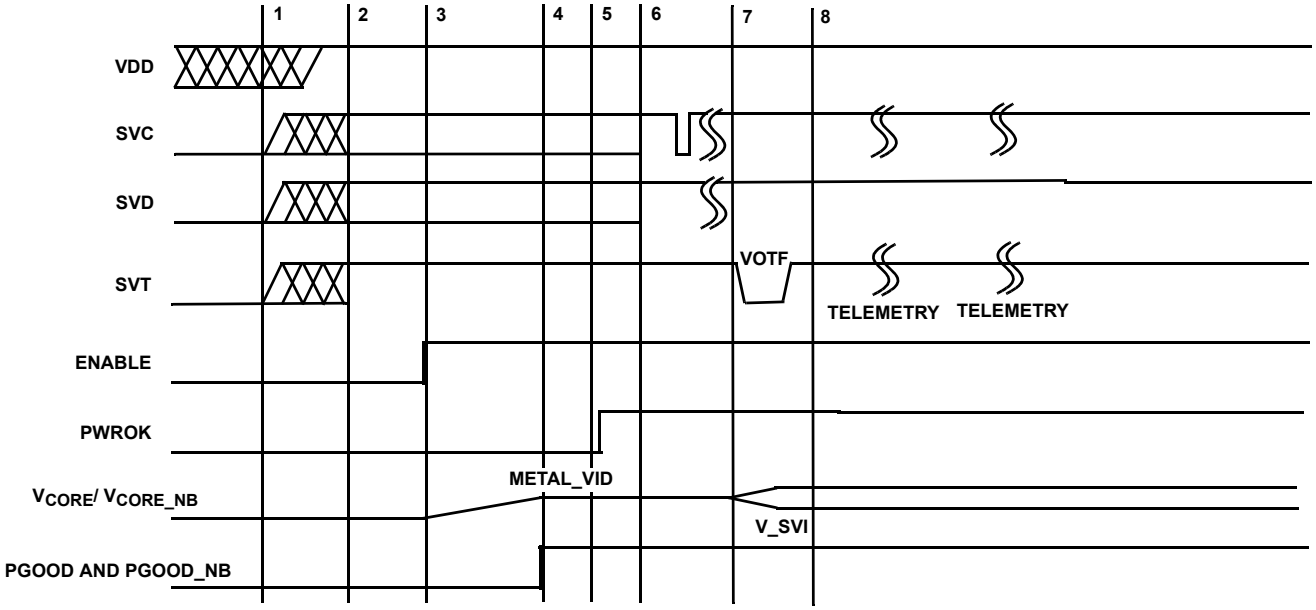
Channel Configuration

Individual PWM channels of either VR can be disabled by connecting the ISENx pin of the channel not required to +5V. For example, placing the controller in a 3+1 configuration, requires ISEN4 of the Core VR and ISEN2_NB and ISEN3_NB of the Northbridge VR to be tied to +5V. This disables Channel 4 of the Core VR and Channels 2 and 3 of the Northbridge VR. ISEN1_NB must be tied through a 10kΩ resistor to GND to prevent this pin from pulling high and disabling the channel. Similarly, if the Core VR is set to single phase mode, ISEN4, ISEN3 and ISEN2 will be tied to +5V while ISEN1 is tied to GND through a 10kΩ resistor.

Connecting ISEN1 or ISEN1_NB to +5V will disable the corresponding VR output. This feature allows debugging of individual VR outputs.

Power-On Reset

Before the controller has sufficient bias to guarantee proper operation, the ISL95712 requires a +5V input supply tied to VDD to exceed the VDD rising Power-On Reset (POR) threshold. Once this threshold is reached or exceeded, the ISL95712 has enough bias to check the state of the SVI inputs once ENABLE is taken high. Hysteresis between the rising and the falling thresholds assure the ISL95712 does not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 7). Note that V_{IN} must be present for the controller to drive the output voltage.



Interval 1 to 2: ISL95712 waits to POR.

Interval 2 to 3: SVC and SVD are externally set to pre-Metal VID code.

Interval 3 to 4: ENABLE locks pre-Metal VID code. Both outputs soft-start to this level.

Interval 4 to 5: PGOOD signal goes HIGH, indicating proper operation.

Interval 5 to 6: PGOOD and PGOOD_NB high is detected and PWROK is taken high. The ISL95712 is prepared for SVI commands.

Interval 6 to 7: SVC and SVD data lines communicate change in VID code.

Interval 7 to 8: ISL95712 responds to VID-ON-THE-FLY code change and issues a VOTF for positive VID changes.

Post 8: Telemetry is clocked out of the ISL95712.

FIGURE 10. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

Start-Up Timing

With VDD above the POR threshold, the controller start-up sequence begins when ENABLE exceeds the logic high threshold. Figure 11 shows the typical soft-start timing of the Core and Northbridge VRs. Once the controller registers ENABLE as a high, the controller checks the state of a few programming pins during the typical 8ms delay prior to beginning soft-starting the Core and Northbridge outputs. The pre-PWROK Metal VID is read from the state of the SVC and SVD pins and programs the DAC, the programming resistors on the COMP, COMP_NB and PROG pins are read to configure switching frequency, slew rate and output offsets. These programming resistors are discussed in subsequent sections. The ISL95712 use a digital soft-start to ramp up the DAC to the Metal VID level programmed. The soft-start slew rate is programmed by the PROG resistor, which is used to set the VID-on-the-fly slew rate as well. See the "VID-on-the-Fly Slew Rate Selection" on page 17 for more details on selecting the PROG resistor. PGOOD is asserted high at the end of the soft-start ramp.

Diode Throttling

During the soft-start ramp-up, the ISL95712 operates in Diode Throttling mode until the output has exceeded 400mV. In Diode Throttling mode, the lower MOSFET is kept OFF so that the MOSFET body diode conducts, similar to a standard buck regulator.

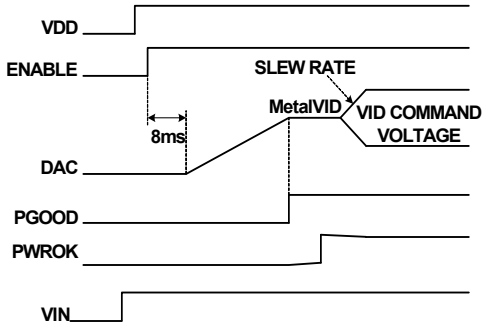


FIGURE 11. TYPICAL SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the soft-start sequence, the ISL95712 regulates the output voltages to the pre-PWROK metal VID programmed, see Table 6 on page 17. The ISL95712 controls the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.55V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

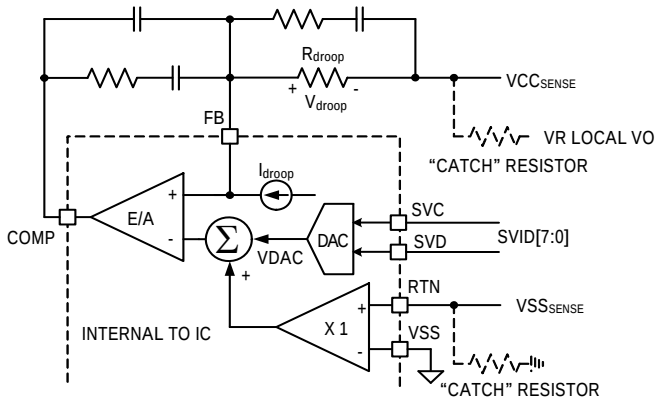


FIGURE 12. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage droops from the VID programmed value by an amount proportional to the load current, to achieve the load line. The ISL95712 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors, as shown in Figures 13 and 14, or through resistors in series with the inductors, as shown in Figure 25 on page 28. In both methods, capacitor C_n voltage represents the total inductor current. An internal amplifier converts C_n voltage into an internal current source, I_{sum}, with the gain set by resistor R_i, see Equation 1.

$$I_{sum} = \frac{V_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

The I_{sum} current is used for load line implementation, current monitoring on the IMON pins and overcurrent protection.

Figure 12 shows the load line implementation. The ISL95712 drives a current source (I_{droop}) out of the FB pin, which is a ratio of the I_{sum} current, as described by Equation 2.

$$I_{droop} = \frac{5}{4} \times I_{sum} = \frac{5}{4} \times \frac{V_{Cn}}{R_i} \quad \text{(EQ. 2)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 3.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 3)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can change the load line slope. Since I_{sum} sets the overcurrent protection level, it is recommended to first scale I_{sum} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 12 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and noninverting input voltages to be equal as shown in Equation 4:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 4)}$$

Rewriting Equation 4 and substituting Equation 3 gives Equation 5 the exact equation required for load line implementation.

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 5)}$$

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback is open circuit in the absence of the processor. As Figure 12 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and to add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω, provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

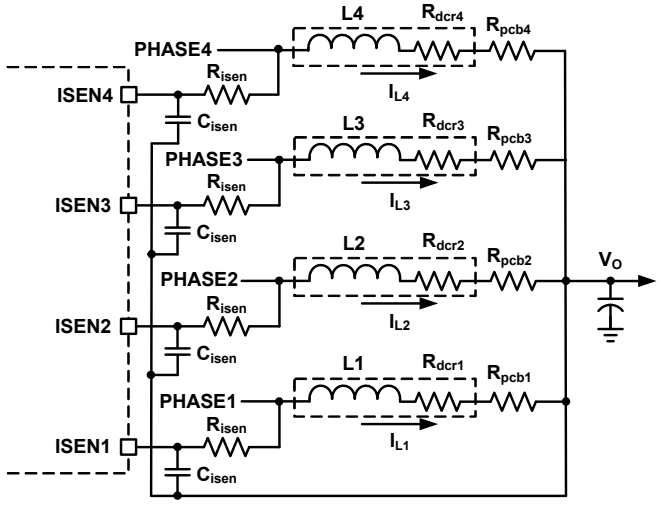


FIGURE 13. CURRENT BALANCING CIRCUIT

The ISL95712 monitors individual phase average current by monitoring the ISEN1, ISEN2, ISEN3 and ISEN4 voltages. Figure 13 shows the recommended current balancing circuit for DCR sensing. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen}, and is presented to the corresponding ISEN pin. R_{isen} should be routed to the inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 6 through 9 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 6)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 7)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 8)}$$

$$V_{ISEN4} = (R_{dcr4} + R_{pcb4}) \times I_{L4} \quad \text{(EQ. 9)}$$

Where R_{dcr1}, R_{dcr2}, R_{dcr3} and R_{dcr4} are inductor DCR; R_{pcb1}, R_{pcb2}, R_{pcb3} and R_{pcb4} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2}, I_{L3} and I_{L4} are inductor average currents.

The ISL95712 will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3} = V_{ISEN4}$, thus to achieve $I_{L1} = I_{L2} = I_{L3} = I_{L4}$, when $R_{dcr1} = R_{dcr2} = R_{dcr3} = R_{dcr4}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3} = R_{pcb4}$.

Using the same components for L1, L2, L3 and L4 provides a good match of R_{dcr1}, R_{dcr2}, R_{dcr3} and R_{dcr4}. Board layout determines R_{pcb1}, R_{pcb2}, R_{pcb3} and R_{pcb4}. It is recommended to have a symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3} = R_{pcb4}$.

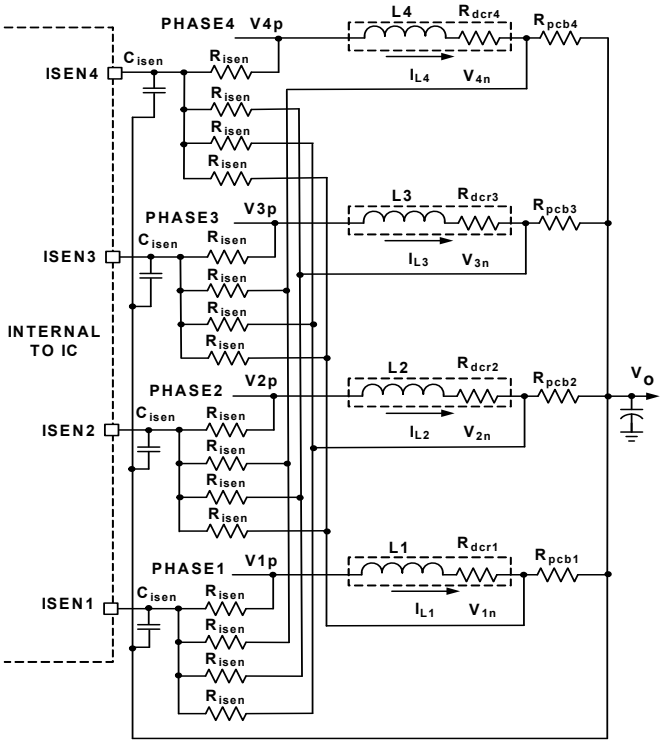


FIGURE 14. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 13, asymmetric layout causes different R_{pcb1}, R_{pcb2}, R_{pcb3} and R_{pcb4} values, thus creating a current imbalance. Figure 14 shows a differential sensing current balancing circuit recommended for ISL95712. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own, phase inductor phase-node pad, and the other two phase inductor output side pads. Equations 10 through 13 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} + V_{4n} \quad \text{(EQ. 10)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} + V_{4n} \quad \text{(EQ. 11)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} + V_{4n} \quad \text{(EQ. 12)}$$

$$V_{ISEN4} = V_{1n} + V_{2n} + V_{3n} + V_{4p} \quad \text{(EQ. 13)}$$

The ISL95712 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3} = V_{ISEN4}$ as shown in Equations 14 and 16:

$$V_{1p} + V_{2n} + V_{3n} + V_{4n} = V_{1n} + V_{2p} + V_{3n} + V_{4n} \quad \text{(EQ. 14)}$$

$$V_{1n} + V_{2p} + V_{3n} + V_{4n} = V_{1n} + V_{2n} + V_{3p} + V_{4n} \quad \text{(EQ. 15)}$$

$$V_{1n} + V_{2n} + V_{3p} + V_{4n} = V_{1n} + V_{2n} + V_{3n} + V_{4p} \quad \text{(EQ. 16)}$$

Rewriting Equation 14 gives Equation 17:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 17)}$$

Rewriting Equation 15 gives Equation 18:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 18)}$$

Rewriting Equation 16 gives Equation 19:

$$V_{3p} - V_{3n} = V_{4p} - V_{4n} \quad \text{(EQ. 19)}$$

Combining Equations 17 through 19 give:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} = V_{4p} - V_{4n} \quad \text{(EQ. 20)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} = R_{dcr4} \times I_{L4} \quad \text{(EQ. 21)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3} = I_{L4}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3} = R_{dcr4}$. R_{pcb1}, R_{pcb2}, R_{pcb3} and R_{pcb4} do not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R3™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 15 shows the current balancing performance of a three-phase evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at a low repetition rate, but cannot keep up when the repetition rate gets into the hundred-kHz range, where it is out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

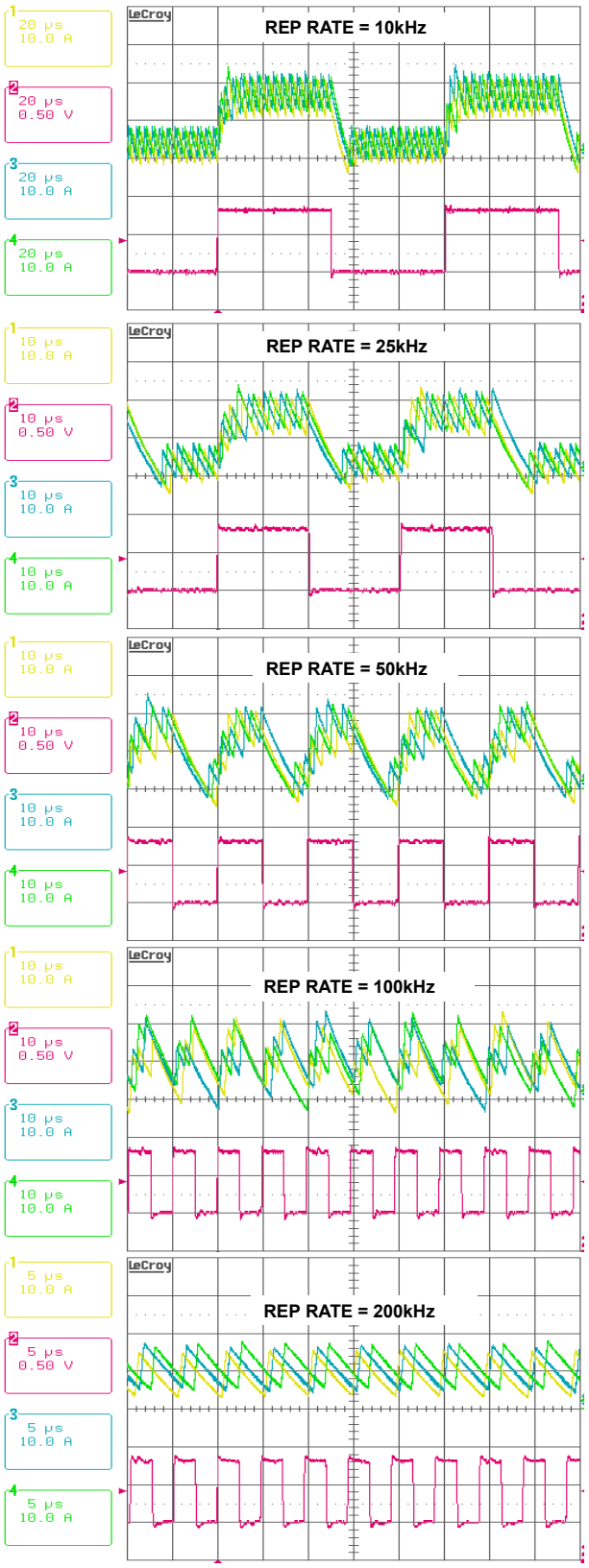


FIGURE 15. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

Modes of Operation

TABLE 1. CORE VR MODES OF OPERATION

CONFIG.	ISEN4	ISEN3	ISEN2	PSI0_L AND PSI1_L	MODE
4-phase Core VR Configuration	To Power Stage	To Power Stage	To Power Stage	11	4-phase CCM
				01	2-phase CCM
				00	1-phase DE
3-phase Core VR Configuration	Tied to 5V	To Power Stage	To Power Stage	11	3-phase CCM
				01	2-phase CCM
				00	1-phase DE
2-phase Core VR Configuration	Tied to 5V	Tied to 5V	To Power Stage	11	2-phase CCM
				01	1-phase CCM
				00	1-phase DE
1-phase Core VR Configuration	Tied to 5V	Tied to 5V	Tied to 5V	11	1-phase CCM
				01	1-phase CCM
				00	1-phase DE

The Core VR can be configured for 4-, 3-, 2- or 1-phase operation. Table 1 shows Core VR configurations and operational modes, programmed by the ISEN4, ISEN3 and ISEN2 pin status and the PSI0_L and PSI1_L commands via the SVI 2 interface. The SVI 2 interface description of these bits is outlined in Table 9.

The ISENx pins disable the channel which they are related to. For example, to setup a 3-phase configuration the ISEN4 pin is tied to 5V. This disables Channel 4 of the controller on the Core side.

In a 3-phase configuration, the Core VR operates in 3-phase CCM, with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR sheds Phase 3. The Core VR then operates 2-phase and remains in CCM. When both PSI0_L and PSI1_L are taken low, the Core VR sheds Phase 2 and the Core VR enters 1-phase Diode Emulation (DE) mode.

For 2-phase configurations, the Core VR operates in 2-phase CCM with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR sheds Phase 2 and the Core VR operates in 1-phase and remains in CCM. When both PSI0_L and PSI1_L are taken low, the Core VR operates in 1-phase DE mode.

In a 1-phase configuration, the Core VR operates in 1-phase CCM and remains in this mode when PSI0_L is taken low. When both PSI0_L and PSI1_L are taken low, the controller enters DE mode.

When the Core VR is taken into PSI1 mode, where both PSI0_L and PSI1_L are taken low, the ISL95712 will shed any additional phases in excess of Phase 1. If there is a VID change as well, the regulator will then slew the output to the new VID level in CCM mode. Once the output has reached the new VID level, the Core VR is then placed into DE mode. The Core VR can be disabled completely by connecting ISEN1 to +5V.

The ISL95712 Northbridge VR can be configured for 3-, 2-, or 1-phase operation. Table 2 shows the Northbridge VR configurations and operational modes, which are programmed by the ISEN3_NB and ISEN2_NB pin status and the PSI0_L and PSI1_L bits of the SVI 2 command.

TABLE 2. NORTHBRIDGE VR MODES OF OPERATION

CONFIG.	ISEN3_NB	ISEN2_NB	PSI0_L AND PSI1_L	MODE
3-phase NB VR Configuration	To Power Stage	To Power Stage	11	2-phase CCM
			01	1-phase CCM
			00	1-phase DE
2-phase NB VR Configuration	Tied to 5V	To Power Stage	11	2-phase CCM
			01	1-phase CCM
			00	1-phase DE
1-phase NB VR Configuration	Tied to 5V	Tied to 5V	11	1-phase CCM
			01	1-phase CCM
			00	1-phase DE

In a 1-phase configuration, the ISEN2_NB pin is tied to +5V. The Northbridge VR operates in 1-phase CCM when both PSI0_L and PSI1_L are high and continues in this mode when PSI0_L is taken low. The controller enters 1-phase DE mode when both PSI0_L and PSI1_L are low.

When the Northbridge VR is taken into PSI1 mode, where both PSI0_L and PSI1_L are taken low, the ISL95712 will shed any additional phases in excess of Phase 1. If there is a VID change as well, the regulator will then slew the output to the new VID level in CCM mode. Once the output has reached the new VID level, the Northbridge VR is then placed into DE mode.

The Northbridge VR can be disabled completely by tying ISEN1_NB to 5V.

Dynamic Operation

Core and Northbridge VRs behave the same during dynamic operation. The controller responds to VID-on-the-fly changes by slewing to the new voltage at the slew rate programmed, see Table 4. During negative VID transitions, the output voltage decays to the lower VID value at the slew rate determined by the load.

The R3™ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET. To minimize the body diode-related loss, the controller also adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns.

Resistor Configuration Options

The ISL95712 uses the COMP, COMP_NB and PROG pins to configure some functionality within the IC. Resistors from these pins to GND are read during the first portion of the soft-start sequence. The following sections outline how to select the resistor values for each of these pins to correctly program the output voltage offset of each output, VID-on-the-fly slew rate and switching frequency used for both VRs.

VR Offset Programming

A positive or negative offset is programmed for the Core VR using a resistor to ground from the COMP pin and the Northbridge in a similar manner from the COMP_NB pin. Table 3 provides the resistor value to select the desired output voltage offset. The 1% tolerance resistor value shown in Table 3 must be used to program the corresponding Core or NB output voltage offset. The MIN and MAX tolerance values provide margin to insure the 1% tolerance resistor will be read correctly.

TABLE 3. COMP AND COMP_NB OUTPUT VOLTAGE OFFSET SELECTION

RESISTOR VALUE [kΩ]			COMP $V_{CORE\ OFFSET}$ [mV]	COMP_NB OFFSET [mV]
MIN TOLERANCE	1% TOLERANCE VALUE	MAX TOLERANCE		
3.96	**4.02**	4.07	-43.75	18.75
7.76	**7.87**	7.98	-37.5	31.25
11.33	**11.5**	11.67	-31.25	43.76
16.65	**16.9**	17.15	-25	50
19.3	**19.6**	19.89	-18.75	37.5
24.53	**24.9**	25.27	-12.5	25
33.49	**34.0**	34.51	-6.25	12.5
40.58	**41.2**	41.81	6.25	0
51.52	**52.3**	53.08	18.75	18.75
72.10	**73.2**	74.29	31.25	31.25
93.87	**95.3**	96.72	43.76	43.76
119.19	**121**	112.81	50	50
151.69	**154**	156.31	37.5	37.5
179.27	**182**	184.73	25	25
206.85	**210**	213.15	12.5	12.5
	OPEN		0	0

TABLE 4. PROG RESISTOR SELECTION

RESISTOR VALUE [kΩ]	SLEW RATE FOR CORE AND NORTHBRIDGE [mV/µs]
4.02	20
7.87	15
11.5	12.5
16.9	10
19.6	20
24.9	15
34.0	12.5
41.2	10
52.3	20
73.2	15
95.3	12.5
121	10
154	20
182	15
210	12.5
OPEN	10

VID-on-the-Fly Slew Rate Selection

The PROG resistor is used to select the slew rate for VID changes commanded by the processor. Once selected, the slew rate is locked in during soft-start and is not adjustable during operation. The lowest slew rate that can be selected is 10mV/µs, which is above the minimum of 7.5mV/µs required by the SVI2 specification. The slew rate selected sets the slew rate for both Core and Northbridge VRs. The controller does not allow for independent selection of slew rate.

CCM Switching Frequency

The Core and Northbridge VR switching frequency is set by the programming resistors on COMP_NB and PROG. When the ISL95712 is in Continuous Conduction Mode (CCM), the switching frequency is not absolutely constant due to the nature of the R3™ modulator. As explained in "Multiphase R3™ Modulator" on page 10, the effective switching frequency increases during load insertion and decreases during load release to achieve fast response. Thus, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 10% and does not have any significant effect on output voltage ripple magnitude. Table 5 defines the switching frequency based on the resistor values used to program the COMP_NB and PROG pins. Use the previous tables related to COMP_NB and PROG to determine the correct resistor value in these ranges to program the desired output offset and slew rate.

TABLE 5. SWITCHING FREQUENCY SELECTION

FREQUENCY [kHz]	COMP_NB RANGE [kΩ]	PROG RANGE [kΩ]
300	57.6 to OPEN	19.1 to 41.2 or 154 to OPEN
350	4.02 to 41.2	19.1 to 41.2 or 154 to OPEN
400	57.6 to OPEN	5.62 to 16.9 or 57.6 to 121
450	4.02 to 41.2	5.62 to 16.9 or 57.6 to 121

The controller monitors SVI commands to determine when to enter power-saving mode, implement dynamic VID changes and shut down individual outputs.

AMD Serial VID Interface 2.0

The on-board Serial VID Interface 2.0 (SVI 2) circuitry allows the AMD processor to directly control the Core and Northbridge voltage reference levels within the ISL95712. Once the PWROK signal goes high, the IC begins monitoring the SVC and SVD pins for instructions. The ISL95712 uses a Digital-to-Analog Converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 10 on page 12 for a simple SVI interface timing diagram.

Pre-PWROK Metal VID

Typical motherboard start-up begins with the controller decoding the SVC and SVD inputs to determine the pre-PWROK Metal VID setting (see Table 6). Once the ENABLE input exceeds the rising threshold, the ISL95712 decodes and locks the decoded value into an on-board hold register.

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Once the programming pins are read, the internal DAC circuitry begins to ramp Core and Northbridge VRs to the decoded pre-PWROK Metal VID output level. The digital soft-start circuitry ramps the internal reference to the target gradually at a fixed rate of approximately 5mV/µs until the output voltage reaches ~250mV and then at the programmed slew rate. The controlled ramp of all output voltage planes reduces inrush current during the soft-start interval. At the end of the soft-start interval, the PGOOD and PGOOD_NB outputs transition high, indicating both output planes are within regulation limits.

If the ENABLE input falls below the enable falling threshold, the ISL95712 tri-states both outputs. PGOOD and PGOOD_NB are pulled low with the loss of ENABLE. The Core and Northbridge VR output voltages decay, based on output capacitance and load

leakage resistance. If bias to VDD falls below the POR level, the The ISL95712 responds in the manner previously described. Once VDD and ENABLE rise above their respective rising thresholds, the internal DAC circuitry reacquires a pre-PWROK metal VID code, and the controller soft-starts.

SVI Interface Active

Once the Core and Northbridge VRs have successfully soft-started and PGOOD and PGOOD_NB signals transition high, PWROK can be asserted externally to the ISL95712. Once PWROK is asserted to the IC, SVI instructions can begin as the controller actively monitors the SVI interface. Details of the SVI Bus protocol are provided in the “AMD Serial VID Interface 2.0 (SVI2) Specification”. See AMD publication #48022.

Once a VID change command is received, the ISL95712 decodes the information to determine which VR is affected and the VID target is determined by the byte combinations in Table 7. The internal DAC circuitry steps the output voltage of the VR commanded to the new VID level. During this time, one or more of the VR outputs could be targeted. In the event either VR is commanded to power-off by serial VID commands, the PGOOD signal remains asserted.

If the PWROK input is deasserted, then the controller steps both the Core and the Northbridge VRs back to the stored pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, then the ISL95712 SVI interface waits for instructions.

If ENABLE goes low during normal operation, all external MOSFETs are tri-stated and both PGOOD and PGOOD_NB are pulled low. This event clears the pre-PWROK metal VID code and forces the controller to check SVC and SVD upon restart, storing the pre-PWROK metal VID code found on restart.

A POR event on VCC during normal operation shuts down both regulators, and both PGOOD outputs are pulled low. The pre-PWROK metal VID code is not retained. Loss of VIN during operation will typically cause the controller to enter a fault condition on one or both outputs as the output voltage collapses. The controller will shut down both Core and Northbridge VRs and latch off. The pre-PWROK metal VID code is not retained during the process of cycling ENABLE to reset the fault latch and restart the controller.

VID-on-the-Fly Transition

Once PWROK is high, the ISL95712 detects this flag and begins monitoring the SVC and SVD pins for SVI instructions. The microprocessor follows the protocol outlined in the following sections to send instructions for VID-on-the-fly transitions. The ISL95712 decodes the instruction and acknowledges the new VID code. For VID codes higher than the current VID level, the ISL95712 begins stepping the commanded VR outputs to the new VID target at the fixed slew rate of 10mV/µs. Once the DAC ramps to the new VID code, a VID-on-the-Fly Complete (VOTFC) request is sent on the SVI lines.

When the VID codes are lower than the current VID level, the ISL95712 checks the state of power state bits in the SVI command. If power state bits are not active, the controller begins stepping the regulator output to the new VID target. If the power state bits are active, the controller allows the output voltage to decay and slowly steps the DAC down with the natural decay of the output. This allows the controller to quickly recover and move to a high VID code if commanded. The controller issues a VOTFC request on the SVI lines once the SVI command is decoded and prior to reaching the final output voltage.

VOTFC requests do not take priority over telemetry per the AMD SVI 2 specification.

SVI Data Communication Protocol

The SVI WIRE protocol is based on the I^2C bus concept. Two wires [serial clock (SVC) and serial data (SVD)], carry information between the AMD processor (master) and VR controller (slave) on the bus. The master initiates and terminates SVI transactions and drives the clock, SVC, during a transaction. The AMD processor is always the master and the voltage regulators are the slaves. The slave receives the SVI transactions and acts accordingly. Mobile SVI WIRE protocol timing is based on high-speed mode I^2C. See AMD publication #48022 for additional details.

TABLE 7. SERIAL VID CODES

SVID[7:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
0000_0000	1.55000	0010_0000	1.35000	0100_0000	1.15000	0110_0000	0.95000
0000_0001	1.54375	0010_0001	1.34375	0100_0001	1.14375	0110_0001	0.94375
0000_0010	1.53750	0010_0010	1.33750	0100_0010	1.13750	0110_0010	0.93750
0000_0011	1.53125	0010_0011	1.33125	0100_0011	1.13125	0110_0011	0.93125
0000_0100	1.52500	0010_0100	1.32500	0100_0100	1.12500	0110_0100	0.92500
0000_0101	1.51875	0010_0101	1.31875	0100_0101	1.11875	0110_0101	0.91875
0000_0110	1.51250	0010_0110	1.31250	0100_0110	1.11250	0110_0110	0.91250
0000_0111	1.50625	0010_0111	1.30625	0100_0111	1.10625	0110_0111	0.90625
0000_1000	1.50000	0010_1000	1.30000	0100_1000	1.10000	0110_1000	0.90000
0000_1001	1.49375	0010_1001	1.29375	0100_1001	1.09375	0110_1001	0.89375
0000_1010	1.48750	0010_1010	1.28750	0100_1010	1.08750	0110_1010	0.88750
0000_1011	1.48125	0010_1011	1.28125	0100_1011	1.08125	0110_1011	0.88125
0000_1100	1.47500	0010_1100	1.27500	0100_1100	1.07500	0110_1100	0.87500
0000_1101	1.46875	0010_1101	1.26875	0100_1101	1.06875	0110_1101	0.86875
0000_1110	1.46250	0010_1110	1.26250	0100_1110	1.06250	0110_1110	0.86250
0000_1111	1.45625	0010_1111	1.25625	0100_1111	1.05625	0110_1111	0.85625
0001_0000	1.45000	0011_0000	1.25000	0101_0000	1.05000	0111_0000	0.85000
0001_0001	1.44375	0011_0001	1.24375	0101_0001	1.04375	0111_0001	0.84375
0001_0010	1.43750	0011_0010	1.23750	0101_0010	1.03750	0111_0010	0.83750
0001_0011	1.43125	0011_0011	1.23125	0101_0011	1.03125	0111_0011	0.83125
0001_0100	1.42500	0011_0100	1.22500	0101_0100	1.02500	0111_0100	0.82500
0001_0101	1.41875	0011_0101	1.21875	0101_0101	1.01875	0111_0101	0.81875
0001_0110	1.41250	0011_0110	1.21250	0101_0110	1.01250	0111_0110	0.81250
0001_0111	1.40625	0011_0111	1.20625	0101_0111	1.00625	0111_0111	0.80625
0001_1000	1.40000	0011_1000	1.20000	0101_1000	1.00000	0111_1000	0.80000
0001_1001	1.39375	0011_1001	1.19375	0101_1001	0.99375	0111_1001	0.79375
0001_1010	1.38750	0011_1010	1.18750	0101_1010	0.98750	0111_1010	0.78750
0001_1011	1.38125	0011_1011	1.18125	0101_1011	0.98125	0111_1011	0.78125
0001_1100	1.37500	0011_1100	1.17500	0101_1100	0.97500	0111_1100	0.77500
0001_1101	1.36875	0011_1101	1.16875	0101_1101	0.96875	0111_1101	0.76875
0001_1110	1.36250	0011_1110	1.16250	0101_1110	0.96250	0111_1110	0.76250
0001_1111	1.35625	0011_1111	1.15625	0101_1111	0.95625	0111_1111	0.75625
1000_0000	0.75000	1010_0000	0.55000*	1100_0000	0.35000*	1110_0000	0.15000*
1000_0001	0.74375	1010_0001	0.54375*	1100_0001	0.34375*	1110_0001	0.14375*
1000_0010	0.73750	1010_0010	0.53750*	1100_0010	0.33750*	1110_0010	0.13750*
1000_0011	0.73125	1010_0011	0.53125*	1100_0011	0.33125*	1110_0011	0.13125*
1000_0100	0.72500	1010_0100	0.52500*	1100_0100	0.32500*	1110_0100	0.12500*
1000_0101	0.71875	1010_0101	0.51875*	1100_0101	0.31875*	1110_0101	0.11875*
1000_0110	0.71250	1010_0110	0.51250*	1100_0110	0.31250*	1110_0110	0.11250*
1000_0111	0.70625	1010_0111	0.50625*	1100_0111	0.30625*	1110_0111	0.10625*

TABLE 7. SERIAL VID CODES (Continued)

SVID[7:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
1000_1000	0.70000	1010_1000	0.50000*	1100_1000	0.30000*	1110_1000	0.10000*
1000_1001	0.69375	1010_1001	0.49375*	1100_1001	0.29375*	1110_1001	0.09375*
1000_1010	0.68750	1010_1010	0.48750*	1100_1010	0.28750*	1110_1010	0.08750*
1000_1011	0.68125	1010_1011	0.48125*	1100_1011	0.28125*	1110_1011	0.08125*
1000_1100	0.67500	1010_1100	0.47500*	1100_1100	0.27500*	1110_1100	0.07500*
1000_1101	0.66875	1010_1101	0.46875*	1100_1101	0.26875*	1110_1101	0.06875*
1000_1110	0.66250	1010_1110	0.46250*	1100_1110	0.26250*	1110_1110	0.06250*
1000_1111	0.65625	1010_1111	0.45625*	1100_1111	0.25625*	1110_1111	0.05625*
1001_0000	0.65000	1011_0000	0.45000*	1101_0000	0.25000*	1111_0000	0.05000*
1001_0001	0.64375	1011_0001	0.44375*	1101_0001	0.24375*	1111_0001	0.04375*
1001_0010	0.63750	1011_0010	0.43750*	1101_0010	0.23750*	1111_0010	0.03750*
1001_0011	0.63125	1011_0011	0.43125*	1101_0011	0.23125*	1111_0011	0.03125*
1001_0100	0.62500	1011_0100	0.42500*	1101_0100	0.22500*	1111_0100	0.02500*
1001_0101	0.61875	1011_0101	0.41875*	1101_0101	0.21875*	1111_0101	0.01875*
1001_0110	0.61250	1011_0110	0.41250*	1101_0110	0.21250*	1111_0110	0.01250*
1001_0111	0.60625	1011_0111	0.40625*	1101_0111*	0.20625*	1111_0111	0.00625*
1001_1000	0.60000*	1011_1000	0.40000*	1101_1000	0.20000*	1111_1000	OFF*
1001_1001	0.59375*	1011_1001	0.39375*	1101_1001	0.19375*	1111_1001	OFF*
1001_1010	0.58750*	1011_1010	0.38750*	1101_1010	0.18750*	1111_1010	OFF*
1001_1011	0.58125*	1011_1011	0.38125*	1101_1011	0.18125*	1111_1011	OFF*
1001_1100	0.57500*	1011_1100	0.37500*	1101_1100	0.17500*	1111_1100	OFF*
1001_1101	0.56875*	1011_1101	0.36875*	1101_1101	0.16875*	1111_1101	OFF*
1001_1110	0.56250*	1011_1110	0.36250*	1101_1110	0.16250*	1111_1110	OFF*
1001_1111	0.55625*	1011_1111	0.35625*	1101_1111	0.15625*	1111_1111	OFF*

NOTE: * Indicates a VID not required for AMD Family 10h processors. Loosened AMD requirements at these levels.

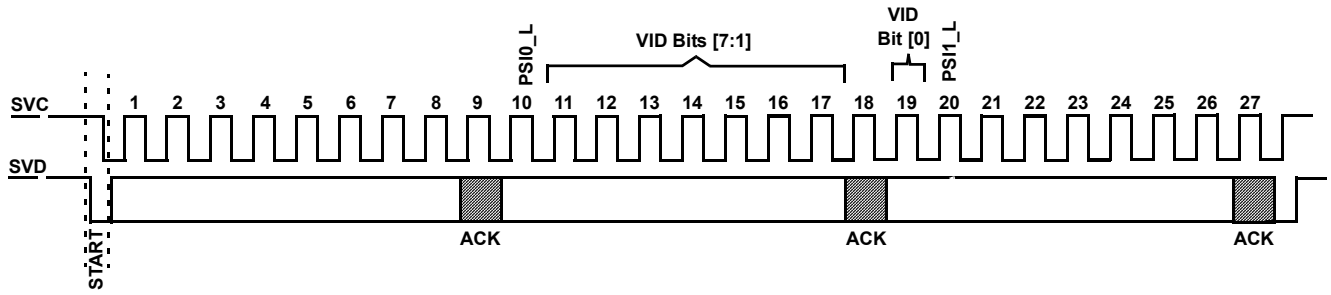


FIGURE 16. SVD PACKET STRUCTURE

SVI Bus Protocol

The AMD processor bus protocol is similar to SMBus send byte protocol for VID transactions. The AMD SVD packet structure is shown in Figure 16. The description of each bit of the three bytes that make up the SVI command are shown in Table 8. During a transaction, the processor sends the start sequence followed by each of the three bytes, which end with an optional acknowledge bit. The ISL95712 does not drive the SVD line during the ACK bit. Finally, the processor sends the stop sequence. After the ISL95712 has detected the stop, it can then proceed with the commanded action from the transaction.

TABLE 8. SVD DATA PACKET

BITS	DESCRIPTION
1:5	Always 11000b
6	Core domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Core VR.
7	Northbridge domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Northbridge VR.
8	Always 0b
9	Acknowledge bit
10	PSI0_L
11:17	VID code bits [7:1]
18	Acknowledge bit
19	VID code bit [0]
20	PSI1_L
21	TFN (Telemetry Functionality)
22:24	Load line slope trim
25:26	Offset Trim [1:0]
27	Acknowledge bit

Power States

SVI2 defines two power state indicator levels, see Tables 1, 2, and 9. As processor current consumption is reduced, the power state indicator level changes to improve VR efficiency under low power conditions.

For the Core VR operating in 4-phase mode (when PSI0_L is asserted) Channels 3 and 4 are tri-stated. The controller continues to operate in 2-phase CCM. The shedding of phases improves the efficiency of the VR at the light to moderate load levels of the CPU in this power state. When PSI1_L is asserted the Core VR sheds Channel 2. If there is a corresponding VID change, then the output is moved to the new VID level while in single phase DE mode. Once the output is at the proper VID level, Channel 1 enters diode emulation mode to further boost light-load efficiency in this power state.

For the Northbridge VR operating in 3-phase mode, when PSI0_L is asserted, Channels 2 and 3 are tri-stated while Channel 1 continues in continuous conduction mode. When PSI1_L is asserted, the output is moved to the new VID level if one is commanded and Channel 1 then enters diode emulation mode to conserve power.

It is possible for the processor to assert or deassert PSI0_L and PSI1_L out of order. PSI0_L takes priority over PSI1_L. If PSI0_L is deasserted while PSI1_L is still asserted, the ISL95712 will return the selected VR back full channel CCM operation. For example, if the Core VR is configured for 4-Phase operation and both PSI0_L and PSI1_L are asserted low during a command, the VR will shed three phases and operate in 1-Phase DE mode. If an SVI command follows which takes PSI0_L high, but leaves PSI1_L low, the VR will exit power savings mode and being operation in 4-Phase CCM mode.

TABLE 9. PSI0_L AND PSI1_L DEFINITION

FUNCTION	BIT	DESCRIPTION
PSI0_L	10	Power State Indicate level 0. When this signal is asserted (active Low), the processor is in a low enough power state for the ISL95712 to take action to boost efficiency by dropping phases.
PSI1_L	20	Power State Indicate level 1. When this signal is asserted (active Low), the processor is in a low enough power state for the ISL95712 to take action to boost efficiency by dropping phases and entering 1-Phase DE.

Dynamic Load Line Slope Trim

The ISL95712 supports the SVI2 ability for the processor to manipulate the load line slope of the Core and Northbridge VRs independently using the serial VID interface. The slope manipulation applies to the initial load line slope. A load line slope trim will typically coincide with a VOTF change. See Table 10 for more information about the load line slope trim feature of the ISL95712. The Disable LL selection is not recommended unless operation without a LL is required and considered during the compensation of the VR.

TABLE 10. LOAD LINE SLOPE TRIM DEFINITION

LOAD LINE SLOPE TRIM [2:0]	DESCRIPTION
000	Disable LL
001	-40% mΩ Change
010	-20% mΩ Change
011	No Change
100	+20% mΩ Change
101	+40% mΩ Change
110	+60% mΩ Change
111	+80% mΩ Change

Dynamic Offset Trim

The ISL95712 supports the SVI2 ability for the processor to manipulate the output voltage offset of the Core and Northbridge VRs. This offset is in addition to any output voltage offset set via the COMP resistor reader. The dynamic offset trim can disable the COMP resistor programmed offset of either output when Disable All Offset is selected.

TABLE 11. OFFSET TRIM DEFINITION

OFFSET TRIM [1:0]	DESCRIPTION
00	Disable All Offset
01	-25mV Change
10	0mV Change
11	+25mV Change

Telemetry

The ISL95712 can provide voltage and current information to the AMD CPU through the telemetry system outlined by the AMD SVI2 specification. The telemetry data is transmitted through the SVC and SVT lines of the SVI2 interface.

Current telemetry is based on a voltage generated across a 133kΩ resistor placed from the IMON pin to GND. The current flowing out of the IMON pin is proportional to the load current in the VR. The I_{sum} current defined in "Voltage Regulation and Load Line Implementation" on page 12, provides the base conversion from the load current to the internal amplifier created I_{sum} current. The I_{sum} current is then divided down by a factor of 4 to create the IMON current, which flows out of the IMON pin. The I_{sum} current will measure 36µA when the load current is at full load based on a droop current designed for 45µA at the same load current. The difference between the I_{sum} current and the droop current is provided in Equation 2. The IMON current will measure 11.25µA at full load current for the VR and the IMON voltage will be 1.2V. The load percentage, which is reported by the IC is based on the this voltage. When the load is 25% of the full load, the voltage on the IMON pin will be 25% of 1.2V or 0.3V.

The SVI interface allows the selection of no telemetry, voltage only, or voltage and current telemetry on either or both of the VR outputs. The TFN bit along with the Core and Northbridge domain selector bits are used by the processor to change the functionality of telemetry, see Table 12 for more information.

TABLE 12. TFN TRUTH TABLE

TFN, CORE, NB BITS [21, 6, 7]	DESCRIPTION
1,0,1	Telemetry is in voltage and current mode. Therefore, voltage and current are sent for VDD and VDDNB domains by the controller.
1,0,0	Telemetry is in voltage mode only. Only the voltage of VDD and VDDNB domains is sent by the controller.
1,1,0	Telemetry is disabled.
1,1,1	Reserved

PMBus Interface

The ISL95712 includes a PMBus interface, which allows for user programmability of numerous operating parameters and for monitoring various parameters of the Core and NB regulators. The PMBus address for the ISL95712 is 1001111.

TABLE 13. PMBus READ AND WRITE REGISTERS

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION		
9Bh	R	01h	MANUFACTURER REVISION	Silicon revision starts at 01h		
D0h	Reserved					
D1h	Reserved					
D2h	R/W	00h	FAULT_STATUS_2	BIT	BIT VALUE	
					0	1
				5 (Read Only)	ISL95712 Enabled	ISL95712 Fault Disabled
				4	No Fault	Core OV
				3		NB OV
				2		Core OCP
				1		NB OCP
				0		CML. Indicates that an unsupported command is received or a write command to a read-only register or PEC does not match
D3h	R	xxh	READ_VOUT_CORE	Read the Core Voltage in ADC format. Each LSB is 6.25mV		
D4h	R	xxh	READ_IOUT_CORE	Read Core Current in ADC format. FFh = 100% (7.5µA on IMON)		
D5h	Reserved					
D6h	R	xxh	READ_VOUT_NB	Read the NB voltage in ADC format. Each LSB is 6.25mV		
D7h	R	xxh	READ_IOUT_NB	Read NB load current in ADC format. FFh = 100% (7.5µA on IMON)		
D8h	Reserved					
D9h	Reserved					
DAh	Reserved					
DBh	Reserved					
DCh	Reserved					
DDh	Reserved					
DEh	R/W	00h	LOCK_SVID	BIT[0] VALUE	FUNCTIONALITY	
				0	Execute SVI2 Commands. PMBus commands DFh through E4h are not executed. These registers can still be read and written to.	
				1	Execute PMBus commands DFh through E4h while ignoring SVI2 commands.	
DFh	R/W	08h	SET_VID_CORE	Set Core VID, default set to 800mV. Each LSB is 6.25mV. Metal VID level is determined by SVC/SVD logic levels at power-up.		
E0h	R/W	00h	OFFSET_CORE	Set Core offset. The offset range is from -250mV to +200mV. This is a 2's complement number. Bit[7] is the sign bit.		

TABLE 13. PMBus READ AND WRITE REGISTERS (Continued)

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION	
E1h	R/W	0fh	LOADLINE_PWRSTATE_CORE	BIT	FUNCTIONALITY
				[4:2]	Load line slope trim. Refer to Table 10 for proper usage.
				1	Sets PSI0 power state. Refer to Table 9 for proper usage.
				0	Sets PSI1 power state. Refer to Table 9 for proper usage.
E2h	R/W	08h	SET_VID_NB	Set NB VID, default set to 800mV. Each LSB is 6.25mV. Metal VID level is determined by SVC/SVD logic levels at power-up.	
E3h	R/W	00h	OFFSET_NB	Set NB offset. The offset range is from -250mV to +200mV. This is a 2's complement number. Bit[7] is the sign bit.	
E4h	R/W	0fh	LOADLINE_PWRSTATE_NB	BIT	FUNCTIONALITY
				[4:2]	Load line slope trim. Refer to Table 10 for proper usage.
				1	Sets PSI0 power state. Refer to Table 9 for proper usage.
				0	Sets PSI1 power state. Refer to Table 9 for proper usage.

Protection Features

Core VR and Northbridge VR both provide overcurrent, current-balance, undervoltage and overvoltage fault protections. The controller also provides over-temperature protection. The following discussion is based on Core VR and also applies to the Northbridge VR.

Overcurrent

The IMON voltage provides a means of determining the load current at any moment in time. The Overcurrent Protection (OCP) circuitry monitors the IMON voltage to determine when a fault occurs. Based on the previous description in "Voltage Regulation and Load Line Implementation" on page 12, the current which flows out of the IMON pin is proportional to the I_{sum} current. The I_{sum} current is created from the sensed voltage across C_n, which is a measure of the load current based upon the sensing element selected. The IMON current is generated internally and is 1/4 of the I_{sum} current. The EDC or IDDspike current value for the AMD CPU load is used to set the maximum current level for droop and the IMON voltage of 1.2V, which indicates 100% loading for telemetry. The I_{sum} current level at maximum load, or IDDspike, is 36µA and this translates to an IMON current level of 9µA. The IMON resistor is 133kΩ and the 9µA flowing through the IMON resistor results in a 1.2V level at maximum loading of the VR.

The overcurrent threshold is 1.5V on the IMON pin. Based on a 1.2V IMON voltage equating to 100% loading, the additional 0.3V provided above this level equates to a 25% increase in load current before an OCP fault is detected. The EDC or IDDspike current is used to set the 1.2V on IMON for full load current. Thus the OCP level is 1.25 times the EDC or IDDspike current level. This additional margin above the EDC or IDDspike current allows the AMD CPU to enter and exit the IDDspike performance mode without issue unless the load current is out of line with the IDDspike expectation, thus the need for overcurrent protection.

When the voltage on the IMON pin meets the overcurrent threshold of 1.5V, this triggers an OCP event. Within 2µs of detecting an OCP event, the controller asserts VR_HOT_L low to communicate to the AMD CPU to throttle back. A fault timer begins counting while IMON is at or above the 1.5V threshold. The fault timer lasts 7.5µs to 11µs and then the controller takes action by tri-stating the active channels. This provides the CPU time to recover and reduce the load current. If the OCP conditions are relieved, then the fault timer is cleared and VR_HOT_L is taken high clearing the fault condition. If the load current is not reduced and the OCP condition is maintained, the output voltage will fall below the undervoltage threshold due to the lack of switching or a way-overcurrent fault could occur. Either of these fault conditions will cause the controller to drop PGOOD of that output. When PGOOD is taken low, a fault flag from this VR is sent to the other VR and it is shut down within 10µs and PGOOD of the other output is taken low.

The ISL95712 also features a Way-Overcurrent [WOC] feature, which immediately takes the controller into shutdown. This protection is also referred to as fast overcurrent protection for short-circuit protection. If the IMON current reaches 15µA, WOC is triggered. Active channels are tri-stated and the controller is placed in shutdown and PGOOD is pulled low. There is no fault timer on the WOC fault, the controller takes immediate action. The other controller output is also shut down within 10µs.

Current-Balance

The controller monitors the ISENx pin voltages to determine current-balance protection. If the ISENx pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

Undervoltage

If the VSEN voltage falls below the output voltage VID value plus any programmed offsets by -325mV, the controller declares an undervoltage fault. The controller deasserts PGOOD and tri-states the power MOSFETs.

Overvoltage

If the VSEN voltage exceeds the output voltage VID value plus any programmed offsets by +325mV, the controller declares an overvoltage fault. The controller deasserts PGOOD and turns on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value. Once the output voltage is below this level, the lower gate is tri-stated. If the output voltage rises above the overvoltage threshold again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

Thermal Monitor [NTC, NTC_NB]

The ISL95712 features two thermal monitors using an external resistor network, which includes an NTC thermistor to monitor motherboard temperature and alert the AMD CPU of a thermal issue. Figure 17 shows the basic thermal monitor circuit on the Core VR NTC pin. The Northbridge VR features the same thermal monitor. The controller drives a 30µA current out of the NTC pin and monitors the voltage at the pin. The current flowing out of the NTC pin creates a voltage that is compared to a warning threshold of 640mV. When the voltage at the NTC pin falls to this warning threshold or below, the controller asserts VR_HOT_L to alert the AMD CPU to throttle back load current to stabilize the motherboard temperature. A thermal fault counter begins counting toward a minimum shutdown time of 100µs. The thermal fault counter is an up/down counter, so if the voltage at the NTC pin rises above the warning threshold, it will count down and extend the time for a thermal fault to occur. The warning threshold does have 20mV of hysteresis.

If the voltage at the NTC pin continues to fall down to the shutdown threshold of 580mV or below, the controller goes into shutdown and triggers a thermal fault. The PGOOD pin is pulled low and tri-states the power MOSFETs. A fault on either side will shutdown both VRs.

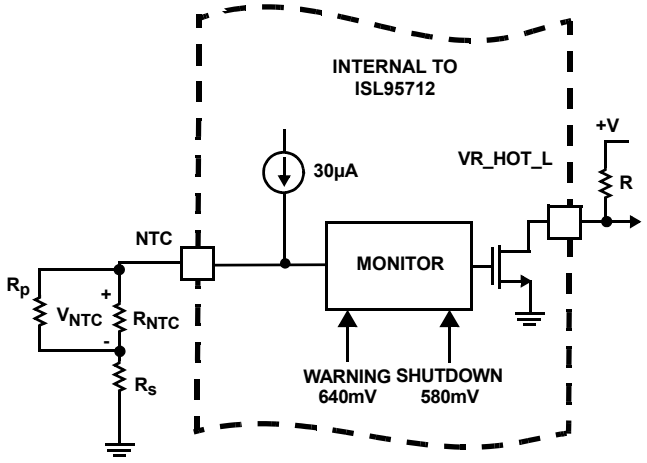


FIGURE 17. CIRCUITRY ASSOCIATED WITH THE THERMAL MONITOR FEATURE OF THE ISL95712

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the over-temperature trip threshold, then VR_HOT is pulled low. The VR_HOT signal is used to change the CPU operation and decrease power consumption. With the reduction in power consumption by the CPU, the board temperature decreases and the NTC thermistor voltage rises. Once the over-temperature threshold is tripped and VR_HOT is taken low, the over-temperature threshold changes to the reset level. The addition of hysteresis to the over-temperature threshold prevents nuisance trips. Once both pin voltages exceed the over-temperature reset threshold, the pull-down on VR_HOT is released. The signal changes state and the CPU resumes normal operation. The over-temperature threshold returns to the trip level.

Table 14 summarizes the fault protections.

TABLE 14. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	7.5µs to 11.5µs	PWM tri-state	ENABLE toggle or VDD toggle
Phase Current Unbalance	1ms	PWM tri-state, PGOOD latched low	
Way-Overcurrent (1.5xOC)	Immediately		
Undervoltage -325mV		PGOOD latched low. PWM tri-state.	
Overvoltage +325mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	
NTC Thermal	100µs min	PGOOD latched low. PWM tri-state.	

Fault Recovery

All of the previously described fault conditions can be reset by bringing ENABLE low or by bringing VDD below the POR threshold. When ENABLE and VDD return to their high operating levels, the controller resets the faults and soft-start occurs.

Interface Pin Protection

The SVC and SVD pins feature protection diodes, which must be considered when removing power to VDD and VDDIO, but leaving it applied to these pins. Figure 18 shows the basic protection on the pins. If SVC and/or SVD are powered but VDD is not, leakage current will flow from these pins to VDD.

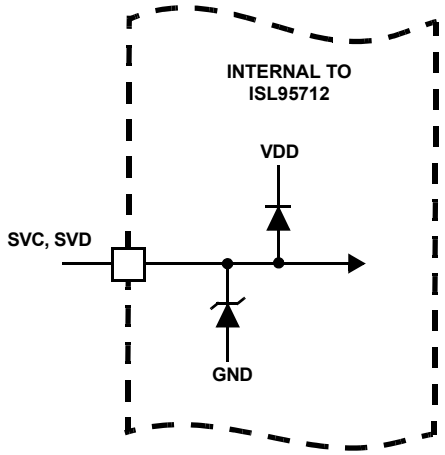


FIGURE 18. PROTECTION DEVICES ON THE SVC AND SVD PINS

Key Component Selection

Inductor DCR Current-Sensing Network

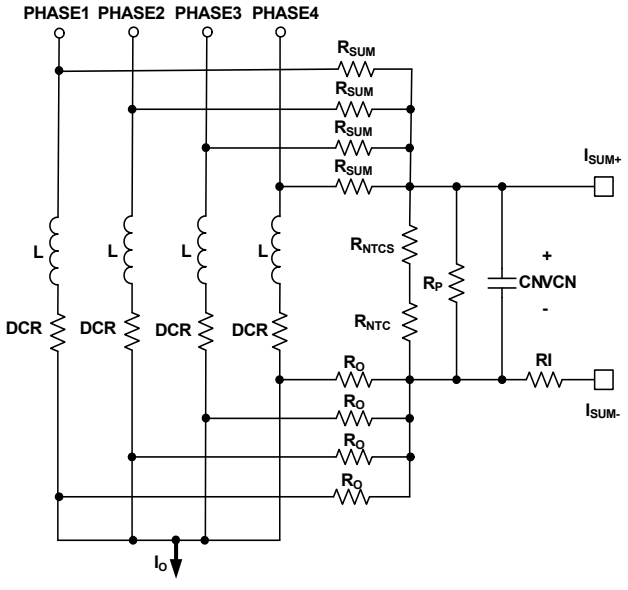


FIGURE 19. DCR CURRENT-SENSING NETWORK

Figure 19 shows the inductor DCR current-sensing network for a 4-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis ignores it.

The summed inductor current information is presented to the capacitor C_n. Equations 22 through 26 describe the frequency domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 22)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 23)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 24)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 25)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 26)}$$

Where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} value decrease as its temperature decreases. Proper selection of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensures that V_{Cn} represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage so the droop circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full

load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole ω_{sns} and a zero w_L. One needs to match ω_L and ω_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing ω_L equal to ω_{sns} and solving for the solution, Equation 27 gives C_n value.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 27)}$$

For example, given N = 4, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ and L = 0.36µH, Equation 27 gives C_n = 0.518µF.

Assuming the compensator design is correct, Figure 20 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ does not accurately represent real-time $I_o(s)$ and worsens the transient response. Figure 21 shows the load transient response when C_n is too small. V_{core} sags excessively upon load insertion and may create a system failure. Figure 22 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There is excessive overshoot if load insertion occurs during this time, which may negatively affect the CPU reliability.

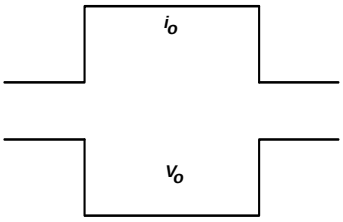


FIGURE 20. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

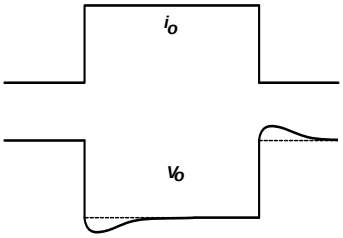


FIGURE 21. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

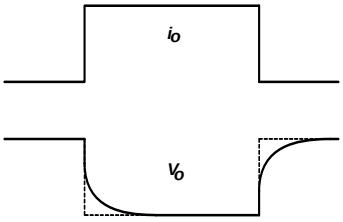


FIGURE 22. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

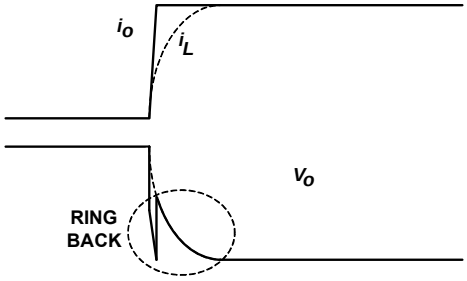


FIGURE 23. OUTPUT VOLTAGE RING-BACK PROBLEM

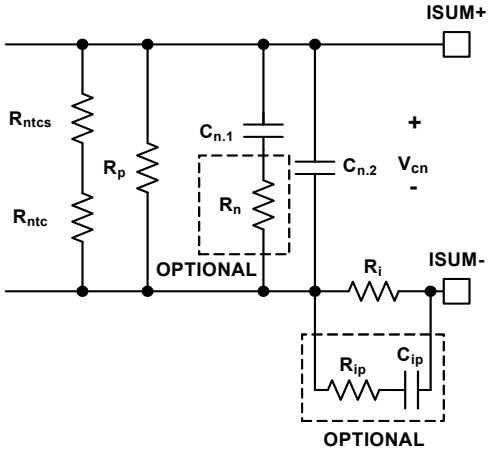


FIGURE 24. OPTIONAL CIRCUITS FOR RING-BACK REDUCTION

Figure 23 shows the output voltage ring-back problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first-order system fashion due to the nature of the current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore, it pulls V_o back to the level dictated by i_L, causing the ring-back problem. This phenomenon is not observed when the output capacitor has very low ESR and ESL, as is the case with all ceramic capacitors.

Figure 24 shows two optional circuits for reduction of the ring-back. C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 24 shows that two capacitors ($C_{n.1}$ and $C_{n.2}$) are in parallel. Resistor R_n is an optional component to reduce the V_o ring-back. At steady state, $C_{n.1}$ + $C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o

change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 21 shows, V_o tends to dip when C_n is too small, and this effect reduces the V_o ring-back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L, and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip} - C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

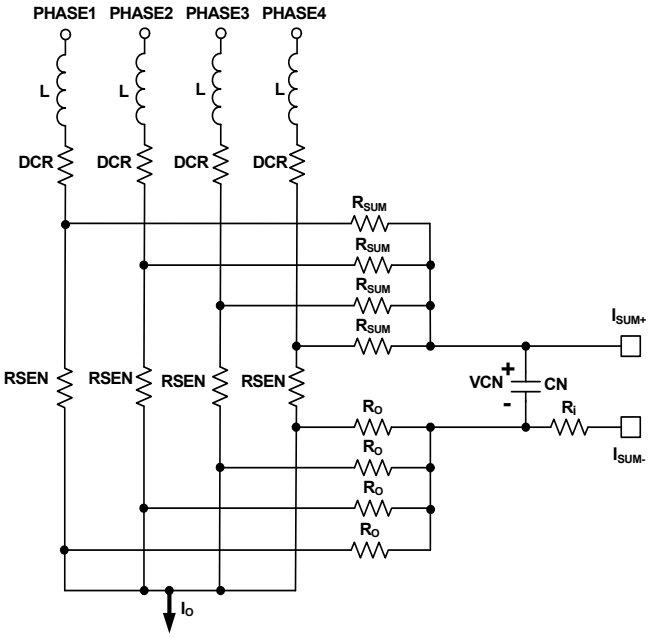


FIGURE 25. RESISTOR CURRENT-SENSING NETWORK

Figure 25 shows the resistor current-sensing network for a 4-phase solution. Each inductor has a series current sensing resistor, R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 28 through 30 give the $V_{Cn}(s)$ expression.

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 28)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 29)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 30)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value does not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 2 on page 13 and Figures 19 and 25; resistor R_i sets the I_{sum} current, which is proportional to droop current and IMON current. The OCP threshold is 1.5V on the IMON pin, which equates to an IMON current of 11.25µA using a 133kΩ IMON resistor. The corresponding I_{sum} is 45µA, which results in an I_{droop} of 56.25µA. At full load current, I_{omax}, the I_{sum} current is 36µA and the resulting I_{droop} is 45µA. The ratio of I_{sum} at OCP relative to full load current is 1.25. Therefore, the OCP current trip level is 25% higher than the full load current.

For inductor DCR sensing, Equation 31 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$:

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 31)}$$

Substitution of Equation 31 into Equation 2 gives Equation 32:

$$I_{droop} = \frac{5}{4} \times \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 32)}$$

Therefore:

$$R_i = \frac{5}{4} \times \frac{R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 33)}$$

Substitution of Equation 23 and application of the OCP condition in Equation 33 gives Equation 34:

$$R_i = \frac{5}{4} \times \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 34)}$$

Where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 4, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, I_{omax} = 100A and $I_{droopmax}$ = 45µA. Equation 34 gives R_i = 529Ω.

For resistor sensing, Equation 35 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 35)}$$

Substitution of Equation 35 into Equation 2 gives Equation 36:

$$I_{droop} = \frac{5}{4} \times \frac{1}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 36)}$$

Therefore:

$$R_i = \frac{5}{4} \times \frac{R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 37)}$$

Substitution of Equation 37 and application of the OCP condition in Equation 33 gives Equation 38:

$$R_i = \frac{5}{4} \times \frac{R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 38)}$$

Where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 4, R_{sen} = 1mΩ, I_{omax} = 100A and $I_{droopmax}$ = 45µA, Equation 38 gives R_i = 694Ω.

Load Line Slope

See Figure 12 for load line implementation.

For inductor DCR sensing, substitution of Equation 32 into Equation 3 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{5}{4} \times \frac{R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 39)}$$

For resistor sensing, substitution of Equation 36 into Equation 3 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{5}{4} \times \frac{R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 40)}$$

Substitution of Equation 33 and rewriting Equation 39, or substitution of Equation 37 and rewriting Equation 40, gives the same result as in Equation 41:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 41)}$$

One can use the full-load condition to calculate R_{droop}. For example, given I_{omax} = 100A, $I_{droopmax}$ = 45µA and LL = 2.1mΩ, Equation 41 gives R_{droop} = 4.67kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 41 and fine-tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 20 shows the desired load transient response waveforms. Figure 26 shows the equivalent circuit of a Voltage Regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e., a constant output impedance, then in the entire frequency range, V_o will have a square response when I_o has a square change.

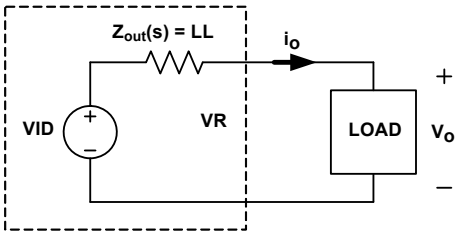


FIGURE 26. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network so that VR achieves constant output impedance as a stable system.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 27 conceptually shows T1(s) measurement set-up, and Figure 28 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, adds it on top of the sensed output voltage, and then feeds it to the compensator. T1 is measured after the summing node, and T2 is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can actually be measured on an ISL95712 regulator.

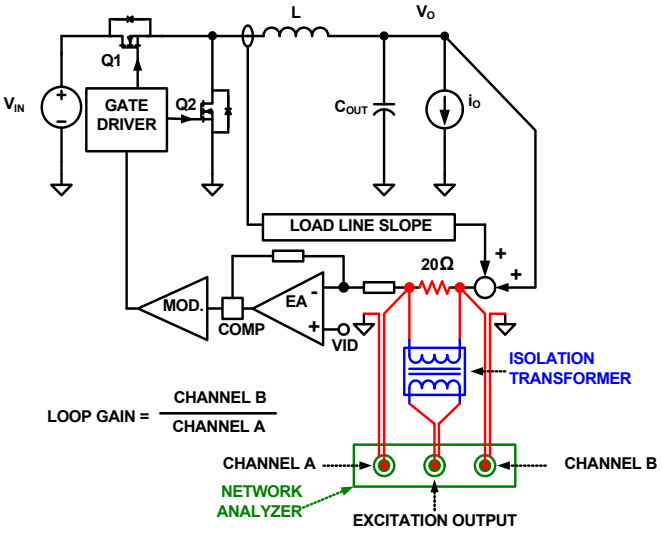


FIGURE 27. LOOP GAIN T1(s) MEASUREMENT SET-UP

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s), therefore has a higher impact on system stability.

T2(s) is the voltage loop gain with closed droop loop, thus having a higher impact on output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin and an output impedance equal to or smaller than the load line slope.

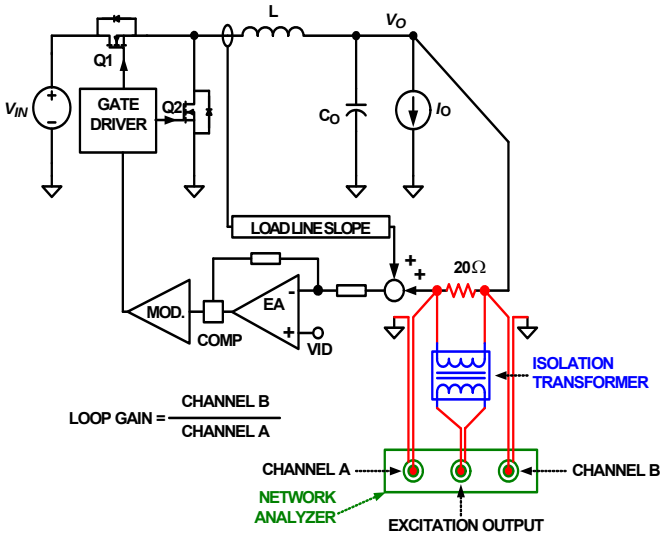


FIGURE 28. LOOP GAIN T2(s) MEASUREMENT SET-UP

Current Balancing

Refer to Figures 13 through 19 for information on current balancing. The ISL95712 achieves current balancing through matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. It is recommended to use a rather long $R_{isen}C_{isen}$ time constant, such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_S = 10kΩ and C_S = 0.22µF.

Thermal Monitor Component Selection

The ISL95712 features two pins, NTC and NTC_NB, which are used to monitor motherboard temperature and alert the AMD CPU if a thermal issues arises. The basic function of this circuitry is outlined in the "Thermal Monitor [NTC, NTC_NB]" on page 25. Figure 29 shows the basic configuration of the NTC resistor, R_{NTC}, and offset resistor, R_S, used to generate the warning and shutdown voltages at the NTC pin.

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the thermal warning threshold of 0.640V, then VR_HOT_L is pulled low. When the AMD CPU detects VR_HOT_L has gone low, it will begin throttling back load current on both outputs to reduce the board temperature.

If the board temperature continues to rise, the NTC thermistor resistance will drop further and the voltage at the NTC pin could drop below the thermal shutdown threshold of 0.580V. Once this threshold is reached, the ISL95712 shuts down both Core and Northbridge VRs indicating a thermal fault has occurred prior to the thermal fault counter triggering a fault.

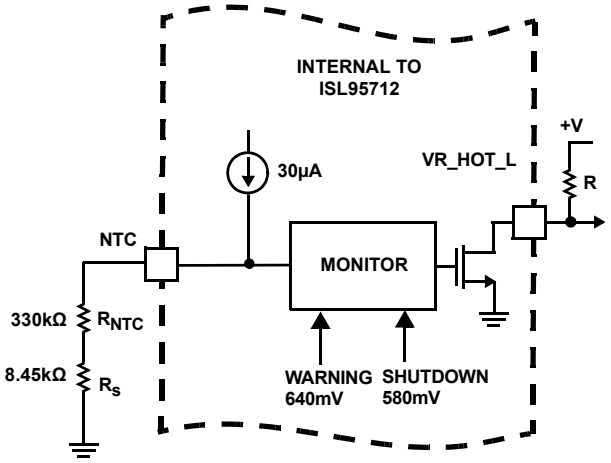


FIGURE 29. THERMAL MONITOR FEATURE OF THE ISL95712

Selection of the NTC thermistor can vary depending on how the resistor network is configured. The equivalent resistance at the typical thermal warning threshold voltage of 0.64V is defined in Equation 42.

$$\frac{0.64\text{V}}{30\mu\text{A}} = 21.3\text{k}\Omega \quad \text{(EQ. 42)}$$

The equivalent resistance at the typical thermal shutdown threshold voltage of 0.58V required to shutdown both outputs is defined in Equation 43.

$$\frac{0.58\text{V}}{30\mu\text{A}} = 19.3\text{k}\Omega \quad \text{(EQ. 43)}$$

The NTC thermistor value correlates to the resistance change between the warning and shutdown thresholds and the required temperature change. If the warning level is designed to occur at a board temperature of +100°C and the thermal shutdown level at a board temperature of +105°C, then the resistance change of the thermistor can be calculated. For example, a Panasonic NTC thermistor with B = 4700 has a resistance ratio of 0.03939 of its nominal value at +100°C and 0.03308 of its nominal value at +105°C. Taking the required resistance change between the thermal warning threshold and the shutdown threshold and dividing it by the change in resistance ratio of the NTC thermistor at the two temperatures of interest, the required resistance of the NTC is defined in Equation 44.

$$\frac{(21.3\text{k}\Omega - 19.3\text{k}\Omega)}{(0.03939 - 0.03308)} = 317\text{k}\Omega \quad \text{(EQ. 44)}$$

The closest standard thermistor to the value calculated with B = 4700 is 330kΩ. The NTC thermistor part number is ERTJ0EV334J. The actual resistance change of this standard thermistor value between the warning threshold and the shutdown threshold is calculated in Equation 45.

$$(330\text{k}\Omega \cdot 0.03939) - (330\text{k}\Omega \cdot 0.03308) = 2.082\text{k}\Omega \quad \text{(EQ. 45)}$$

Since the NTC thermistor resistance at +105°C is less than the required resistance from Equation 43, additional resistance in series with the thermistor is required to make up the difference. A standard resistor, 1% tolerance, added in series with the thermistor will increase the voltage seen at the NTC pin. The additional resistance required is calculated in Equation 46.

$$19.3k\Omega - 10.916k\Omega = 8.384k\Omega \quad \text{(EQ. 46)}$$

The closest, standard 1% tolerance resistor is 8.45kΩ.

The NTC thermistor is placed in a hot spot on the board, typically near the upper MOSFET of Channel 1 of the respective output. The standard resistor is placed next to the controller.

Layout Guidelines

PCB Layout Considerations

POWER AND SIGNAL LAYERS PLACEMENT ON THE PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding.

COMPONENT PLACEMENT

There are two sets of critical components in a DC/DC converter; the power components and the small signal components. The power components are the most critical because they switch large amounts of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each power train. Symmetrical layout allows heat to be dissipated equally across all power trains. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, PHASE and BOOT.

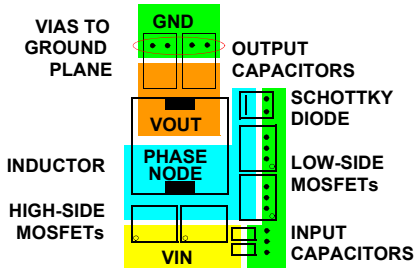


FIGURE 30. TYPICAL POWER COMPONENT PLACEMENT

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible (see Figure 30). Input high-frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High-frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target (microprocessor), making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Table 15 shows layout considerations for the ISL95712 controller by pin.

TABLE 15. LAYOUT CONSIDERATIONS FOR THE ISL95712 CONTROLLER

PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. A minimum of 5 vias are recommended to connect this pad to the internal ground plane layers of the PCB.
1	ISEN3_NB	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN_NB, then through another capacitor (C_{vsumn_nb}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISENx_NB pin to another ISENx_NB pin 2. Any ISENx_NB pin to GND
2	NTC_NB	The NTC thermistor must be placed close to the thermal source that is monitored to determine Northbridge thermal throttling. Placement at the hottest spot of the Northbridge VR is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.
3	IMON_NB	Place the IMON_NB resistor close to this pin and make a tight GND connection.
4	SVC	Use good signal integrity practices and follow AMD recommendations.
5	VR_HOT_L	Follow AMD recommendations. Placement of the pull-up resistor near the IC is recommended.
6	SVD	Use good signal integrity practices and follow AMD recommendations.
7	VDDIO	Use good signal integrity practices and follow AMD recommendations.
8	SVT	Use good signal integrity practices and follow AMD recommendations.
9	ENABLE	No special considerations.
10	PWROK	Use good signal integrity practices and follow AMD recommendations.
11	IMON	Place the IMON resistor close to this pin and make a tight GND connection.

TABLE 15. LAYOUT CONSIDERATIONS FOR THE ISL95712 CONTROLLER (Continued)

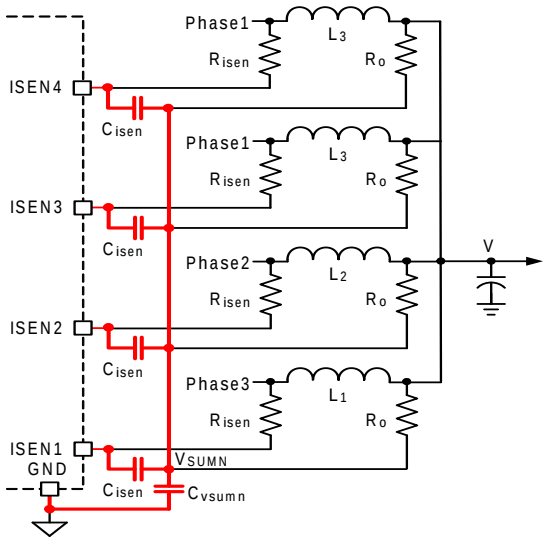
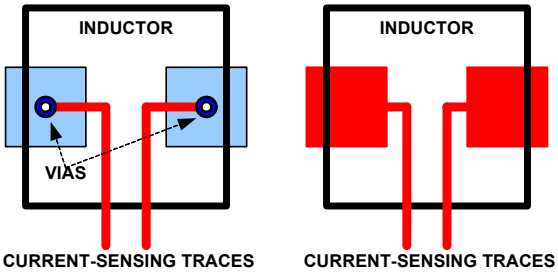
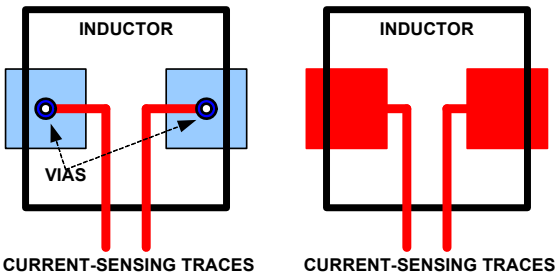
PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
12	NTC	The NTC thermistor must be placed close to the thermal source that is monitored to determine Core thermal throttling. Placement at the hottest spot of the Core VR is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.
13	ISEN4	Each ISEN pin has a capacitor (C_{isen}) decoupling it to V_{SUMN} and then through another capacitor (C_{vsumn}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops to be minimized. 
14	ISEN3	
15	ISEN2	
16	ISEN1	
17	ISUMP	Place the current sensing circuit in general proximity of the controller. Place capacitor C_n very close to the controller. Place the NTC thermistor next to Core VR Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of V_{SUMP} and V_{SUMN} signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
18	ISUMN	
19	VSEN	Place the filter on these pins in close proximity to the controller for good coupling.
20	RTN	
21	FB	Place the compensation components in general proximity of the controller.
22	VDD	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin with the filter resistor nearby the IC.
23	PGOOD	No special consideration.
24	COMP	Place the compensation components in general proximity of the controller.
25	BOOT1	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.

TABLE 15. LAYOUT CONSIDERATIONS FOR THE ISL95712 CONTROLLER (Continued)

PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
26	PHASE1	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE1 to the Core VR Channel 1 high-side MOSFET source pin instead of a general connection to PHASE1 copper is recommended for better performance.
27	UGATE1	
28	LGATE1	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
29	BOOT2	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
30	PHASE2	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE2 to the Core VR Channel 2 high-side MOSFET source pin instead of a general connection to PHASE2 copper is recommended for better performance.
31	UGATE2	
32	VDDP	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin.
33	LGATE2	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
34	LGATE1_NB	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
35	PHASE1_NB	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE1_NB to the high-side MOSFET source pin instead of a general connection to the PHASE1_NB copper is recommended for better performance.
36	UGATE1_NB	
37	BOOT1_NB	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
38	PWM3	No special considerations.
39	PWM4	No special considerations.
40	PWM2_NB	No special considerations.
41	PWM3_NB	No special considerations.
42	I2CLK	Use good signal integrity practices
43	I2DATA	Use good signal integrity practices
44	PROG	No special considerations.
45	PGOOD_NB	No special consideration.
46	COMP_NB	Place the compensation components in general proximity of the controller.
47	FB_NB	
48	VSEN_NB	Place the filter on this pin in close proximity to the controller for good coupling.
49	ISUMN_NB	Place the current sensing circuit in general proximity of the controller. Place capacitor C_n very close to the controller. Place the NTC thermistor next to NB VR Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of V_{SUMP} and V_{SUMN} signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
50	ISUMP_NB	
51	ISEN1_NB	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN_NB, then through another capacitor (C_{vsumn_nb}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISENx_NB pin to another ISENx_NB pin 2. Any ISENx_NB pin to GND
52	ISEN2_NB	

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 2, 2015	FN8566.1	On page 1 under Features, added “Serial VID clock frequency range 100kHz to 25MHz” below “Supports AMD SVI 2.0 serial data bus interface and PMBus”. Updated Package Outline Drawing L52.6X6A to the latest revision. Changes are as follows: -Added tolerance ± values.
March 26, 2014	FN8566.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

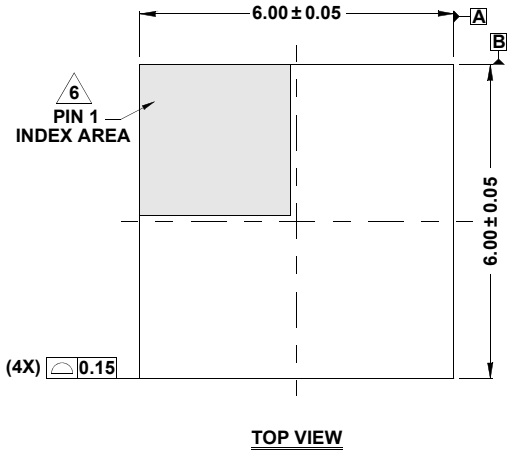
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

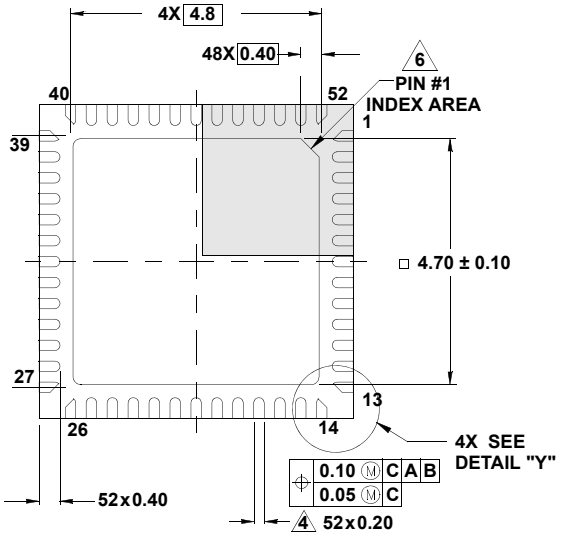
L52.6X6A

52 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE CHAMFERED CORNER LEADS

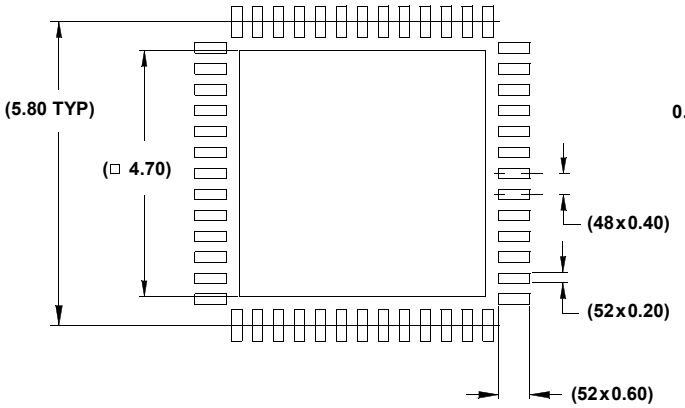
Rev 1, 7/14



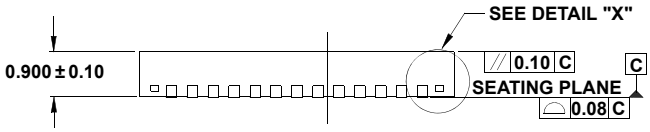
TOP VIEW



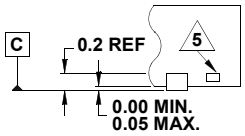
BOTTOM VIEW



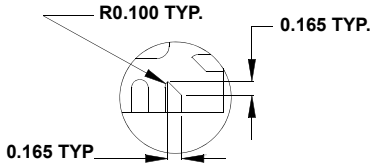
TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"



DETAIL "Y"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.