life.augmented

STGAP2D

Datasheet

Galvanically isolated 4 A half-bridge gate driver

SO-16

Product status link

STGAP2D

Product label

SUSTAINABLE TECHNOLOGY

Features

- 1700 V dual channel gate driver
- Driver current capability: 4 A sink / source at 25 °C
- dV/dt transient immunity ±100 V/ns
- Overall input-output propagation delay: 75 ns
- UVLO function
- Configurable interlocking function
- Dedicated SD and BRAKE pins
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function
- UL 1577 recognized

Applications

- Motor driver for industrial drives, factory automation, home appliances and fans
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

The STGAP2D is a half-bridge gate driver which isolates the gate driving channels from the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications.

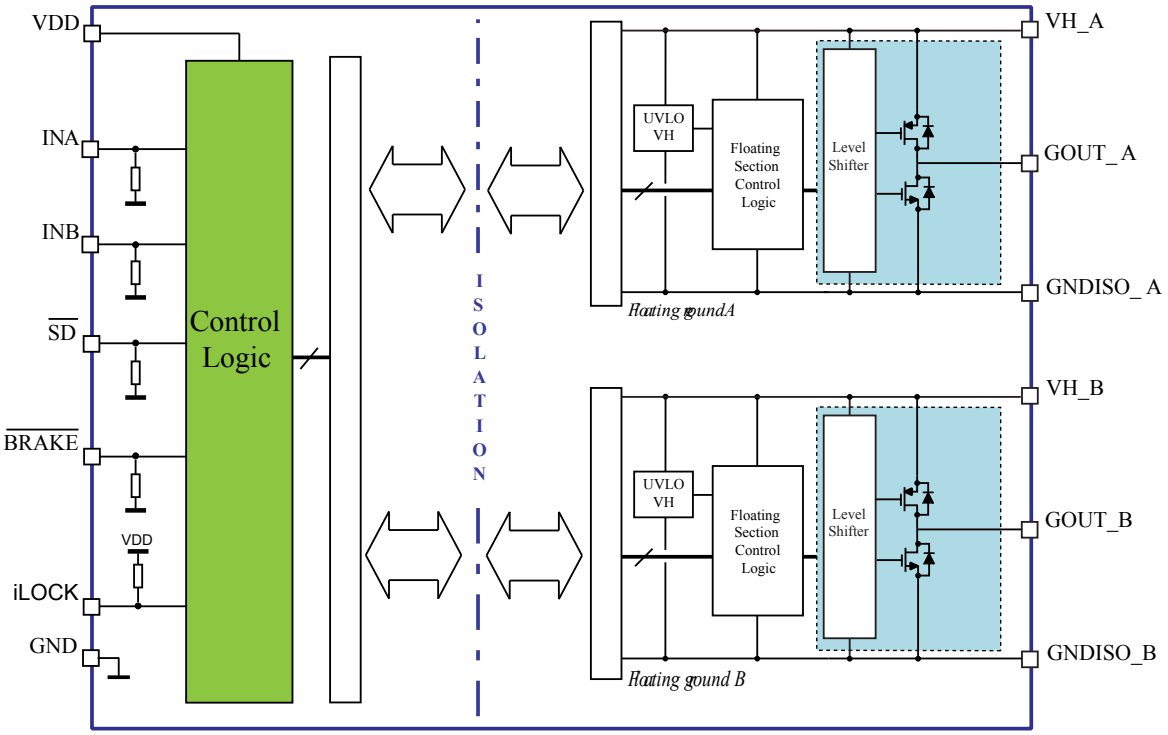
The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems, and an interlocking function prevents outputs from being high at the same time.

The input to output propagation delay results are contained within 75 ns, providing high PWM control accuracy.

A standby mode is available in order to reduce idle power consumption.

1 Block diagram

Figure 1. **Block diagram**



2 Pin description and connection diagram

Figure 2. **Pin connection (top view)**

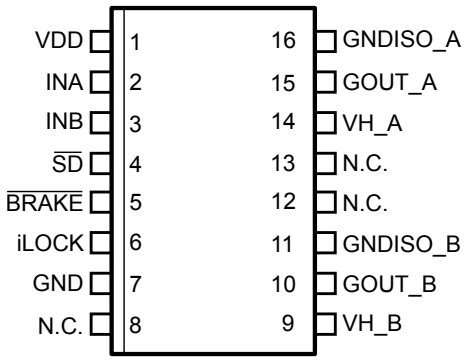


Table 1. **Pin description**

Pin #	Pin name	Type	Function
1	VDD	Power supply	Control logic supply voltage.
2	INA	Logic input	Control logic input for Channel A, active high.
3	INB	Logic input	Control logic input for Channel B, active high.
4	$\overline{SD}$	Logic input	Shutdown input, active low.
5	$\overline{BRAKE}$	Logic input	Control logic input, active low.
6	iLOCK	Analog input	Interlocking enable/disable.
7	GND	Power supply	Control logic ground.
9	VH_B	Power supply	Channel B gate driving positive supply.
10	GOUT_B	Analog output	Channel B Sink/Source output.
11	GNDISO_B	Power supply	Channel B gate driving isolated ground.
14	VH_A	Power supply	Channel A gate driving positive supply.
15	GOUT_A	Analog output	Channel A Sink/Source output.
16	GNDISO_A	Power supply	Channel A gate driving isolated ground.
Others	-	-	Not connected.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	-0.3	6.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.3	6.5	V
iLOCK	Interlocking enable vs. GND		-0.3	VDD + 0.3	V
VH_x	Positive supply voltage (VH_x vs. GNDISO_x)	-	-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GOUT_x vs. GNDISO_x)	-	-0.3	VH_x + 0.3	V
V_{ISO-OP}	Input to output isolation voltage (GND vs. GNDISO_x)	DC or peak	-1700	+1700	V
T_J	Junction temperature	-	-40	150	°C
T_S	Storage temperature	-	-50	150	°C
P_{Din}	Power Dissipation input chip	T_A = 25 °C	-	40	mW
P_{Dout}	Power Dissipation output chip	T_A = 25 °C	-	1.16	W
ESD	HBM- (human body model)	-	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-16	90	°C/W

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	3.1	5.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
iLOCK	Interlocking enable vs. GND		0	VDD	V
VH_x	Positive supply voltage (VH_x vs. GNDISO-x)	-	-	26	V
$GNDISO_{A-B}$ (1)	Floating grounds differential voltage (GNDISO_A - GNDISO_B)	DC or peak	-1500	+1500	V
F_{SW}	Maximum switching frequency(2)	-	-	1	MHz
t_{OUT}	Pulse width	-	100	-	ns
T_J	Operating Junction Temperature	-	-40	125	°C

1. *Characterization data, 1200 V max. tested in production.*
2. *Actual limit depends on power dissipation and T_J*

4 Electrical characteristics

Table 5. Electrical characteristics (T_J = 25 °C, VH_x = 15 V, VDD = 5 V unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	INA, INB, SD, BRAKE	Input to output propagation delay ON	See Figure 8	50	75	90	ns
t_{Doff}	INA, INB, SD, BRAKE	Input to output propagation delay OFF	See Figure 8	50	75	90	ns
t_r	-	Rise time	C_L = 4.7 nF, See Figure 8	-	30	-	ns
t_f	-	Fall time		-	30	-	ns
PWD	-	Pulse width distortion(1)	-	-	-	20	ns
$t_{deglitch}$	INA, INB, SD, BRAKE	Inputs deglitch filter	-	-	20	40	ns
CMTI(2)	-	Common-mode transient immunity, | dV_{ISO}/dt|	V_{CM} = 1500 V, see Figure 9	100	-	-	V/ns
Supply voltage							
VH_{on}	-	VH_x UVLO turn-on threshold	-	8.6	9.1	9.6	V
VH_{off}	-	VH_x UVLO turn-off threshold	-	7.9	8.4	8.9	V
VH_{hyst}	-	VH_x UVLO hysteresis	-	0.6	0.75	0.95	V
I_{QHU_A}, I_{QHU_B}	-	VH_x undervoltage quiescent supply current	VH_x = 7 V	-	1.3	1.8	mA
I_{QH_A}, I_{QH_B}	-	VH_x quiescent supply current	-	-	1.3	1.8	mA
I_{QHSBY_A}, I_{QHSBY_B}	-	Standby VH_x quiescent supply current	-	-	400	550	µA
SafeClp	-	GOUT active clamp	I_{GOUT} = 0.2 A; VH floating	-	2	2.3	V
I_{QDD}	-	VDD quiescent supply current	-	-	1.8	2.4	mA
I_{QDDSBY}	-	Stand-by VDD quiescent supply current	Standby mode	-	40	80	µA
Logic inputs							
V_{il}	INA, INB, SD, BRAKE	Low-level logic threshold voltage	-	0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	INA, INB, SD, BRAKE	High-level logic threshold voltage	-	0.62·VDD	0.66·VDD	0.7·VDD	V
I_{logic_h}	INA, INB, SD, BRAKE	Logic inputs high-level input bias current	V_{logic} = 5 V	33	50	70	µA
I_{logic_l}	INA, INB, SD, BRAKE	Logic inputs low-level input bias current	V_{logic} = 0 V	-	-	1	µA
R_{pd}	INA, INB, SD, BRAKE	Logic inputs pull-down resistor	-	70	100	150	kΩ
Interlocking							
iLOCKen	iLOCK	Interlocking enable voltage		0.7·VDD V			V
$iLOCK_{_l}$	iLOCK	iLOCK low-level bias current	iLOCK = GND	35	55	75	µA
$iLOCK_{_h}$	iLOCK	iLOCK high-level bias current	iLOCK = VDD			1	µA
$iLOCK_{_pu}$	iLOCK	iLOCK pull-up resistor		66	90	142	kΩ

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Driver buffer section							
I_{GON}	GOUT	Source short-circuit current	T_J = 25 °C	-	4	-	A
			T_J = -40 to +125 °C (2)	3	-	5	
I_{GOFF}	GOUT	Sink short-circuit current	T_J = 25 °C	-	4	-	A
			T_J = -40 to +125 °C (2)	3	-	5.5	
V_{GONH}	GOUT	G_{ON} output high-level voltage	I_{GON} = 100 mA	VH - 0.15	VH - 0.125	-	V
V_{GOFFL}	GOUT	G_{OFF} output low-level voltage	I_{GOFF} = 100 mA	-	110	120	mV
R_{GON}	GOUT	Source R_{DS_ON}	I_{GON} = 100 mA	-	1.25	1.5	Ω
R_{GOFF}	GOUT	Sink R_{DS_ON}	I_{GOFF} = 100 mA	-	1.1	1.2	Ω
Overtemperature protection							
T_{SD}		Shutdown temperature	-	170	-	-	°C
T_{hys}		Temperature hysteresis	-	-	20	-	°C
Standby							
t_{STBY}	-	Standby time	See Section 5.6	200	280	500	µs
t_{WUP}	-	Wake-up time		10	20	35	µs
t_{awake}	-	Wake-up delay		90	140	200	µs
$t_{stbyfilt}$	-	Standby filter		200	280	800	ns

1. *PWD = max ($|t_{Don(A)} - t_{Don(B)}|$, $|t_{Doff(A)} - t_{Doff(B)}|$, $|t_{Doff(A)} - t_{Don(B)}|$, $|t_{Doff(B)} - t_{Don(A)}|$).*
2. *Characterization data, not tested in production.*

Table 6. Isolation related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap)	CLR	4	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	4	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index (Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 7. Isolation characteristics

Parameter	Symbol	Test Conditions	Characteristic	Unit
Input to Output test voltage In accordance with VDE 0884-11	V_{PR}	Method a, Type test	2720	V_{PEAK}
		V_{PR} = 2720, t_m = 10 s		
		Partial discharge < 5 pC		
		Method b1, 100% Production test	3200	V_{PEAK}
		V_{PR} = 3200, t_m = 1 s		
		Partial discharge < 5 pC		
Transient Overvoltage (Highest Allowable Overvoltage)	V_{IOTM}	t_{ini} = 60 s Type test	4800	V_{PEAK}
Maximum Surge Test Voltage	V_{IOSM}	Type test	4800	V_{PEAK}
Isolation Resistance	R_{IO}	V_{IO} = 500 V, Type test	>10^9	Ω

Table 8. UL 1577 isolation voltage ratings

Description	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1 min (Type test)	V_{ISO}	2828/4000	V_{rms}/ PEAK
Isolation Test Voltage, 1 sec (100% production)	$V_{ISOtest}$	3394/4800	V_{rms}/ PEAK

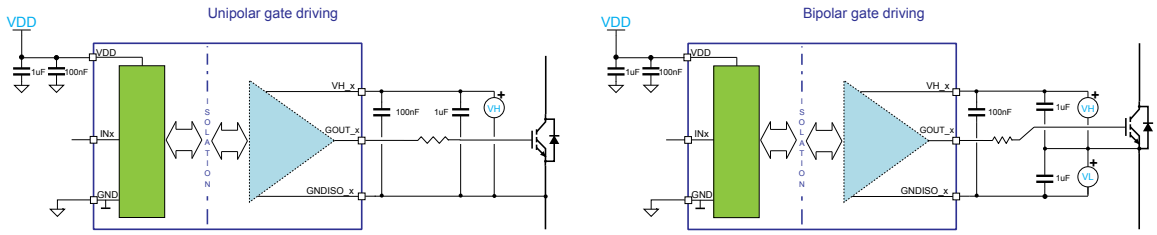
Recognized under the UL 1577 Component Recognition Program - file number E362869

5 Functional description

5.1 Gate driving power supply and UVLO

The STGAP2D is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementing either unipolar or bipolar gate driving.

Figure 3. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH_x supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH_x voltage goes below the VH_{off} threshold, the output buffer enters 'safe state'. When VH_x voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH_x supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. We recommend using low-ESR SMT ceramic capacitors for the best filtering performance. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value between 1 µF and 10 µF should be placed close to it.

5.2 Power-up, power-down and safe state

The following conditions define the safe state:

- GOUT n-channel = ON state
- GOUT p-channel = high impedance

Such conditions are maintained at power-up of the isolated side (VH_x < VH_{on}) and during whole device power-down phase (VH < VH_{off}), regardless of the value of the input pins.

The device integrates a structure that clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOUT n-channel on. If VH_x positive supply pin is floating or not supplied, the GOUT pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state and remains in this condition until the VDD voltage returns to operative conditions.

After power-up of both isolated and low voltage side, the device output state depends on the status of the input pins.

5.3 Control Inputs

The device is controlled through the following logic inputs:

- SD: active low shutdown input;
- BRAKE: active low brake input;
- INA, INB: active high logic inputs for channel A and channel B driver outputs;
- iLOCK: used to enable or disable the interlocking protection

The operation of the driver IOs is described in Table 9.

Table 9. Inputs truth table (applicable when device is not in UVLO or "safe state")

Input pins(1)						Output pins	
	iLOCK	$\overline{SD}$	$\overline{BRAKE}$	INA	INB	GOUT_A	GOUT_B
	X	L	X	X	X	Low	Low
	X	H	L	X	X	Low	**HIGH**
	X	H	H	L	L	Low	Low
	X	H	H	H	L	**HIGH**	Low
	X	H	H	L	H	Low	**HIGH**
Interlocking	VDD	H	H	H	H	Low	Low
	GND	H	H	H	H	**HIGH**	**HIGH**

1. *X: Don't care.*

A deglitch filter allows input signals with duration shorter than $t_{deglitch}$ to be ignored, thereby preventing any noise spikes in the application from generating unwanted commutations.

5.4 Watchdog

The isolated HV side has a watchdog function to identify when it is not able to communicate with the LV side; for example, because the VDD of the LV side is not supplied. In this case, the output of the driver is forced into 'safe state' until the communication link is properly established again.

5.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced into 'safe state'. Device operation is restored as soon as the junction temperature falls below T_{SD} - T_{hys}.

5.6 Standby function

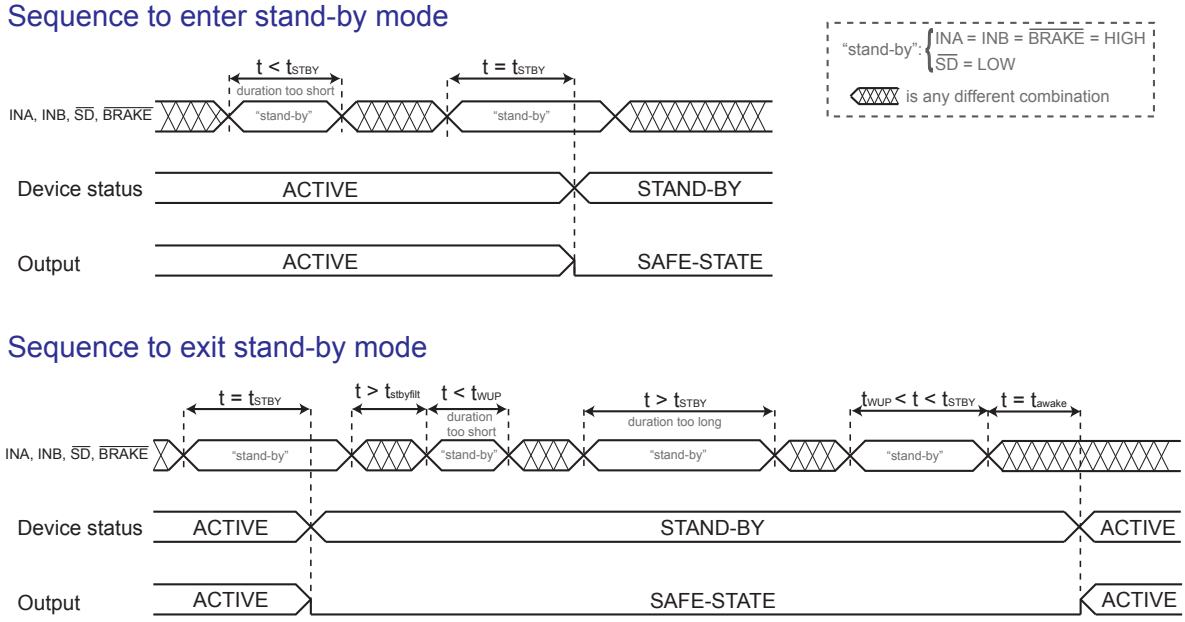
The device can be put in standby mode to reduce the power consumption of both the control interface and gate driving sides. In standby mode, the quiescent current from VDD and VH_x supply pins is reduced to I_{QDDS} and I_{QHS_x}, respectively, and the output remains in 'safe state' (the output is actively forced low).

To enter standby, keep the SD low while keeping the other input pins (INA, INB and BRAKE) high ('standby' value) for a time longer than t_{STBY}. During standby, the inputs can change from the 'standby' value.

To exit standby, inputs must be put in any combination different from the 'standby' value for a time longer than $t_{stbyfilt}$, and then in the "standby" value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the 'standby' value, the output is enabled and set according to inputs state after a time t_{awake}.

Figure 4. Standby state sequences



5.7 Interlocking function

The interlocking function prevents outputs GOUT_A and GOUT_B from being high at the same time, regardless of the status of the input pins INA and INB.

In half-bridge topologies this protection avoids shoot-through in case that wrong input signals are generated by the controller device. In case the status of INA and INB is such to require both channels to be ON at the same time, the driver turns both channels off.

In some topologies it is required to allow both channels to be ON at the same time: this can be achieved by disabling the interlocking function trough the iLOCK pin. The iLOCK pin shall be either connected to VDD, which enables the interlocking function, or to GND, which disables the interlocking function and allows parallel operation of Channel_A and Channel_B.

Refer to Section 5.3 for complete logic inputs truth table.

6 Typical application diagrams

Figure 5. **Half-bridge configuration**

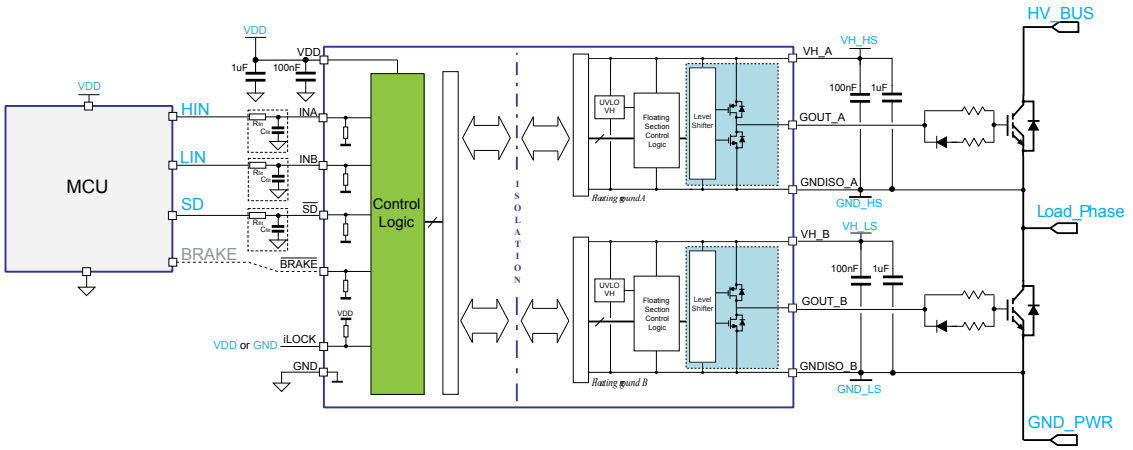
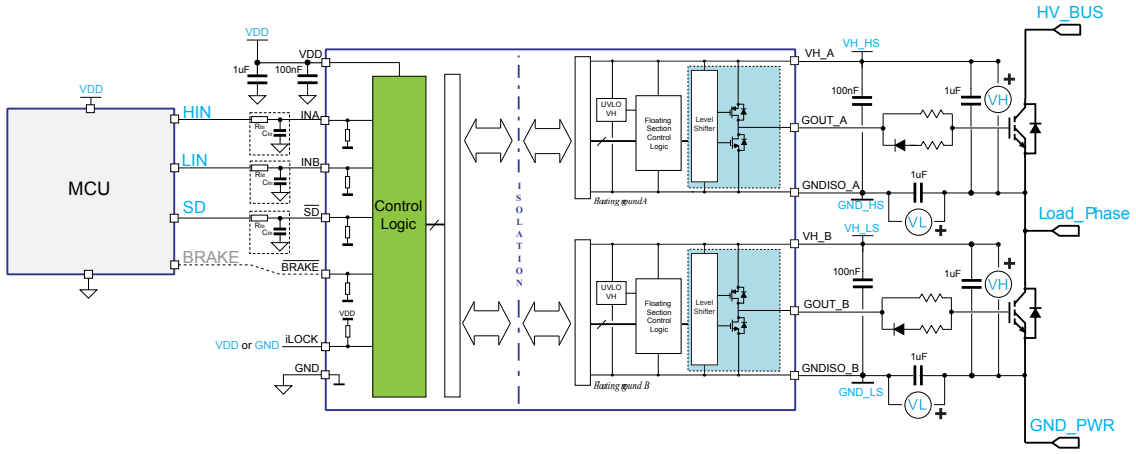


Figure 6. **Half-bridge configuration with negative gate driving**



7 Layout

7.1 Layout guidelines and considerations

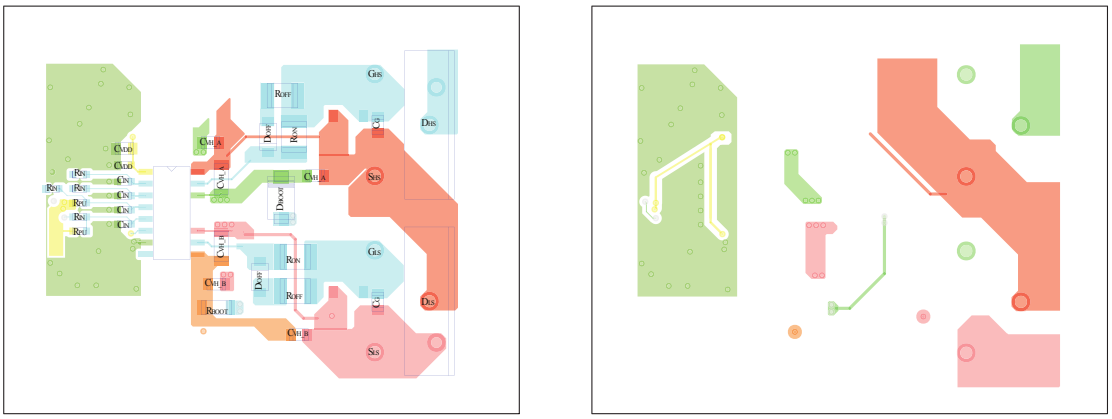
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMD ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF capacitor must be placed between VDD and GND and between VH_x and GNDISO_x, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current a second capacitor with value in the range between 1 µF and 10 µF should also be placed close to the supply pins.
  - As a good practice it is suggested to add filtering capacitors close to logic inputs of the device (INA, INB, BRAKE, SD), in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might bring about noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH_x and GNDISO_x pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

7.2 Layout example

An example of STGAP2D suggested half-bridge with negative gate driving PCB layout is shown in Figure 7; the main signals have been highlighted by different colors. It is recommended to follow this example for proper positioning and connection of filtering capacitors.

Figure 7. Suggested PCB layout for half-bridge configuration with negative driving voltage



8 Testing and characterization information

Figure 8. **Timings definition**

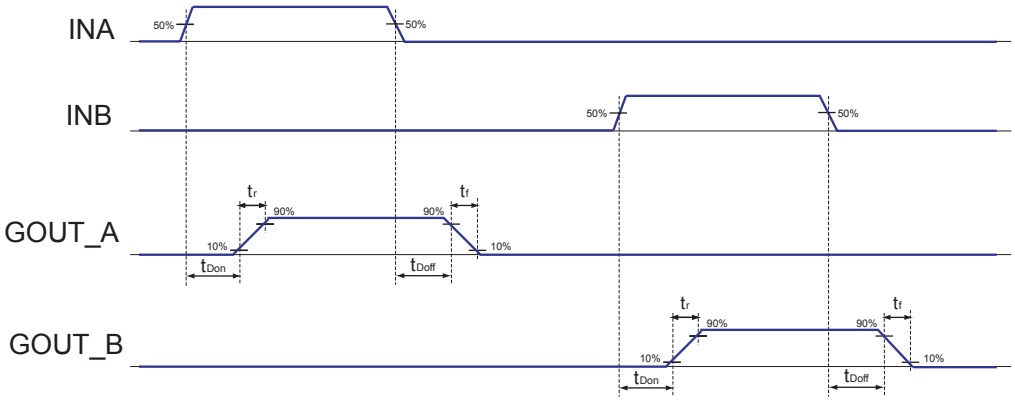
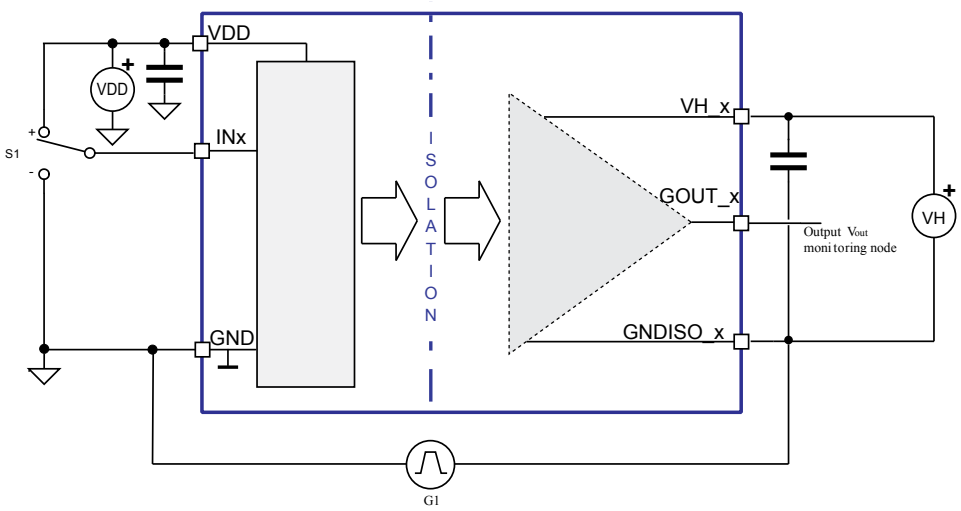


Figure 9. **CMTI test circuit**



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

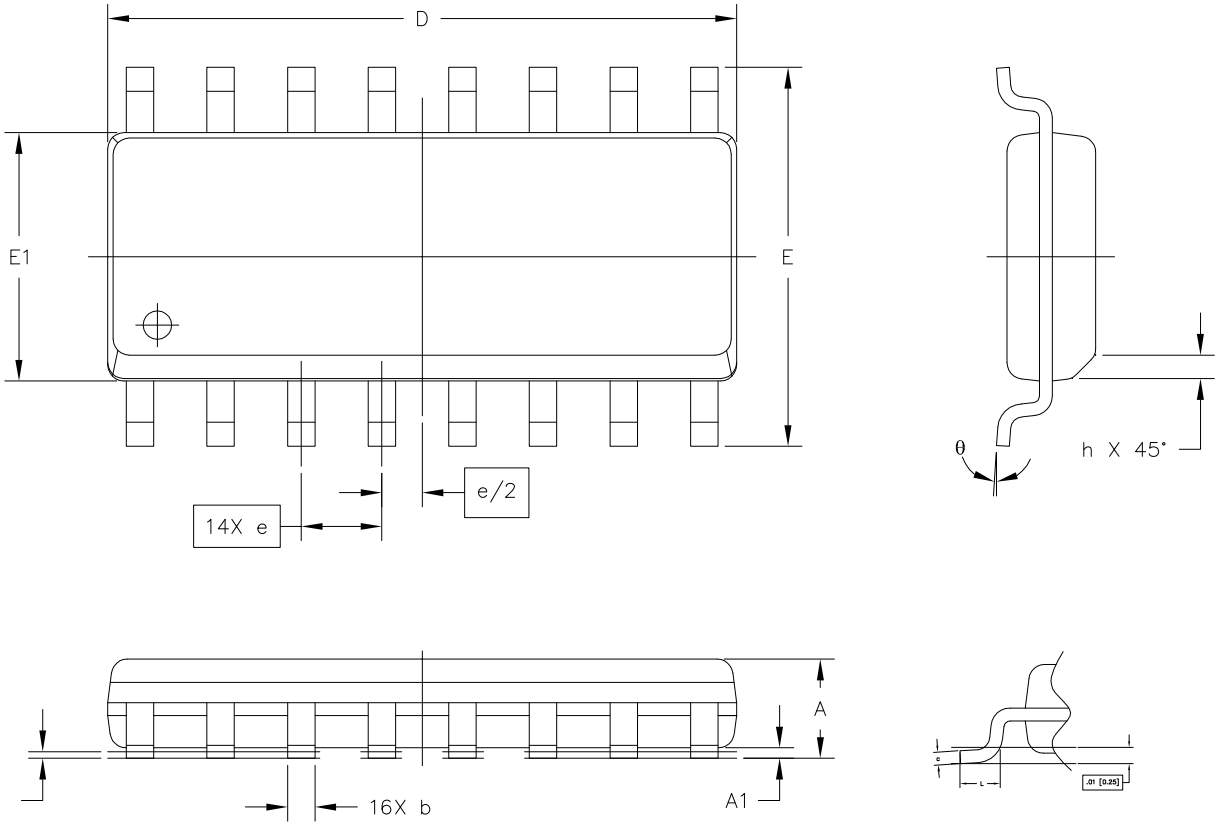
9.1 SO-16 narrow package information

Table 10. SO-16 narrow package dimensions

Dim.	mm			NOTES
	Min.	Typ.	Max.	
A	1.35	-	1.75	-
A1	0.10	-	0.25	-
b	0.35	-	0.49	(1)
c	0.19	-	0.25	-
D	9.80	-	10.00	(2)
E	5.80	-	6.20	-
E1	3.80	-	4.00	(2)
e	1.27BSC			-
L	0.40	-	1.25	-
h	0.25	-	0.50	-
Θ	0	-	7	degrees

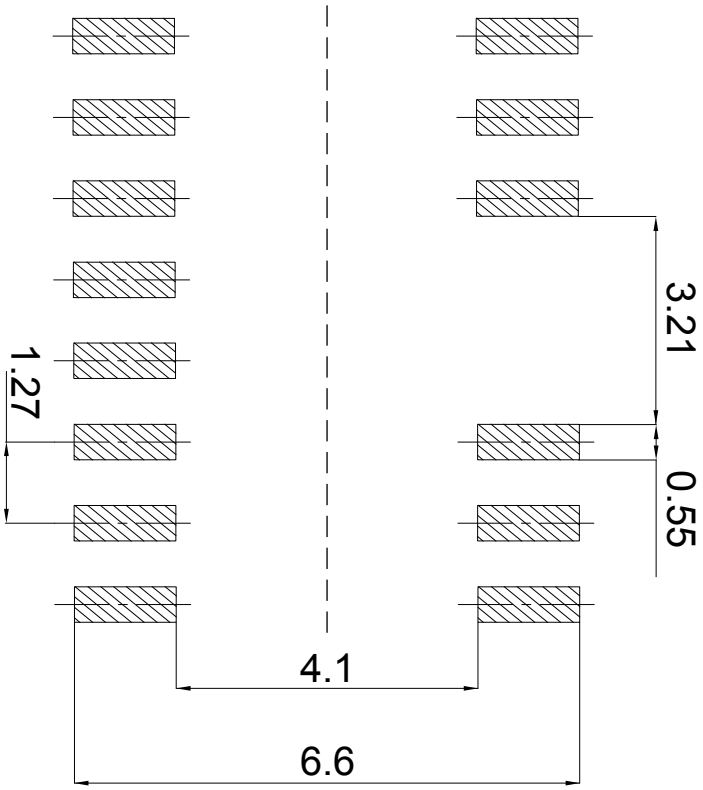
1. *Dimension "b" and "E1" does not include dam bar protrusion (allowable dam bar protrusion shall be 0.127 mm total).*
2. *Dimension "D" and "E1" do not include mold protrusions (maximum 0.15 mm per side).*

Figure 10. **SO-16 package outline**



10 Suggested land pattern

Figure 11. **SO-16 suggested land pattern**



11 Ordering information

Table 11. **Device summary**

Order code	Output configuration	Package	Package marking	Packaging
STGAP2DM	GOUT	SO-16	GAP2DM	Tube
STGAP2DMTR	GOUT	SO-16	GAP2DM	Tape and Reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
24-Aug-2018	1	Initial release.
26-Jan-2022	2	Added iLOCK pin for interlocking function disable. Added Table 6, Table 7, and Table 8. Updated Table 2, Table 4, and Table 5. Updated Figure 3.
25-Jul-2022	3	Updated Table 2, added UL file certification

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