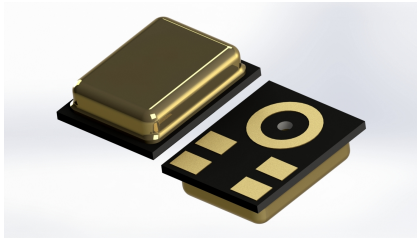


MEMS audio sensor: digital microphone with multiple performance modes



RHLGA 5LD (3.5 x 2.65 x 0.98 mm)

Product status link

[MP23DB01HP](#)

Product summary

Order code	MP23DB01HPTR
Temp. range [°C]	-40 to +85
Package	RHLGA 5LD (3.5 x 2.65 x 0.98) mm
Packing	Tape and reel

Features

- Omnidirectional digital microphone
- Very low distortion / very high AOP
 - 135 dB SPL acoustic overload point for all operative modes
- Sensitivity: -41 dBFS ±1dB
- Sensitivity matching
- “Always-on” experience with low power consumption
- Multiple performance modes (sleep, low-power, performance)
- Typical current consumption
 - 2 µA (sleep mode)
 - 285 µA (low-power mode)
 - 800 µA (performance mode)
- PDM single-bit output with option for stereo configuration
- RHLGA package
 - Bottom-port design
 - SMD-compliant
 - EMI-shielded
 - ECOPACK, RoHS and “Green” compliant

Applications

- Smart IoT
- Smartphones and handsets
- Smart speakers
- Laptops and notebook computers
- Wearable devices
- TWS and headsets
- Hands-free calling

Description

The **MP23DB01HP** is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface with optional stereo configuration.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process dedicated to producing audio sensors.

The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format.

The **MP23DB01HP** offers multiple performance modes (power-down, low-power and performance mode) enabled by different clock frequency ranges. The device has a very high AOP in performance mode, sensitivity range of ±1 dB and high SNR for all operative modes.

The **MP23DB01HP** is available in a bottom-port, SMD-compliant, EMI-shielded package and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

1 Pin description

Figure 1. Pin connections

Bottom View

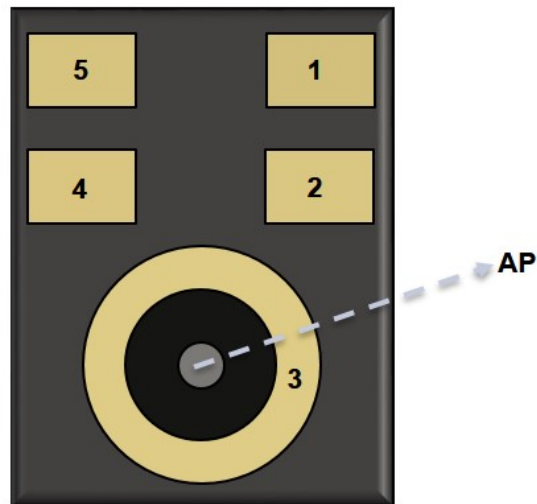


Table 1. Pin description

Pin #	Pin name	Function
1	DOUT	Left/right PDM data output
2	L/R	Left/right channel selection
3 (ground ring)	GND	0 V supply
4	CLK	Synchronization input clock
5	VDD	Supply voltage

2 Acoustic and electrical specifications

2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for Vdd = 1.8 V, clock = 2.4 MHz, T = 25 °C, no load, unless otherwise noted.

Table 2. Acoustic and electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
Vdd	Supply voltage		1.6		3.6	V
f _{CLK}	Clock frequency range ⁽²⁾⁽³⁾	Power-down mode	0		0.15	MHz
		Low-power mode	0.54	0.768	1.1	
		Performance mode	1.5	2.4	3.3	
I _{dd}	Current consumption in low-power mode	Fc = 768 kHz		285		μA
	Current consumption in performance mode	Fc = 2.4 MHz		800		
		Fc = 3.072 MHz		880		
I _{ddPdn}	Current consumption in power-down mode ⁽⁴⁾			2	5	
I _{cc}	Short-circuit current		1		10	mA
V _{IOL}	Low-level logic input/output voltage	I _{out} = 1 mA	-0.3		0.35xV _{dd}	V
V _{IOH}	High-level logic input/output voltage	I _{out} = 1 mA	0.65xV _{dd}		V _{dd} +0.3	V
T _{WK}	Wake-up time ⁽⁵⁾	Specified by design			20	ms
Roll-off	Frequency response	at -3 dB		35		Hz
C _{load}	DOUT load capacitance				100	pF
T _{op}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Duty cycle: min = 40% max = 60%
3. In case of mode change (from low-power to performance mode or vice versa), the clock has to be continuous or has to be stopped for at least 50 μs.
4. Input clock in static mode
5. Time from the first clock edge to valid output data

The values listed in the table below are specified for V_{dd} = 1.8 V, clock = 768 kHz, no load, T = 25 °C, unless otherwise noted.

Table 3. Low-power mode

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
I _{dd}	Current consumption			285		μA
S _o	Sensitivity	94 dB SPL @ 1 kHz	-25	-24	-23	dBFS
SNR	Signal-to-noise ratio	94 dB SPL @ 1 kHz A-weighted (20 Hz - 8 kHz)		64		dB(A)
THD	Total harmonic distortion	94 dB SPL @ 1 kHz		0.2		%
AOP	Acoustic overload point			120		dB SPL
PSR	Power supply rejection	100 mVpp sine wave @ 217 Hz		-85		dBFS

1. Typical specifications are not guaranteed.

The values listed in the table below are specified for V_{dd} = 1.8 V, clock = 2.4 MHz, no load, T = 25 °C, unless otherwise noted.

Table 4. Performance mode

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
I _{dd}	Current consumption	2.4 MHz		800		μA
		3.072 MHz		880		
S _o	Sensitivity	94 dB SPL @ 1 kHz	-42	-41	-40	dBFS
SNR	Signal-to-noise ratio 94 dB SPL @ 1 kHz A-weighted (20 Hz - 20 kHz)	2.4 MHz		65		dB(A)
		3.072 MHz		65.5		
THD	Total harmonic distortion	94 dB SPL @ 1 kHz		0.2		%
		110 dB SPL @ 1 kHz		0.5		
AOP	Acoustic overload point			135		dB SPL
PSR	Power supply rejection	100 mVpp sine wave @ 217 Hz		-95		dBFS

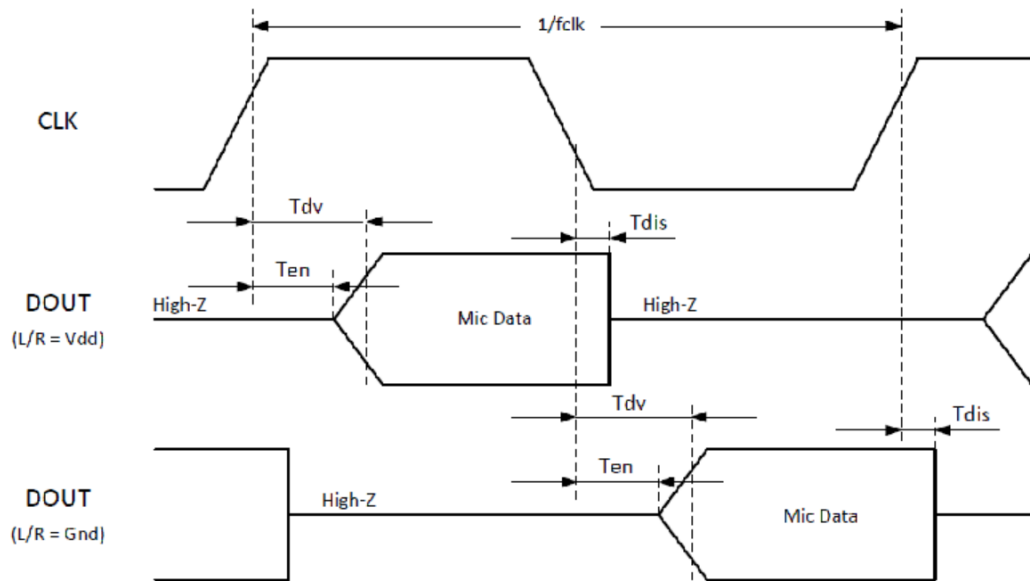
1. Typical specifications are not guaranteed.

2.2 Timing characteristics

Table 5. Timing characteristics

Symbol	Description	Min.	Max.	Unit
T_{dv}	Delay time to valid data (Cload = 100 pF)		120	ns
T_{en}	Delay time to driven data	19		ns
T_{dis}	Delay time to high-Z	4	17	ns

Figure 2. Timing waveforms



2.3 Typical performance curves

Figure 3. Typical free-field response normalized to 1 kHz

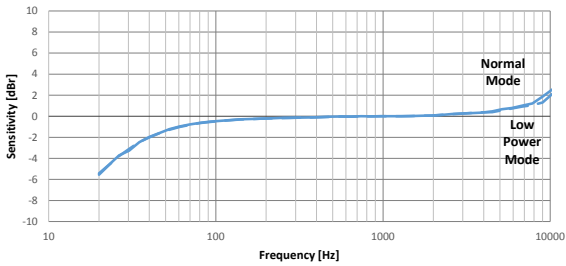


Figure 4. Typical PSRR

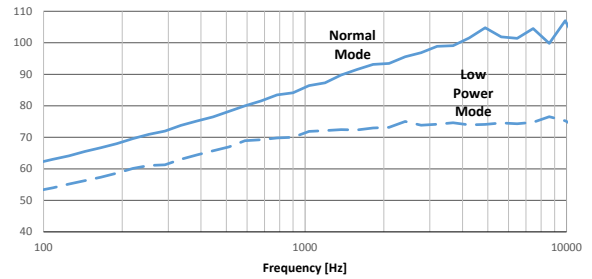


Figure 5. Typical THD at 1 kHz vs. sound pressure level

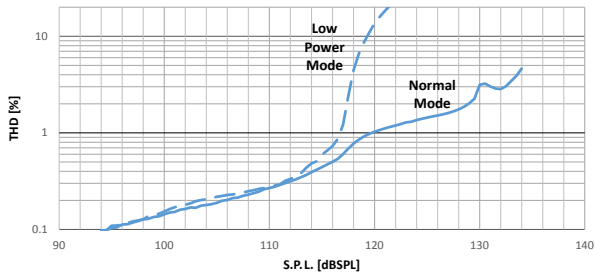


Figure 6. Typical I_{dd} vs. V_{dd}

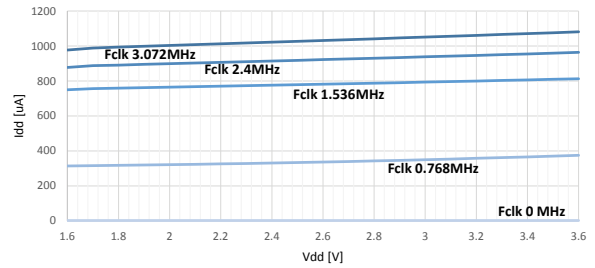


Figure 7. Typical THD at 1 kHz vs. sound pressure level

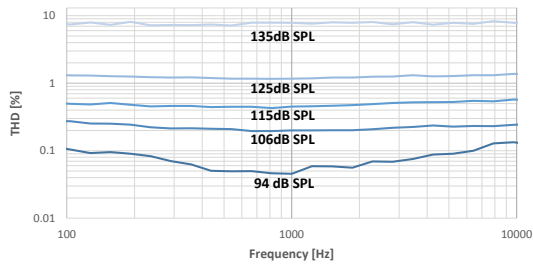
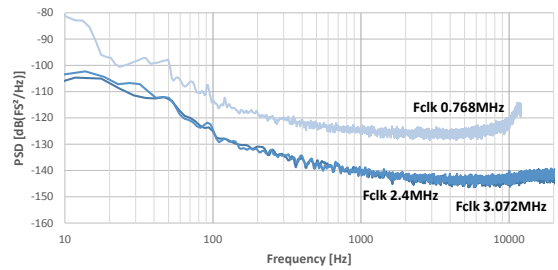


Figure 8. Noise floor power spectral density



3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
V _{DD}	Supply voltage	-0.3 to 4.8	V
V _{IN}	Input voltage on any control pin ⁽¹⁾	-0.3 to V _{DD} +0.3	V
T _{OP}	Operating temperature range	-40 to +105	°C
T _{STG}	Storage temperature range	-40 to +125	°C
ESD	(HBM) ANSI/ESDA/JEDEC JS001	±2000	V
	(MM) EIA/JESD22-A115	±200	
	(CDM) JESD22-C101	±750	
ESD ⁽²⁾	Per IEC61000-4-2, 150 pF, 330 Ω direct contact to housing	±8000	V

1. Supply voltage on any pin should never exceed 4.8V

2. Bypass capacitor of 200 nF or 1 μF (better) is highly recommended for ESD main clamp integrity.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4 Functionality

4.1 L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as indicated in the following table. The L/R pin must be connected to Vdd or GND.

Table 7. L/R channel selection

L/R	CLK low	CLK high
GND	Data valid	High impedance
Vdd	High impedance	Data valid

Note: As the L/R pin is internally connected to GND via a 200 kΩ pull-down resistor, it is not mandatory to connect the pin itself to GND for the respective channel selection.

5 Application recommendations

Figure 9. MP23DB01HP electrical connections

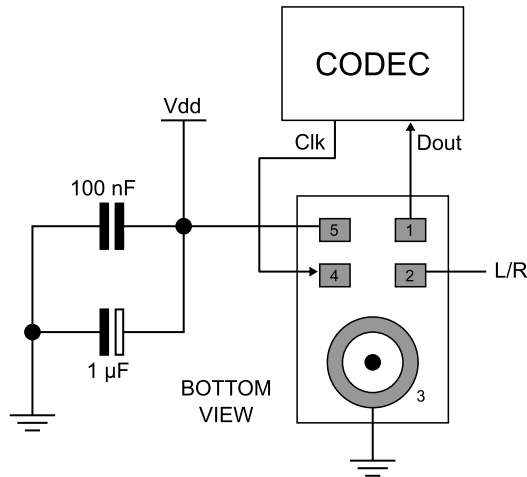
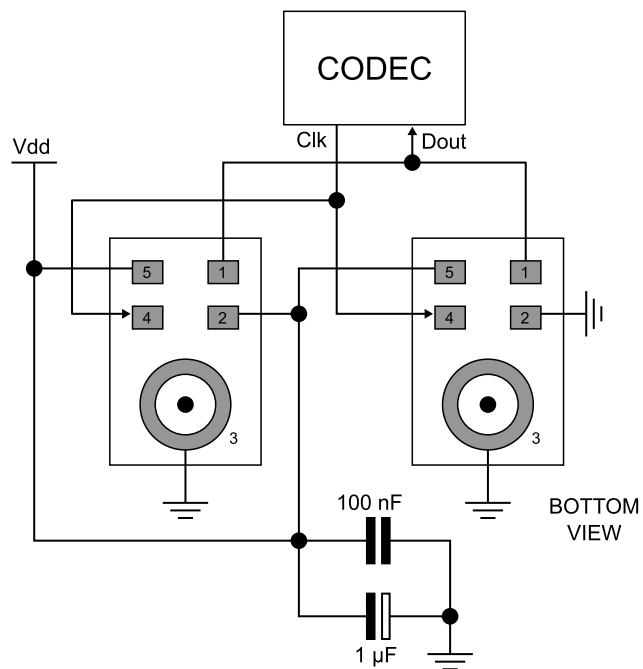


Figure 10. MP23DB01HP electrical connections for stereo configuration



Power supply decoupling capacitors (100 nF ceramic, 1 μF ceramic) should be placed as near as possible to pin 2 of the device (common design practice).

The L/R pin must be connected to Vdd or GND (refer to [Table 7](#)).

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Soldering information

The RHLGA (3.5 x 2.65 x 0.98) mm package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Landing pattern and soldering recommendations are available at www.st.com.

Figure 11. Recommended soldering profile limits

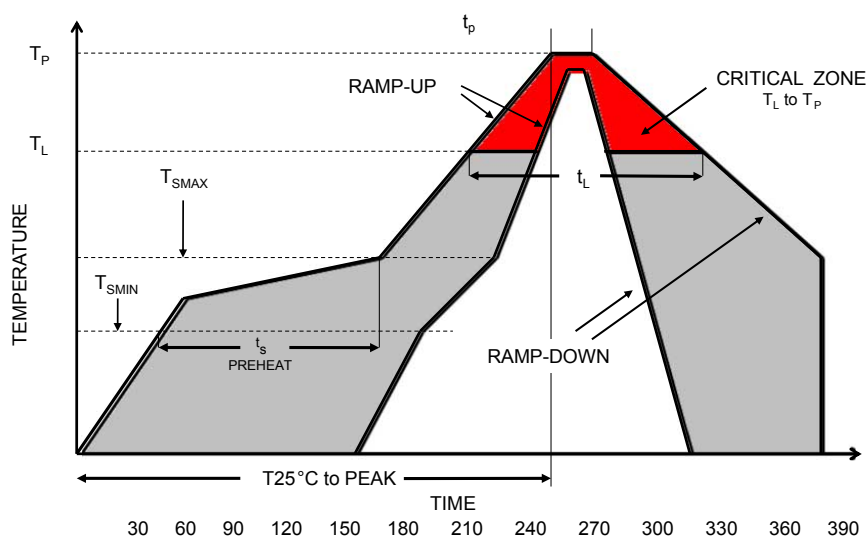
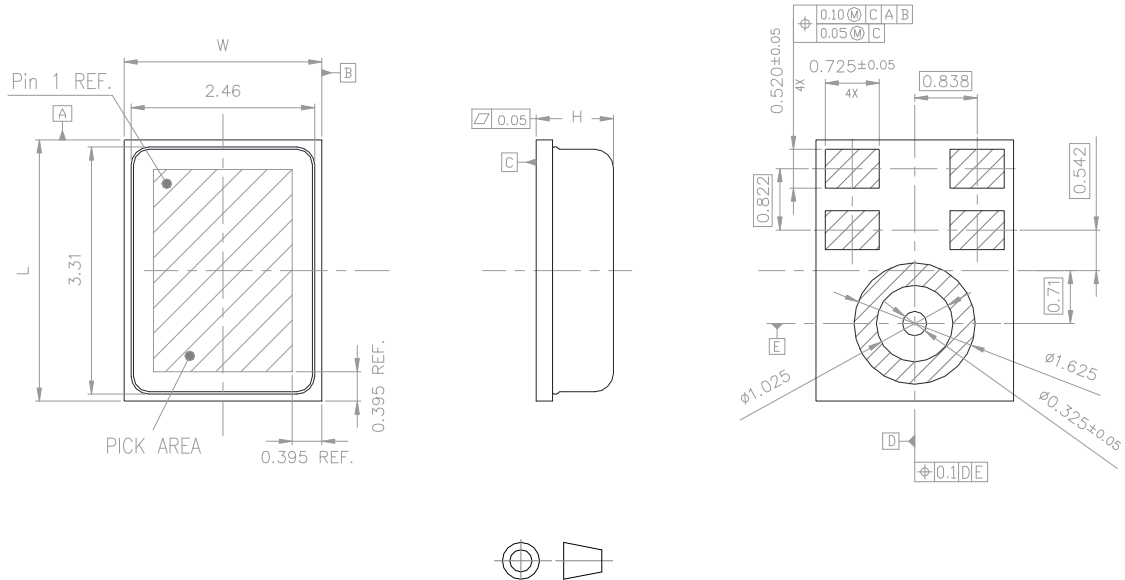


Table 8. Recommended soldering profile limits

Description	Parameter	Pb free
Average ramp rate	T_L to T_P	3 °C/sec max
Preheat		
Minimum temperature	T_{SMIN}	150 °C
Maximum temperature	T_{SMAX}	200 °C
Time (T_{SMIN} to T_{SMAX})	t_s	60 sec to 120 sec
Ramp-up rate	T_{SMAX} to T_L	
Time maintained above liquidus temperature	t_L	60 sec to 150 sec
Liquidus temperature	T_L	217 °C
Peak temperature	T_P	260 °C max
Time within 5 °C of actual peak temperature		20 sec to 40 sec
Ramp-down rate		6 °C/sec max
Time 25 °C ($t_{25\text{ °C}}$) to peak temperature		8 minutes max

6.2 RHLGA-5L package information

Figure 12. RHLGA 3.5 x 2.65 x 0.98 mm (metal cap) 5L package outline



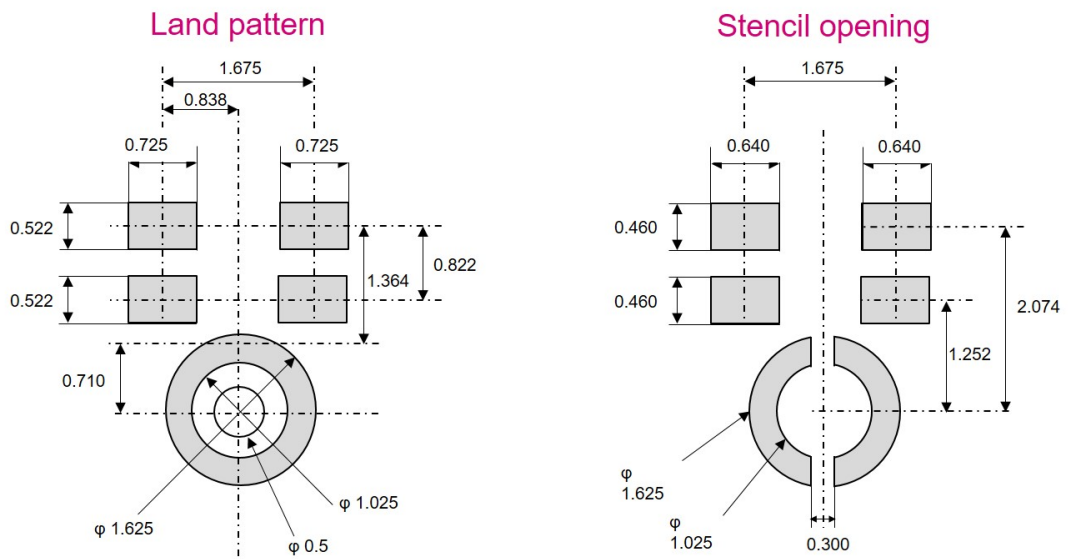
Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.15mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	3.5	±0.1
Width [W]	2.65	±0.1
Height [H]	1.08 MAX	

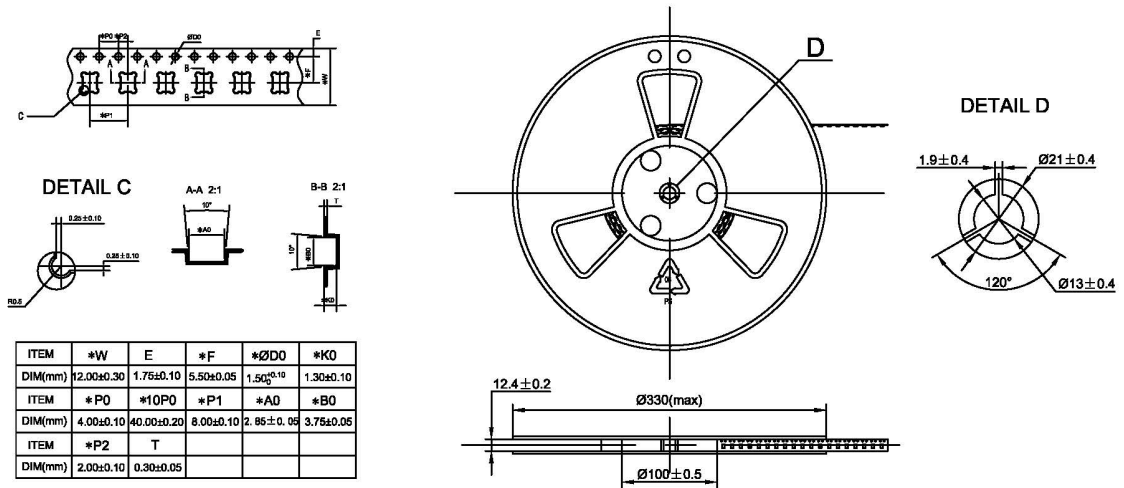
DM00368430_3

Figure 13. Land pattern and recommended stencil opening



6.3 RHLGA-5L packing information

Figure 14. Carrier tape and reel mechanical specifications



Specifications:

1. Unmarked tolerance: $\pm 0.1\text{mm}$;
2. Surface resistance: $10^5 - 10^{10} \Omega/\text{SQ}$, $25 \pm 5^\circ\text{C}/50 \pm 5\%\text{RH}$;

Revision history

Table 9. Document revision history

Date	Version	Changes
29-Apr-2020	1	Initial release
27-Jul-2020	2	Added footnote 3 regarding the clock to Table 3: General microphone specifications
10-Feb-2022	3	Updated wake-up time in Table 2. Acoustic and electrical characteristics Replaced frequency response with Section 2.3 Typical performance curves Minor textual updates
07-Mar-2022	4	Updated Figure 3. Typical free-field response normalized to 1 kHz

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