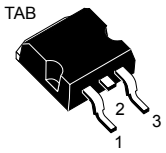
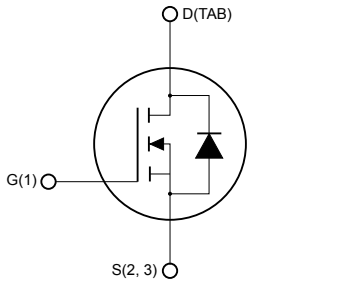
STH200N10WF7-2

Datasheet

N-channel 100 V, 3.2 mΩ typ., 180 A, STripFET F7 Power MOSFET in an H²PAK-2 package



H²PAK-2



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH200N10WF7-2	100 V	4.0 mΩ	180 A	340 W

- Best-in-class SOA capability
- High current surge capability
- Extremely low on-resistance

Applications

- Hot-swap
- Electronic fuse
- Load switch
- In-rush current limiter

Description

This N-channel Power MOSFET utilizes the STripFET F7 technology with an enhanced trench gate structure boosting linear mode withstanding capability and providing a wider SOA combined with a very low on-state resistance. The resulting MOSFET ensures the best trade-off between linear mode and switching operations.

Product status link
STH200N10WF7-2

Product summary	
Order code	STH200N10WF7-2
Marking	200N10WF7
Package	H²PAK-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C (1)	180	A
	Drain current (continuous) at T_C = 100 °C	150	A
I_{DM} (2)	Drain current (pulsed)	720	A
P_{TOT}	Total power dissipation at T_C = 25 °C	340	W
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	65	A
E_{AS}	Single pulse avalanche energy (T_J = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	840	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Current limited by package.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.44	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	35	°C/W

1. *When mounted on an 1 inch^2 FR-4 board, 2 oz of Cu, t < 10 s.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1mA	100			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS} = 100 V,T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 90 A		3.2	4.0	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz,V_{GS} = 0 V	-	4430	-	pF
C_{oss}	Output capacitance		-	3770	-	pF
C_{rss}	Reverse transfer capacitance		-	88	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 180 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	93	-	nC
Q_{gs}	Gate-source charge		-	52	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 90 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	40	-	ns
t_r	Rise time		-	230	-	ns
$t_{d(off)}$	Turn-off delay time		-	430	-	ns
t_f	Fall time		-	730	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 180 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	85		ns
Q_{rr}	Reverse recovery charge	I_{SD} = 180 A, di/dt = 100 A/µs	-	125		nC
I_{rr}	Reverse recovery current	V_{DD} = 80 V	-	2.9		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

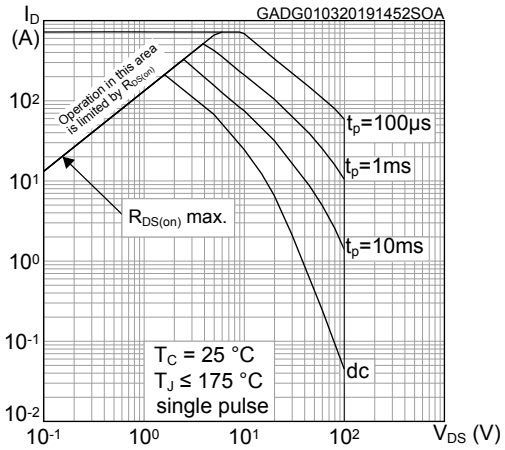


Figure 2. Normalized transient thermal impedance

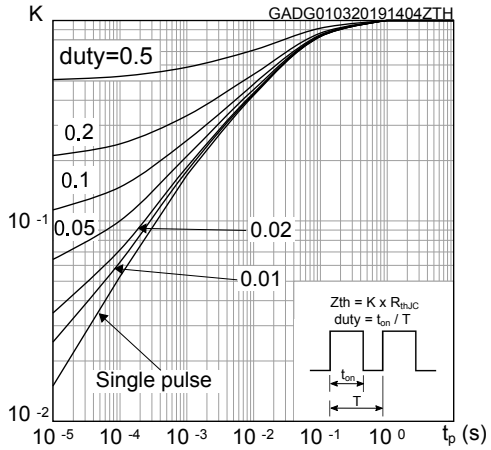


Figure 3. Typical output characteristics

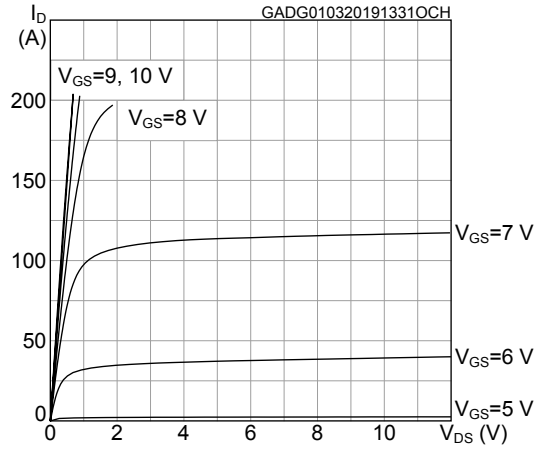


Figure 4. Typical transfer characteristics

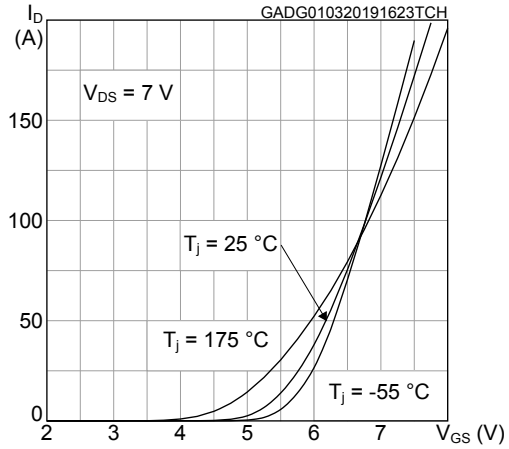


Figure 5. Typical gate charge characteristics

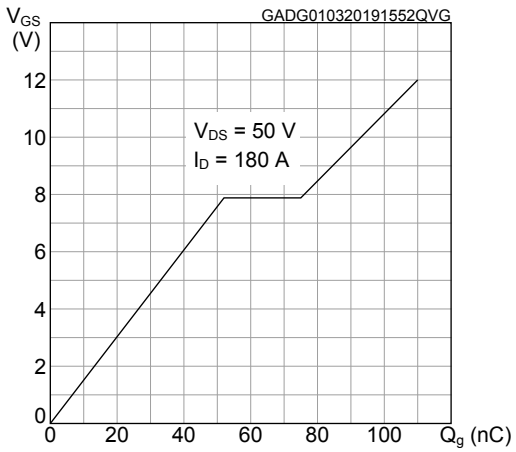


Figure 6. Typical drain-source on-resistance

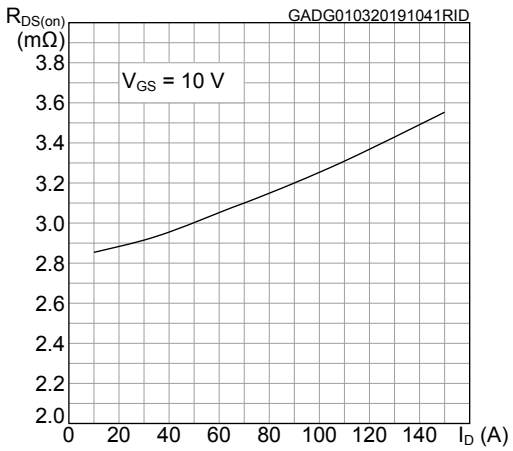


Figure 7. Typical capacitance characteristics

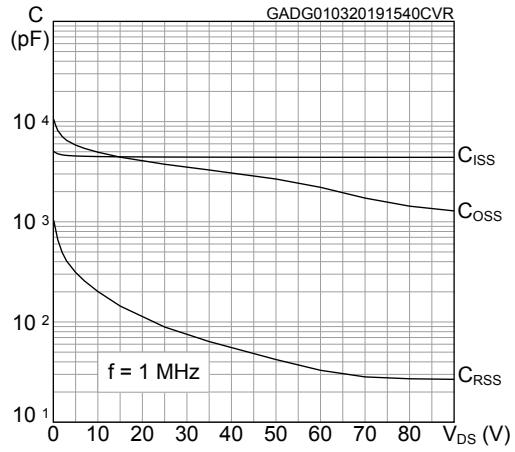


Figure 8. Normalized gate threshold vs temperature

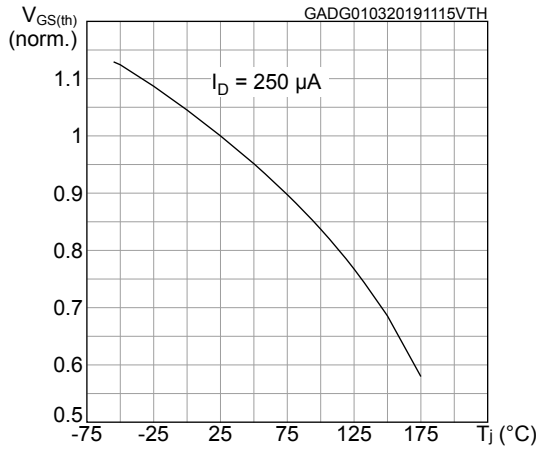


Figure 9. Normalized on-resistance vs temperature

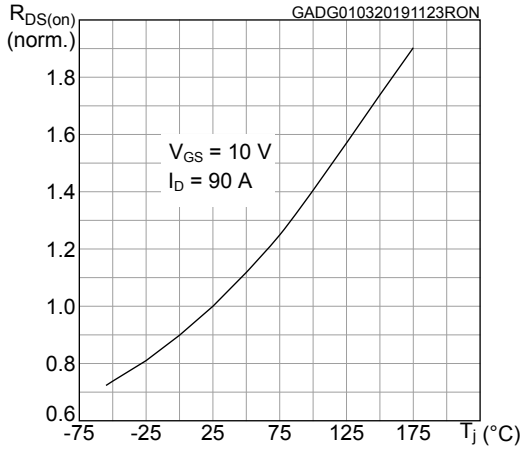


Figure 10. Normalized breakdown voltage vs temperature

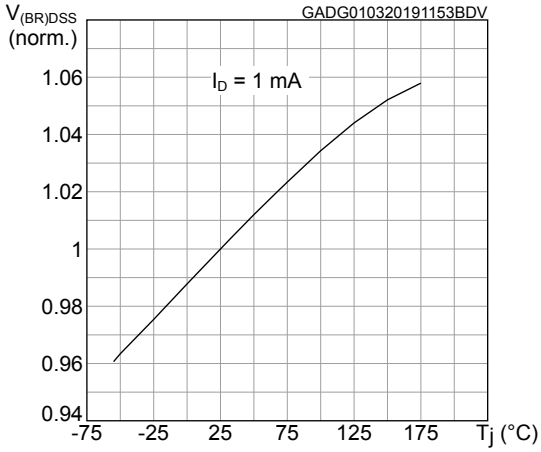
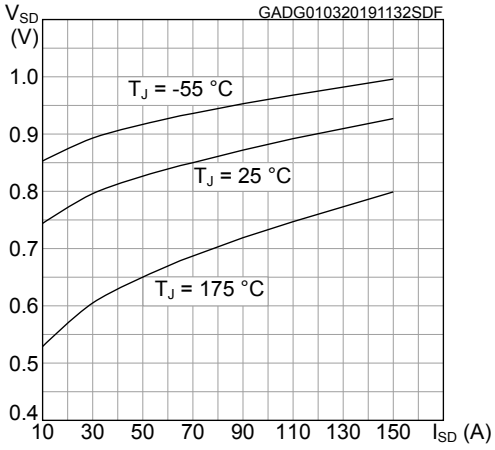


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

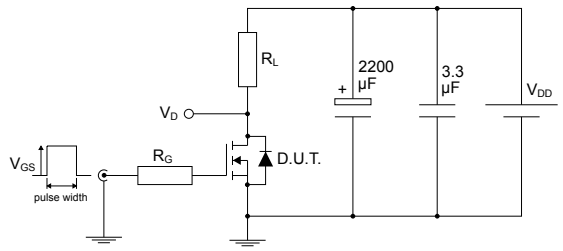


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Figure 13. Test circuit for gate charge behavior

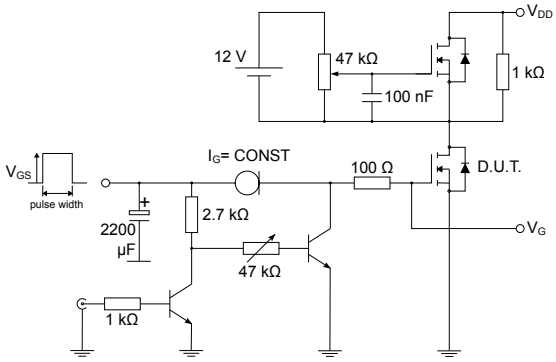

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Figure 14. Test circuit for inductive load switching and diode recovery times

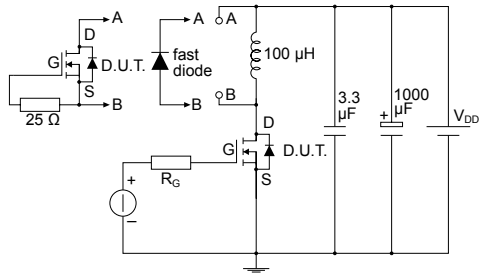

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Figure 15. Unclamped inductive load test circuit

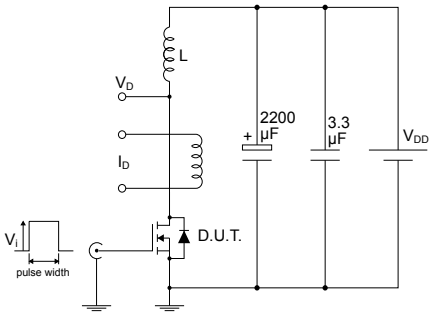

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Figure 16. Unclamped inductive waveform

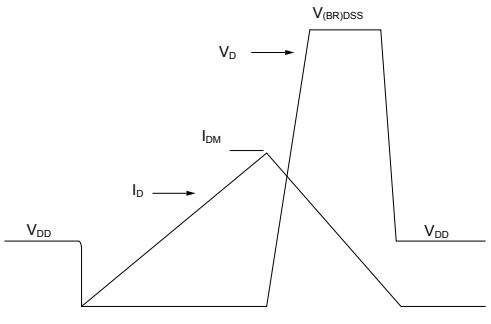

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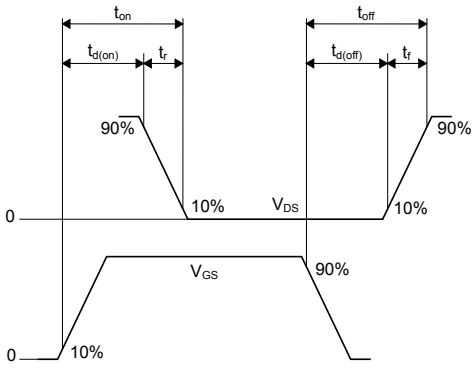
Figure 17. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 18. **H²PAK-2 package outline**

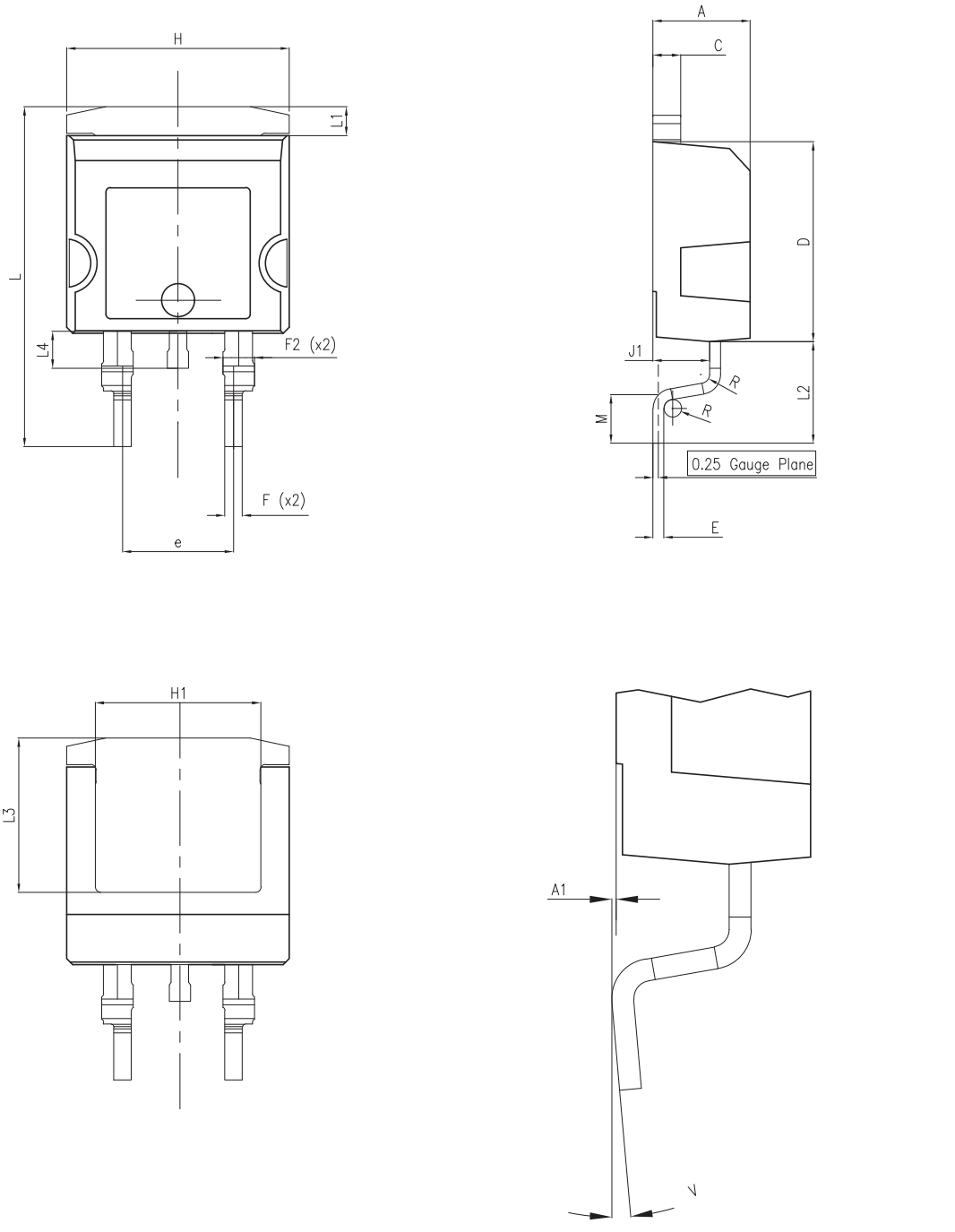

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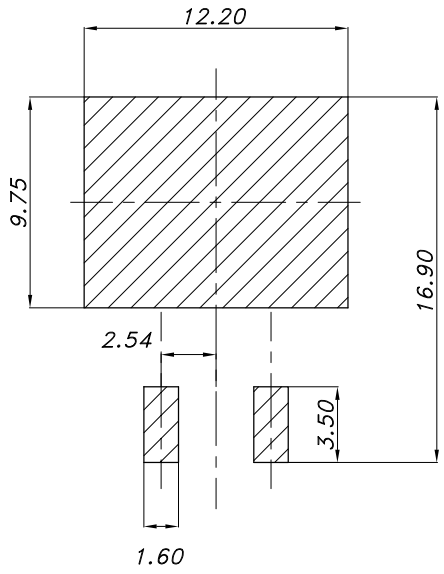
Table 7. **H²PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 19. **H²PAK-2 recommended footprint**



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Note: Dimensions are in mm.

4.2 Packing information

Figure 20. **Tape outline**

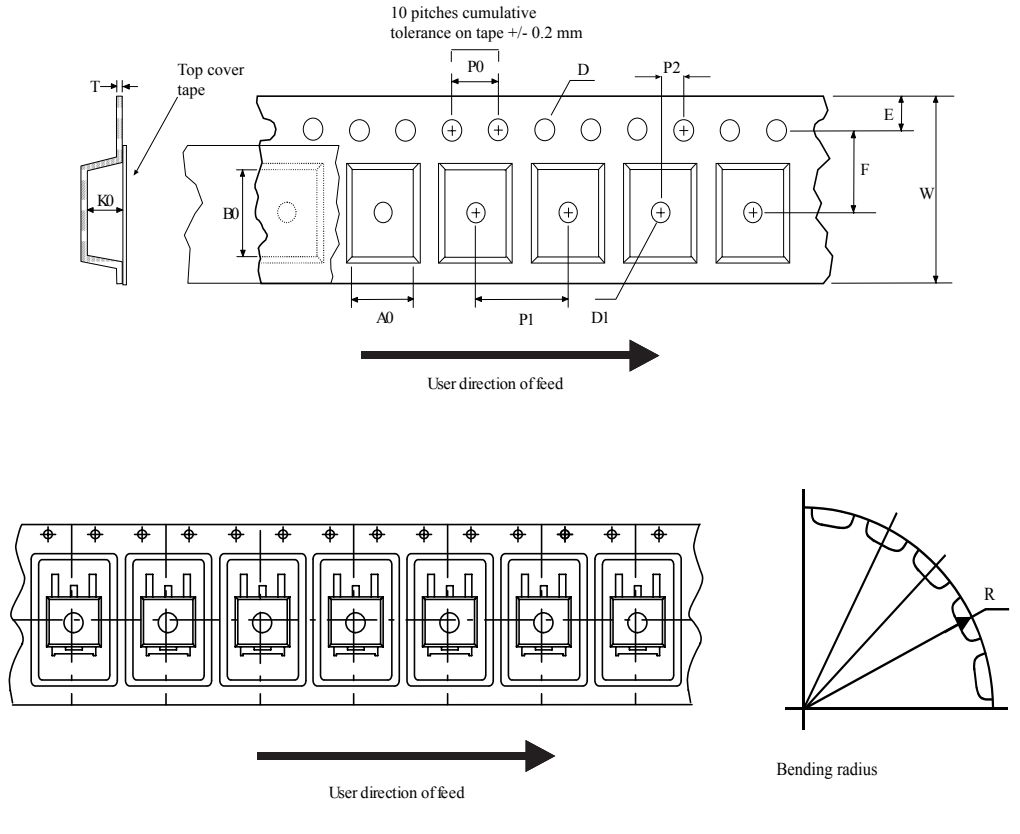

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Figure 21. **Reel outline**

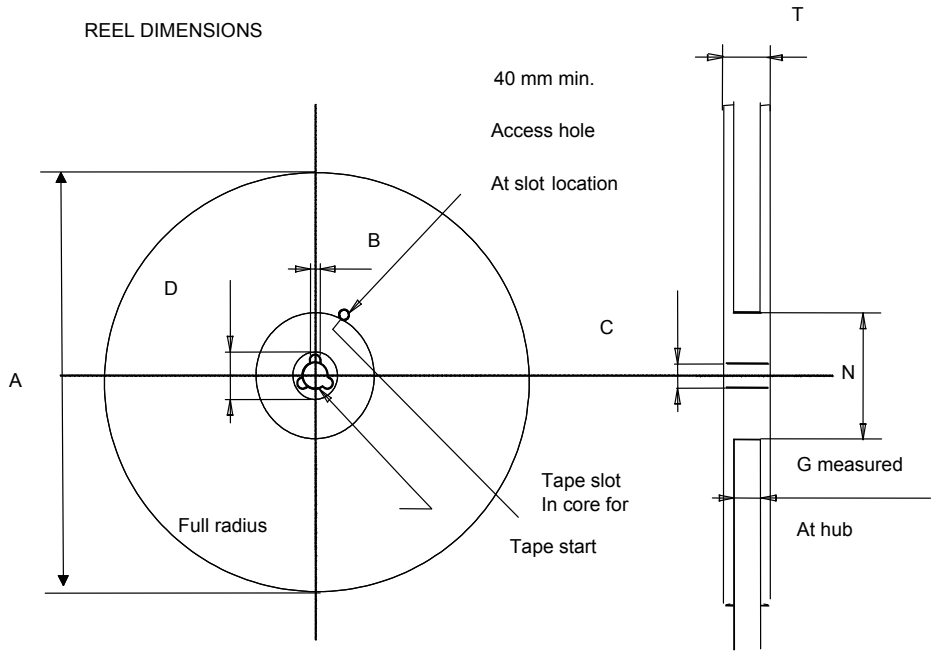

Table 8. **Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
22-Sep-2016	1	First release
07-Mar-2019	2	Updated *Table 4. Dynamic*, *Table 5. Switching time*s and *Table 6. Sourcedrain diode.*
09-Jul-2021	3	Modified Table 1. Absolute maximum ratings, Table 3. On /off-states, Table 4. Dynamic, Table 5. Switching times and Table 6. Source-drain diode. Modified Figure 1. Safe operating area, Figure 3. Typical output characteristics, Figure 4. Typical transfer characteristics, Figure 6. Typical drain-source on-resistance, Figure 7. Typical capacitance characteristics, Figure 9. Normalized on-resistance vs temperature and Figure 11. Typical reverse diode forward characteristics. Minor text changes.
13-Jul-2022	3	Updated Section Description.

Contents