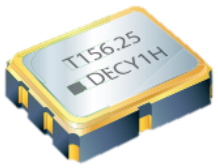
Product Features

1. Output Frequency :
   15~2100 MHz (LVPECL / LVDS /CML)
   15~700 MHz (HCSL)
2. Frequency Stability :
   ± 30 ppm @ (-40 ~ 85℃)
   ± 50 ppm @ (-40 ~ 105℃)
3. Supply Voltage : 1.8 , 2.5 , 3.3V (Typ.)
4. Output Type : LVPECL / LVDS / HCSL /CML
5. Phase Jitter :
   0.15fs (Typ.) @156.25MHz LVPECL, 25℃
6. High Power Supply Noise Rejection Performance
7. Industry Standard Package :
   7.0 x 5.0 x 1.7 mm (BC/BG/BX Series)
   5.0 x 3.2 x 1.2mm (CC/CG/CX Series)
   3.2 x 2.5 x 1.1 mm (DC/DG/DH Series)
   2.5 x 2.0 x 1.2 mm (EC Series)

Application :
- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch



RoHS COMPLIANT
REACH COMPLIANT
Pb Free
Halogen Free HF

Test condition
Ambient temperature : 25 ± 5℃
Relative humidity : 40% ~ 70%

- Table 1 . Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
LVPECL / LVDS / HCSL /CML Common Electrical Characteristics						
Nominal Frequency	F	15~2100			MHz	LVPECL / LVDS /CML
		15~700				HCSL
Frequency Stability	ST	± 30			ppm	@ -40~85℃ , Note 1
		± 50				@ -40~105℃ , Note 1
Operating Temperature	Topr	-40	-	85	℃	
		-40	-	105		
Supply Voltage	Vdd	1.8 , 2.5 , 3.3 (± 10%)			V	Note 2
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
LVPECL Electrical Characteristics						
Current Consumption	Icc	-	93	106	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	91	104	uA	OE = Low
Output Voltage High	VoH	VDD-1.165	-	VDD-0.8	V	
Output Voltage Low	VoL	VDD-2.0	-	VDD-1.555	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 3 , (Logic 1)
Enable Voltage Low	-	-	-	0.3VDD	V	Note 3 , (Logic 0)
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15~0.2	0.25	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note4

Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

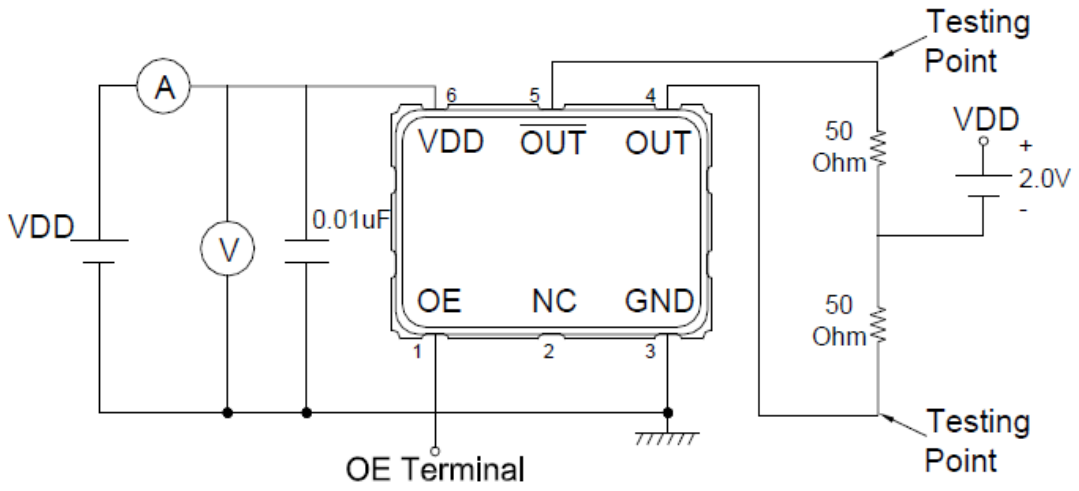
- Table 1 . Electrical Specifications (continued)

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
LVDS Electrical Characteristics						
Current Consumption	Icc	-	69	80	mA	RL=100Ω
Standby Current	Icc(ST)	-	67	78	uA	OE = Low
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	Vdiff	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 3
Enable Voltage Low	-	-	-	0.3VDD	V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15	0.25	ps	Integrated from 12KHz ~ 20MHz @150MHz , 3.3V , Note 4
HCSL Electrical Characteristics						
Current Consumption	Icc	-	-	30	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	10	uA	OE = Low
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 3
Enable Voltage Low	-	-	-	0.3VDD	V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.2	0.25	ps	Integrated from 12KHz ~ 20MHz @100MHz , 3.3V , Note 4
CML Electrical Characteristics						
Current Consumption	Icc	-	-	99	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	97	uA	OE = Low
Output Voltage High	VoH	VDD-0.085	VDD-0.01	VDD	mV	
Output Voltage Low	VoL	VDD-0.6	VDD-0.4	150	mV	
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 3
Enable Voltage Low	-	-	-	0.3VDD	V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.2	0.25	ps	@12KHz ~ 20MHz , Note 4

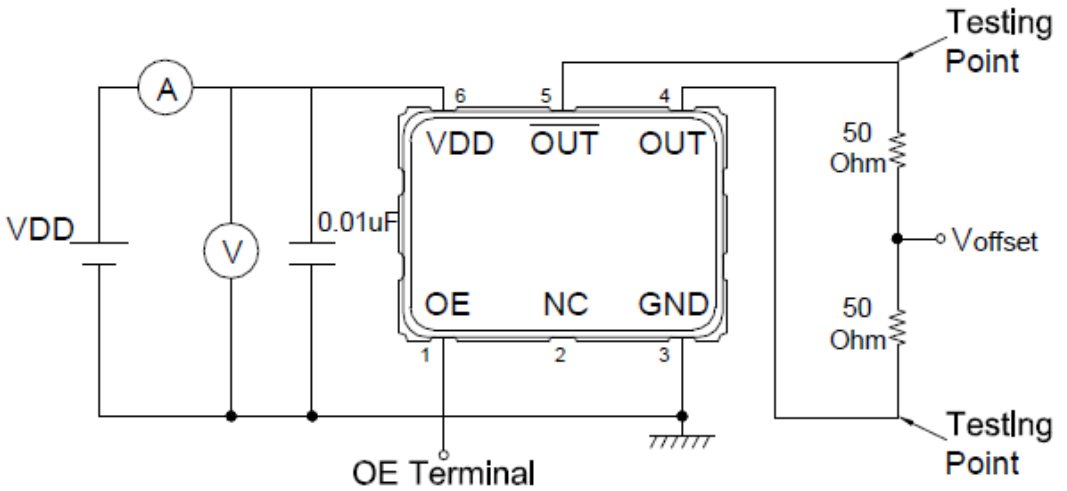
Note 1 : Inclusive of frequency tolerance at 25℃ , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : LVPECL can not support VDD 1.8V .
Note 3 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 4 : Phase Jitter will be slightly different according to output frequency and supply voltage.

- **Test Diagram**

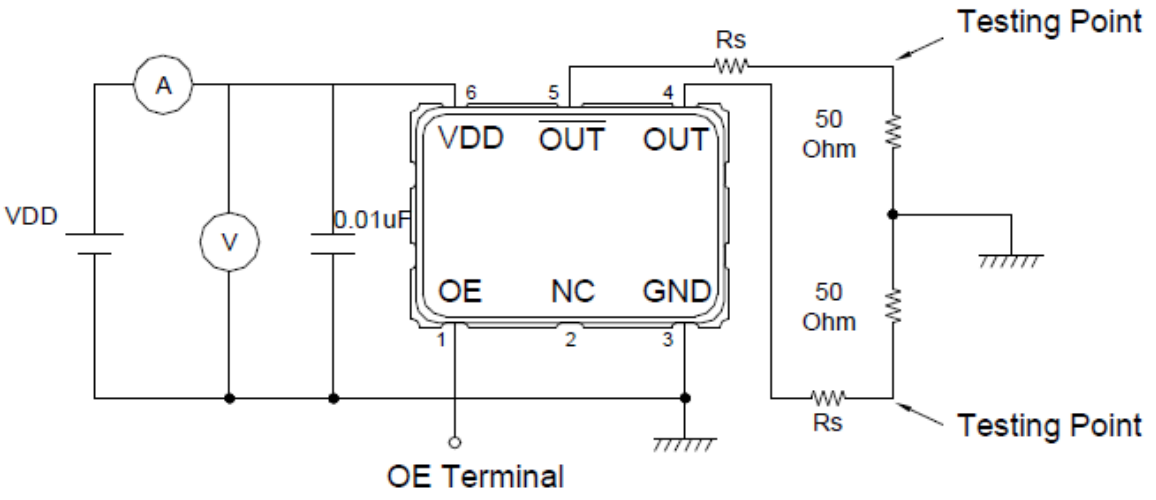
  - **LVPECL**



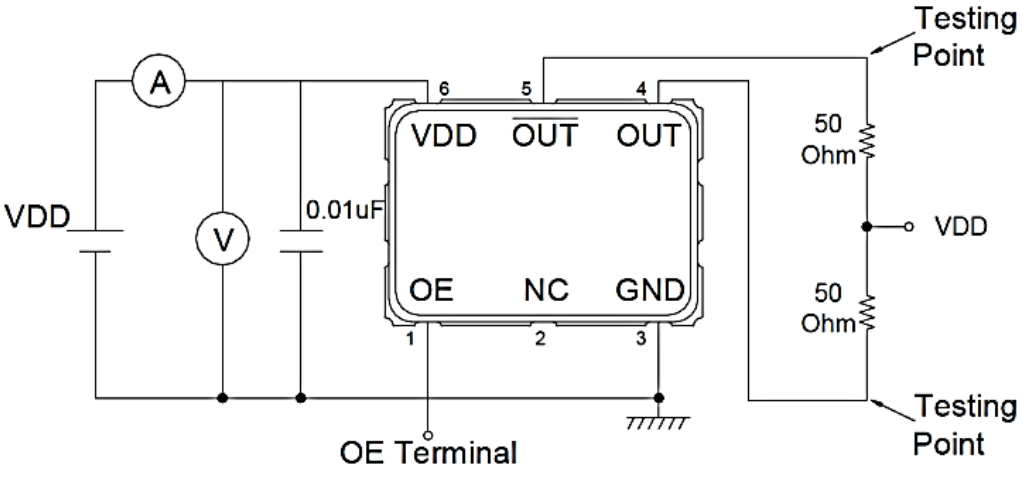
  - **LVDS**



  - **HCSL**



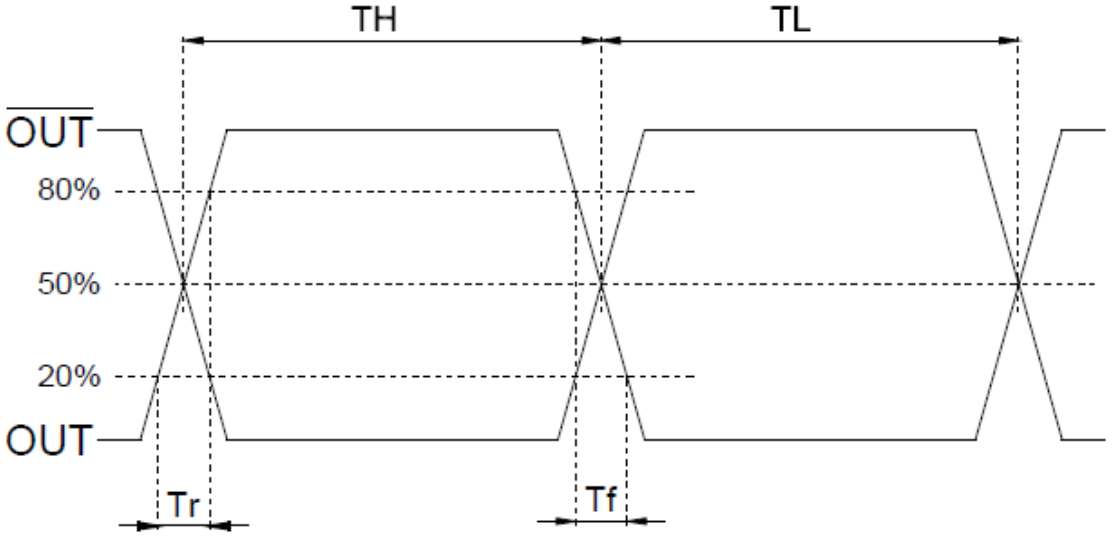
  - **CML**



Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All of the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.
4. HCSL RS= 0 Ohm for test. 0 Ohm to 33 Ohm to minimize overshoot and ringback effect in application.

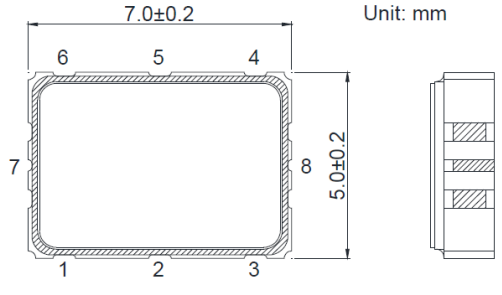
- Waveform Conditions

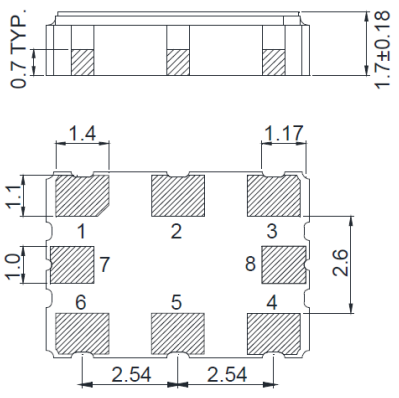


- Dimensions & Footprint(Recommended)

- **Size ： 7.0x5.0 mm**

LVPECL- BC Series
LVDS - BG Series
HCSL - BX Series



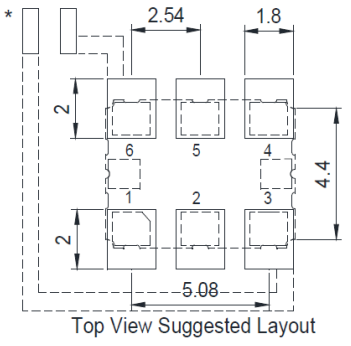


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD
7. NC
8. NC

Land Pattern:



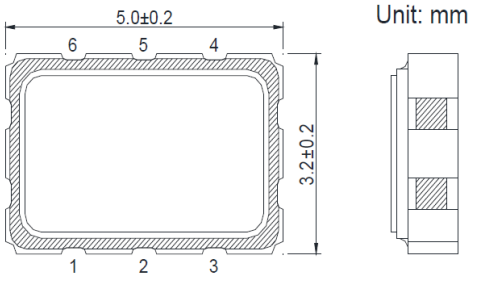
Top View Suggested Layout

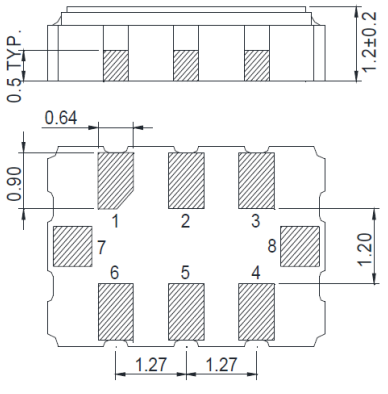
※ Power Supply Decoupling Capacitor is Required.

※ Pad dimension tolerance ±0.2 mm

- **Size ： 5.0x3.2 mm**

LVPECL- CC Series
LVDS - CG Series
HCSL - CX Series



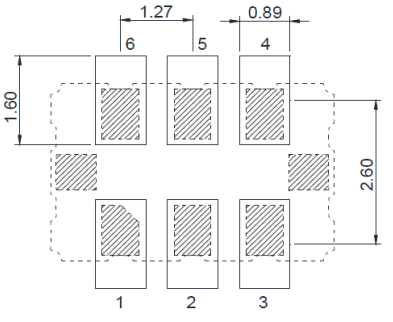


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD
7. NC
8. NC

Land Pattern:



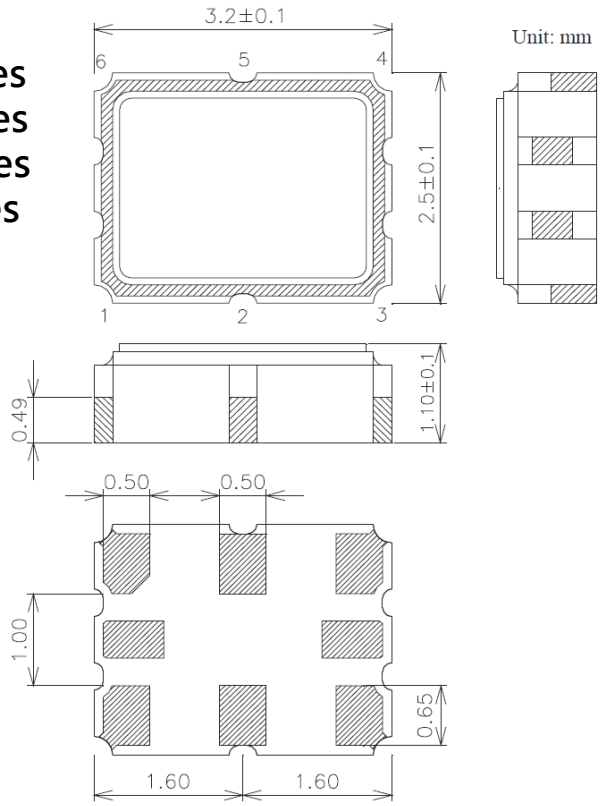
※ Power Supply Decoupling Capacitor is Required.

※ Pad dimension tolerance ±0.2 mm

- Dimensions & Footprint(Continued)

  - **Size ：3.2 x 2.5 mm**

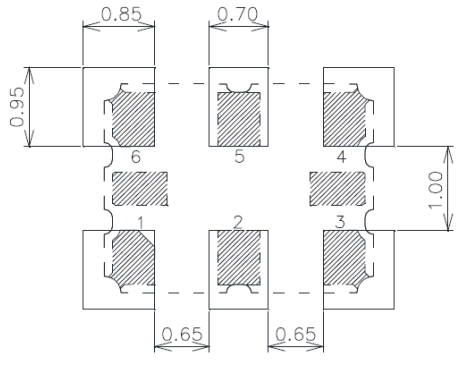
LVPECL- DC Series
LVDS - DG Series
HCSL - DH Series
CML - DL Series



Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD
7. NC
8. NC

Land Pattern:

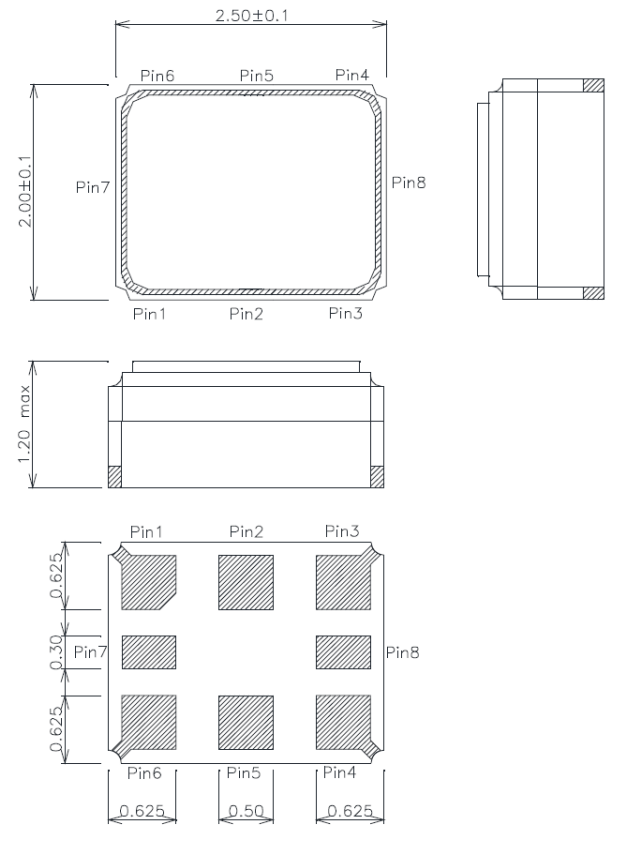


※ Pad dimension tolerance ±0.2 mm

※ Power Supply Decoupling Capacitor is Required.

  - **Size ： 2.5x2.0 mm**

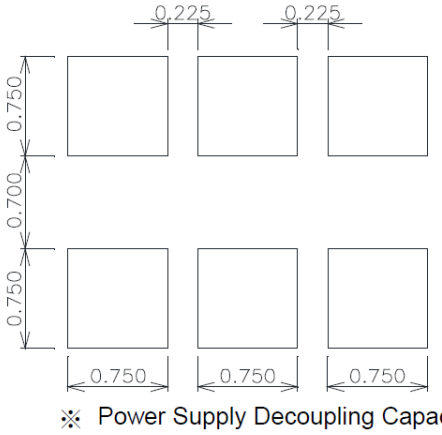
LVPECL- EC Series
LVDS - EC Series
HCSL - EC Series



Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD
7. NC
8. NC

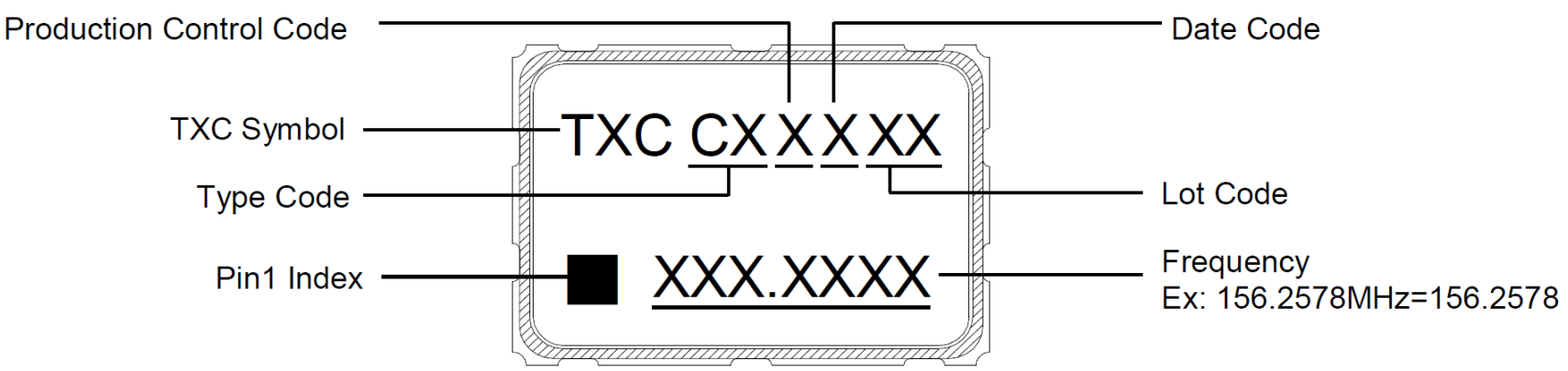
Land Pattern:



※ Pad dimension tolerance ±0.2 mm

※ Power Supply Decoupling Capacitor is Required.

- Marking



Date Code:

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z

*This date code will be cycled every four years

TYPE CODE

Oscillation mode	Fundamental	3rd Overtone	PLL
Code	CA	CB	CC

- Table 2 . Revision History

Rev.	Revise Contents	Release Date
A	Initial released	2022.09.05