

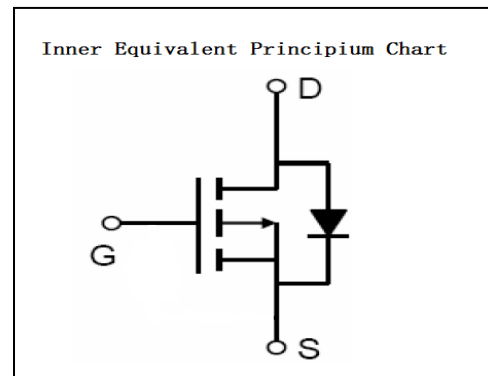
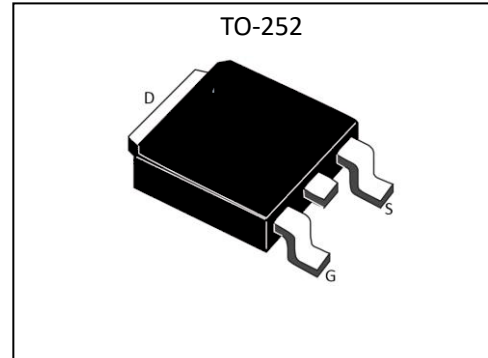
**Features:**

- $R_{DS(ON)} < 0.9\Omega$  @  $V_{GS}=10V$  (Typ0.7 $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

$V_{DSS}$	-200	V
$I_D$	-10	A
$P_D$	35	W
$R_{DS(ON)type}$	0.7	$\Omega$

**Applications:**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



**Absolute** ( $T_c= 25^\circ C$  unless otherwise specified) :

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-to-Source Voltage	-200	V
$I_D$	Continuous Drain Current	-10	A
$I_{DM}$	Pulsed Drain Current	-40	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$P_D$	Power Dissipation	35	W
$E_{AS}$	Single pulse avalanche energy <sup>a5</sup>	260	mJ
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ C$

**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified) :

<b>OFF Characteristics</b>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$V_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-200	--	--	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS}=-200V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1.0	$\mu A$
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	0.1	$\mu A$
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-0.1	$\mu A$

<b>ON Characteristics<sup>a3</sup></b>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=-10V, I_D=-5A$	--	0.7	0.9	$\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2	--	-4	V

Pulse width  $t_p \leq 380\mu s, \delta \leq 2\%$

<b>Dynamic Characteristics<sup>a4</sup></b>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$g_{fs}$	Forward Transconductance	$V_{DS}=-15V, I_D=-5A$	2	--	--	S
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=-25V$ $f=1.0\text{MHz}$	--	960	--	pF
$C_{oss}$	Output Capacitance		--	180	--	
$C_{rss}$	Reverse Transfer Capacitance		--	55	--	

<b>Resistive Switching Characteristics<sup>a4</sup></b>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-160V, I_D=-5A$ $V_{GS}=-10V, R_G=9.1\Omega$	--	22	--	ns
$t_r$	Rise Time		--	43	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	36	--	
$t_f$	Fall Time		--	27	--	
$Q_g$	Total Gate Charge	$V_{DD}=-100V, I_D=-10A$ $V_{GS}=-10V$	--	36	--	nC
$Q_{gs}$	Gate to Source Charge		--	18	--	
$Q_{gd}$	Gate to Drain ( "Miller" ) Charge		--	15	--	

**Source-Drain Diode Characteristics**

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$I_S$	Continuous Source Current <sup>a2</sup> (Body Diode)		--	--	-5	A
$V_{SD}$	Diode Forward Voltage <sup>a3</sup>	$I_S = -5A, V_{GS} = 0V$	--	--	-1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case <sup>a2</sup>	3.57	°C/W

<sup>a1</sup>: Repetitive Rating: Pulse width limited by maximum junction temperature.

<sup>a2</sup>: Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .

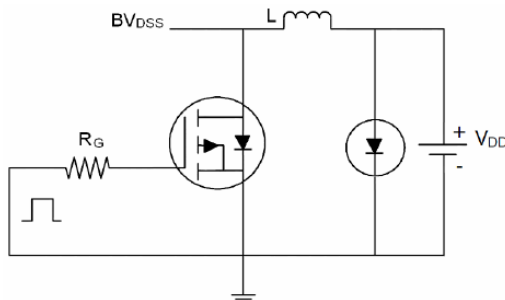
<sup>a3</sup>: Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

<sup>a4</sup>: Guaranteed by design, not subject to production

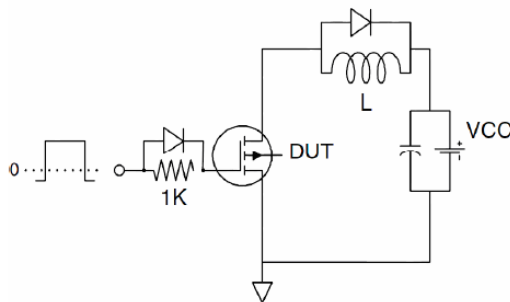
<sup>a5</sup>: EAS condition:  $T_j = 25^\circ\text{C}, V_{DD} = -50V, V_G = -10V, L = 0.5\text{mH}, R_g = 25\Omega$

**Test circuit**

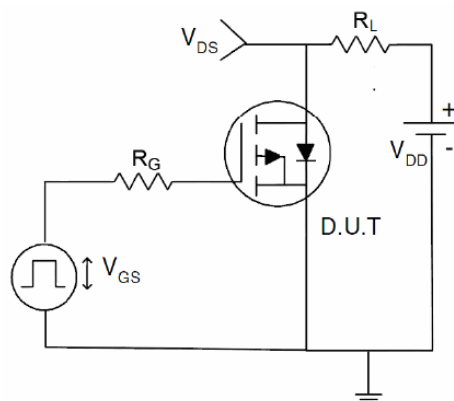
1) EAS Test Circuit



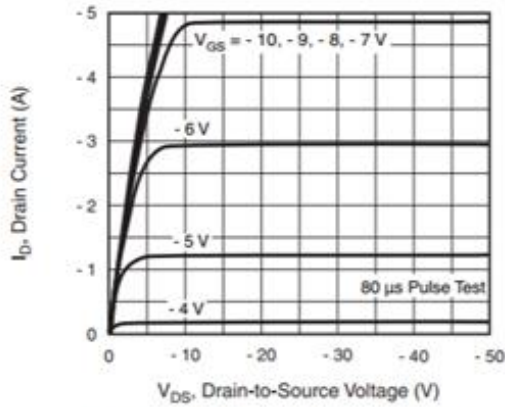
2) Gate Charge Test Circuit



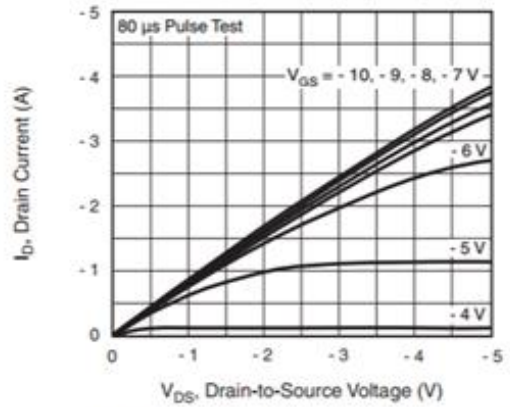
3) Switch Time Test Circuit



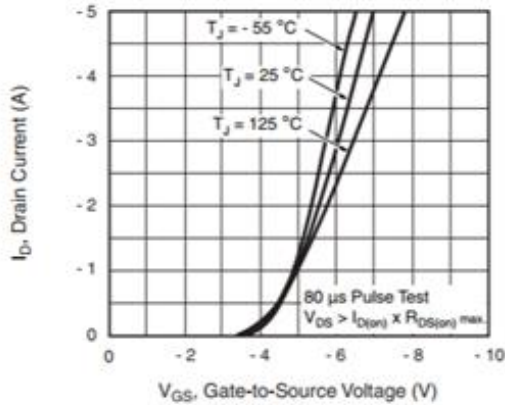
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



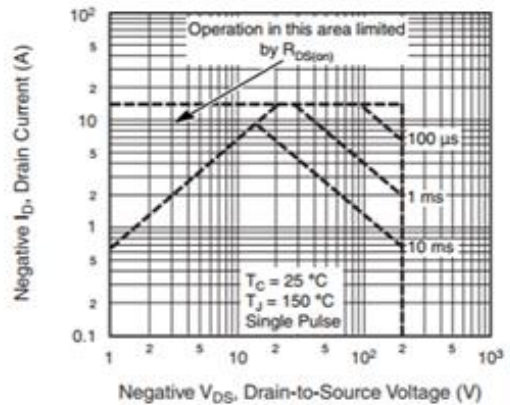
**Fig. 1 - Typical Output Characteristics**



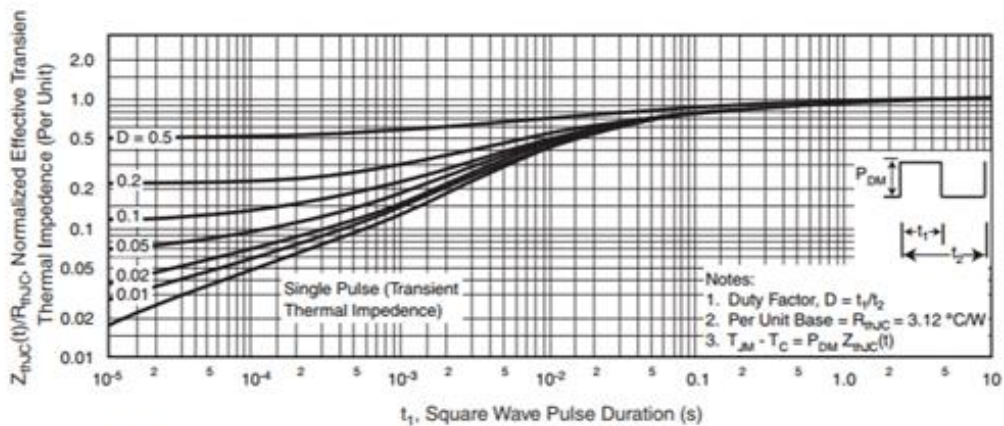
**Fig. 3 - Typical Saturation Characteristics**



**Fig. 2 - Typical Transfer Characteristics**



**Fig. 4 - Maximum Safe Operating Area**



**Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**

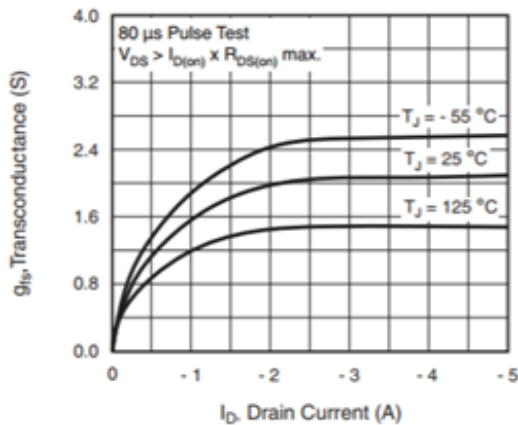


Fig. 6 - Typical Transconductance vs. Drain Current

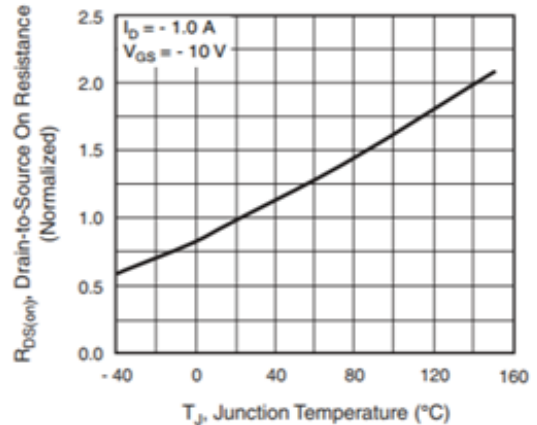


Fig. 9 - Normalized On-Resistance vs. Temperature

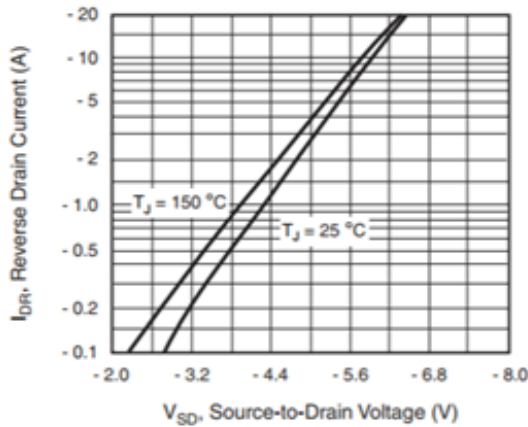


Fig. 7 - Typical Source-Drain Diode Forward Voltage

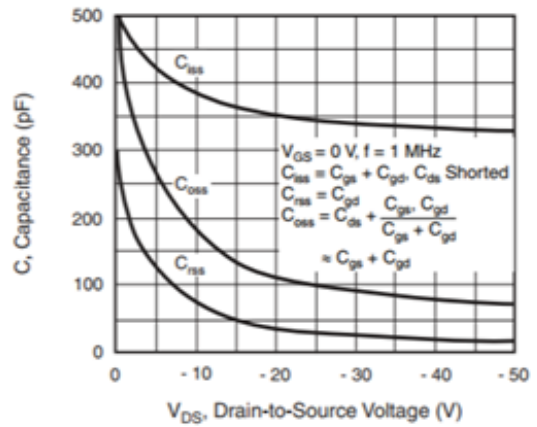


Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

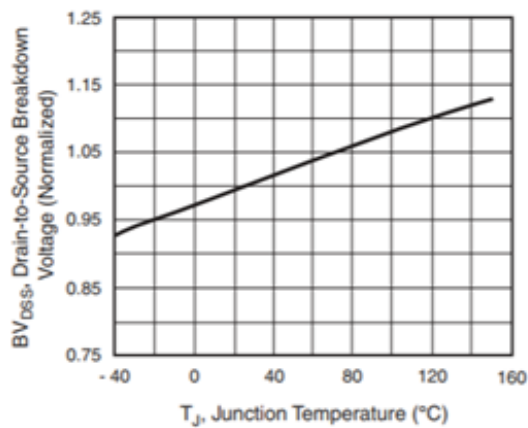


Fig. 8 - Breakdown Voltage vs. Temperature

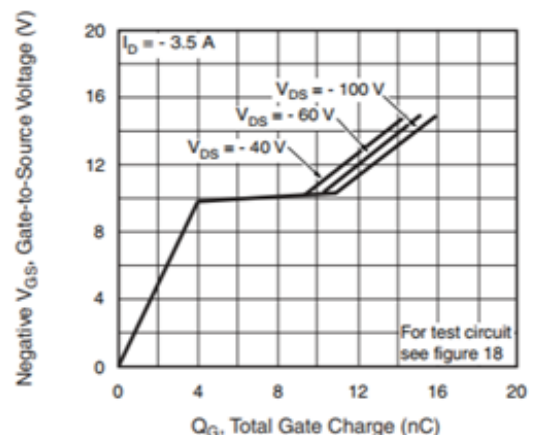


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

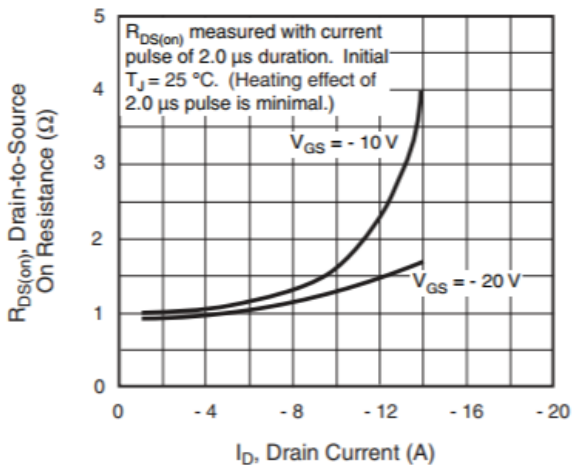


Fig. 12 - Typical On-Resistance vs. Drain Current

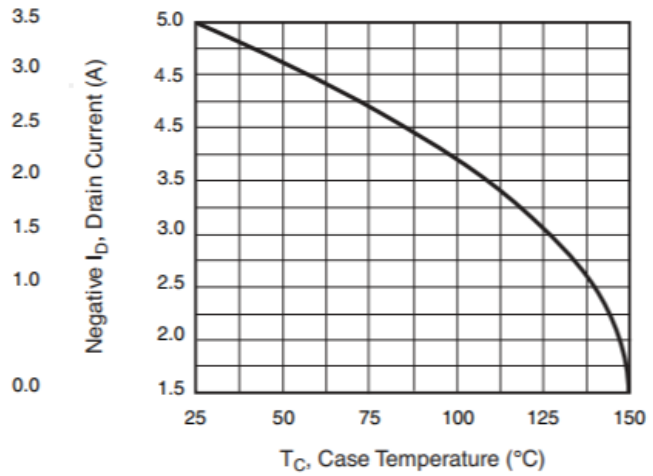


Fig. 13 - Maximum Drain Current vs. Case Temperature

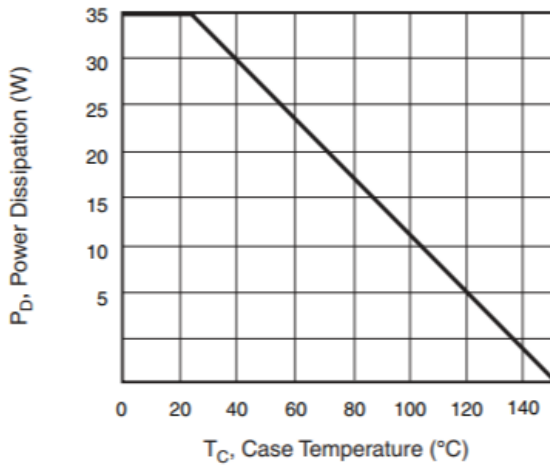


Fig. 14 - Power vs. Temperature Derating Curve