REAL -TIME CLOCK IC－SD2068 (V1.20)

1.General Description

The SD2068 is a CMOS type real-time clock which is connected to the CPU via 2-wires and capable of serial transmission of clock and calendar data to the CPU.

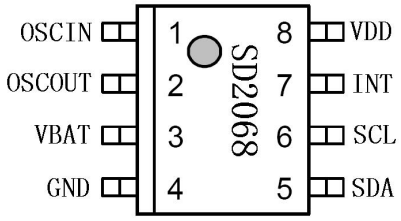
The SD2068 is dual power supply system. When the primary power supply goes down to an assigned value or resumes from low power, the system can switch between the primary power supply and battery automatically.

The SD2068 can generates various periodic interrupt clock pulses lasting for long period (one year), and three alarm interrupts can be made by year,month,date,days of the week, hours, and minutes.,seconds. It also provides a selectable 32.768KHz~1Hz clock output for an external MCU. The product incorporates a time trimming circuit that adjusts the clock with higher precision by adjusting any errors in crystal oscillator frequencies based on signals from the CPU. A 12-bytes general SRAM is implemented in the SD2068.

2.Features：

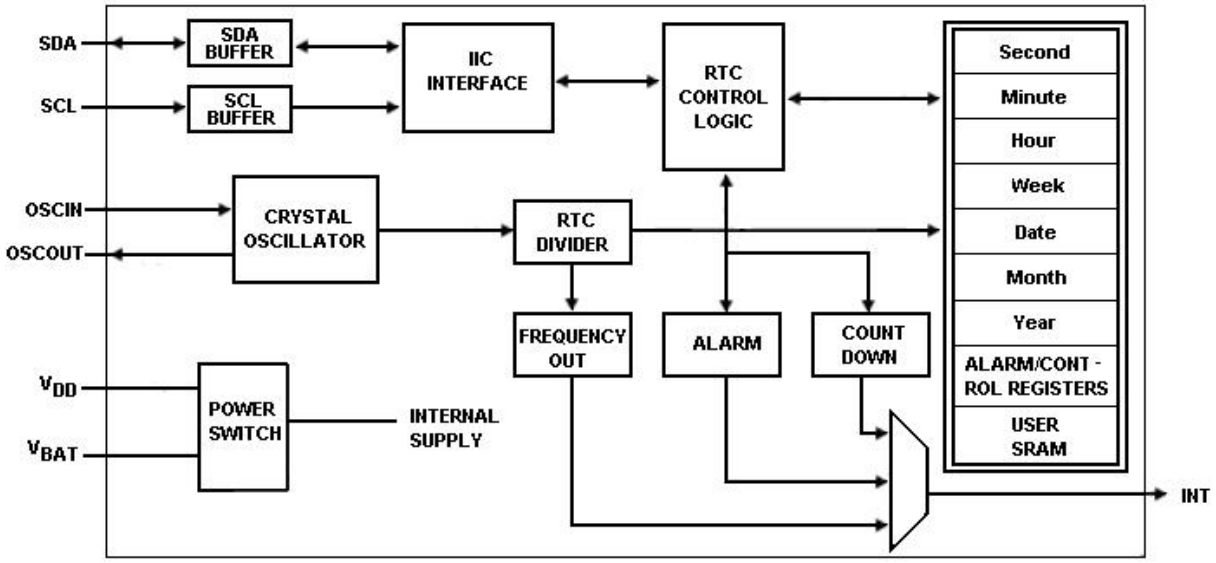
- Operation voltage range:1.8V~5.5V.
- Low-power:typical 1uA at 3.0V.
- Fast (400kHz) I^2C Interface.
- Real-Time Clock Counts Seconds, Minutes,Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Up to 2100.
- Time-of-Year,Month,Day,Week,Hour,Minute,Second Alarms.
- Programmable Square-Wave Output:32768hz,4096hz...1hz..1/16hz.
- 8-bit countdown timer, optional 4 clock sources (4096HZ, 64HZ, 1HZ, 1/60HZ)
- High precision time trimming circuit.
- 12-houe/24-huor time display selectable.
- 12 bytes general SRAM implemented for system data backup.
- CMOS logic
- ROHS Recognized.
- Package: SOP8/TSSOP8

3.Pin Configuration



NAME	FUNCTION
SCL	Serial Clock Input. This pin is the clock input for the I²C serial interface and is used to synchronize data movement on the serial interface. Up to 5.5V can be used for this pin, regardless of the voltage on VCC.
SDA	Serial Data Input/Output. This pin is the data input/output for the I²C serial interface. This open-drain pin requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on VCC.
INT	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor connected to a supply at 5.5V or less. If not used, this pin can be left floating.
VBAT	External Battery input pin.
OSCIN	The input of the interal oscillator
OSCOUT	The output of the interal oscillator
VCC	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1μF to 1.0μF capacitor.
GND	Ground

4.Block Diagram



5.Registers

5.1 Table of the RTC registers

Add.	Register bank	Register name	BIT								Value (DEC)	Default (BIN)
			D7	D6	D5	D4	D3	D2	D1	D0		
00H	Real time clock registres	Second	0	S40	S20	S10	S8	S4	S2	S1	0-59	XXXX-XXXX
01H		Minute	0	MN40	MN20	MN10	MN8	MN4	MN2	MN1	0-59	XXXX-XXXX
02H		Hour	12_/24	0	H20 P/A_	H10	H8	H4	H2	H1	0-23	XXXX-XXXX
03H		Week	0	0	0	0	0	W4	W2	W1	0-6	XXXX-XXXX
04H		Day	0	0	D20	D10	D8	D4	D2	D1	1-31	XXXX-XXXX
05H		Month	0	0	0	MO10	MO8	MO4	MO2	MO1	1-12	XXXX-XXXX
06H		Year	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	0-99	XXXX-XXXX
07H	Time alarm registres	Second alarm	0	AS40	AS20	AS10	AS8	AS4	AS2	AS1	0-59	0000-0000
08H		Minute alarm	0	AMN40	AMN20	AMN10	AMN8	AMN4	AMN2	AMN1	0-59	0000-0000
09H		Hour alarm	0	0	AH20 AP/A_	AH10	AH8	AH4	AH2	AH1	0-23	0000-0000
0AH		Week alarm	0	AW6	AW5	AW4	AW3	AW2	AW1	AW0	N/A	0000-0000
0BH		Day alarm	0	0	AD20	AD10	AD8	AD4	AD2	AD1	1-31	0000-0000
0CH		Mouth alarm	0	0	0	AMO10	AMO8	AMO4	AMO2	AMO1	1-12	0000-0000
0DH		Year alarm	AY7	AY6	AY5	AY4	AY3	AY2	AY1	AY0	0-99	0000-0000
0EH		Alarm enable	0	EAY	EAMO	EAD	EAW	EAH	EAMN	EAS	N/A	0000-0000
0FH	Control registers	CTR1	WRTC3	0	INTAF	INTDF	0	WRTC2	0	RTCF	N/A	0000-0000
10H		CTR2	WRTC1	IM	INTS1	INTS0	FOBAT	INTDE	INTAE	INTFE	N/A	0000-0000
11H		CTR3	ARST	0	TDS1	TDS0	FS3	FS2	FS1	FS0	N/A	0000-0000
12H		TTF	0	F6	F5	F4	F3	F2	F1	F0	N/A	0000-0000
13H		Count down	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	0-255	0000-0000
14~ 1FH	General RAM	(12Bytes)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	N/A	XXXX-XXXX

5.2 Real Time Clock Registers [00h to 06h]

These RTC (Real time clock)registers are stored as binary-coded decimal (BCD) format.

Seconds and Minutes: range from 0 to 59;

Hour :can be set 12-hour or 24-hour mode;

day :from 1 to 31,Month :from1 to 12, Year :from 0 to 99;

Day of the Week:from 0 to 6.

24 HOUR TIME

If 12_/24 bit of the Hour register is “1”, the RTC uses a 24-hour format. If the 12_/24 bit is “0”, the RTC uses a 12-hour format

Note:

1. You must clear the hour's highest bit 12_/24 after you have gotten the data from the hour register, otherwise it will be incorrect when the time is P.M.
2. After power on reset, the real time clock data registers aren't cleaned or set to be "1".
3. When writing the real time data into RTC registers(00H ~ 06H), you must write all of the total seven bytes data one time .

5.3 Interrupt Control Register [07h to 13h]

The SD2068 have three different interrupts and are controlled by these bits of the INTAE, INTFE, INTDE :

No.	Interrupt enable bit (1=enable,0=disable)	Interrupt name	Interrupt flag (1=Yes,0=No)
1	INTAE	Alarm Interrupt	INTAF
2	INTFE	Frequency Interrupt	-
3	INTDE	Countdown timer interrupt	INTDF

When the alarm interrupt is generated, the interrupt flag INTAF bit is set to 1; when the countdown interrupt is generated, interrupt flag INTDF bit is set to 1; if the flag bits is set to 1, it need to clear by progarm. Frequency interrupt hasn't any flag.

The three interrupts used one output pin INT.The INT output is selected via INTS0、INTS1 which are the control register bits of the control register(CTR2).

No.	INTS1	INTS0	Function
0	0	0	Disable output
1	0	1	Alarm Interrupt
2	1	0	Frequency Interrupt
3	1	1	Countdown timer interrupt

(1) Alarm Interrupt

The alarm interrupt is enabled via the INTAE bit, and the alarm time data include second,minute,hour, day, week, month and year are stored in time alarm registers(07h~ 0Dh).

Note:the highest bit of hour alarm register(09h) must be clear to logic "0" all the time.

Real time alarm enable register is 0EH:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	0	EAY	EAMO	EAD	EAW	EAH	EAMN	EAS
Alarm enable	-	Year (0Dh)	Month (0Ch)	Day (0Bh)	Week (0Ah)	Hour (09h)	Minute (08h)	Second (07h)

Note:1=enable ,0=disable.

When one or more of the alarm registers are loaded with a valid second,minute, hour, day ,week,month,year and its corresponding alarm enable bit is a logic 1, then that information will be compared with the current second,minute, hour, day ,week,month,year, When all enabled comparisons first match, the bit INTAF (Alarm flag) is set.

Note:

1. When the week alarm and the date alarm are both enable at the same time, only the date alarm is valid and the week alarm is invalid.
2. Week alarm register data's format is different from real-time clock week data format. The bit of Week alarm register AW6.AW5.AW4.AW3.AW2.AW1.AW0 is respectively indicated Saturday, Friday, Thursday, Wednesday, Tuesday, Monday, Sunday. For example, AW6, AW1 = 1, and other bits are clear to 0, alarm interrupt will be output from INT pin on Monday and Saturday.

The INTAF bit will automatically be cleared when the alarm enable register is written . The alarm interrupt output function is selected by setting the INTS1 bit to “0”,theINTS0 bit to “1”,

The alarm function can be set in either single event alarm mode or periodic interrupt alarm mode (seclcted by IM bit).

IM	Alarm interrupt mode	INT
0	single event alarm	Remain low until the INTAF bit is reset
1	periodic interrupt alarm	Periodic pulse until the INTAF bit is reset

(2) Frequency interrupt

The frequency interrupt is enabled by setting the INTFE bit to “1” .The signal frequency can be selected by the FS3, FS2, FS1, FS0 bits in the register CTR3:

frequency(HZ)	FS3	FS2	FS1	FS0
0	0	0	0	0
32768	0	0	0	1
4096	0	0	1	0
1024	0	0	1	1
64	0	1	0	0
32	0	1	0	1
16	0	1	1	0
8	0	1	1	1
4	1	0	0	0
2	1	0	0	1
1	1	0	1	0
1/2	1	0	1	1
1/4	1	1	0	0
1/8	1	1	0	1
1/16	1	1	1	0
1S	1	1	1	1

(3)Countdown timer interrupt

The countdown timer interrupt is enabled and disabled via the timer control register bit INTDE.The frequency source is selected by the TDS1, TDS0 bits in the control register 3(CTR3).

TDS1	TDS0	Source clock(HZ)
0	0	4096
0	1	64
1	0	1
1	1	1/60

When countdown timer interrupt is enabled and an 8-bit binary countdown data is written into the countdown timer, the countdown timer will reduce according to the source clock. If the countdown timer reduce to zero,The countdown interrupt flag will be set (control register 1 bit INTDF) to “1” immediately . The longest period of the countdown timer interrupt is 256 minutes.

5.4 Time Trimming Register [12h]

D7	D6	D5	D4	D3	D2	D1	D0
0	F6	F5	F4	F3	F2	F1	F0

For the following reasons:

1) In general crystal oscillators are classified by their central frequency of CL (load capacitance) and available further grouped in several ranks as ±10，±20 and ±50ppm of fluctuations in precision.
2) The fluctuation of IC circuit frequency is ±5~10ppm at room temperature.
3) Here, the clock accuracy at room temperature varies along with the variation of the characteristic of crystal oscillator.
4) The influence of stray capacitance on circuit board

These factors will cause large errors

Using the time trimming circuit gain or lose of clock may be adjusted with high precision by changing clock pulses for one second every 20 seconds.

F6 to F0:

The time trimming circuit adjust one second count based on this register readings when second digit is 00，20，or 40 seconds. Normally, counting up to seconds is made once per 32,768 of clock pulse (or 32,000 when 32.000KHz crystal is used) generated by the oscillator. Setting data to this register activates the time trimming circuit.

Register counts will be incremented as ((F5, F4, F3, F2, F1, F0)-1) x2 when F6 is set to “0”.

Register counts will be decremented as ((/F5, /F4, /F3, /F2, /F1, /F0) +1) x2 when F6 is set to “1”.

Counts will not change when (F6, F5, F4, F3, F2, F1, F0) are set to (*, 0, 0, 0, 0, 0, *).

For example, when 32.768KHz crystal is used.

When (F6, F5, F4, F3, F2, F1, F0) are set to (0,1, 0, 1, 0, 0, 1), counts will change as: 32768+（29-1）*2=32824 (clock will be delayed) when second digit is 00, 20, or 40.

When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32,768 without changing when second digit is 00, 20, or 40.

When (F6, F5, F4, F3, F2, F1, F0) are set to (1, 1, 1, 1, 1, 1, 0), counts will change as: 32768-（1+1）*2=32764 (clock will be advanced) when second digit is 00, 20, or 40.

Adding 2 clock pulses every 20 seconds: 2/（32768*20）=3.051ppm (or 3.125ppm when 32.000KHZcrystal is used), delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of±1.5ppm.

Note: that the time trimming function only adjusts clock timing and oscillation frequency but 32.768KHz clock output is not adjusted

Computational method of time trimming register value

1. When oscillation frequency [*1] > target frequency [*2]（clock gain）

$$\text{Adjustment amount}^{*3} = \frac{(OscilationFrequency - T\arg etFrequency + 0.1)}{OscillationFrequency * 2 / (T\arg etFrequency * 20)}$$

$$= (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

*1) Oscillation frequency: Clock frequency output from the INT pin

*2) Target frequency: TYP. 32.768KHz to 32.000KHz

*3) Adjustment amount: A value to be set finally to F6 to F0 bits. This value is expressed in 7 bit binary digits with sign bit (two’s compliment).

2. When oscillation frequency = target frequency (no clock gain or loss)

Set the adjustment value to 0 or +1, or –64, or –63 to disable adjustment.

3. When oscillation frequency < target frequency (clock losses)

$$\text{Adjustment amount} = \frac{(OscilationFrequency - T\arg etFrequency)}{OscillationFrequency * 2 / (T\arg etFrequency * 20)}$$

$$= (\text{Oscillation frequency} - \text{Target frequency}) \times 10$$

Example of Calculations

1) When oscillation frequency = 32770kHz; target frequency = 32768kHz

Adjustment value = （32770-32768+0.1）/(32770*2/(32768*20))

=(32770-32768)*10+1=21

Set （F6，F5，F4，F3，F2，F1，F0）=（0，0，1，0，1，0，1）

2) When oscillation frequency =32762kHz; target frequency = 32768kHz

Adjustment value =（32762-32768）/(32762*2/(32768*20))

= (32762-32768)*10=-60

To express –60 in 7bi binary digits with sign bit (two's compliment)

Subtract 60(3Ch) from 128(80h) in the above case, 80h-3Ch=44h

Thus set （F6，F5，F4，F3，F2，F1，F0）=（1，0，0，0，1，0，0）

After adjustment, adjustment error against the target frequency will the approx. ±1.5ppm at a room temperature.

Notice:

1) Clock frequency output from the INT pin will change after adjustment by the clock adjustment circuit.

2) Adjustment range:

A)When oscillation frequency is higher than target frequency, the range of adjustment values is （F6，F5，F4，F3，F2，F1，F0）=（0，0，0，0，0，0，1）to (0，1，1，1，1，1，1) and actual adjustable amount shall be -3.05ppm to –189.2ppm (-3.125ppm to 193.7ppm for 32000Hz crystal).

B) When oscillation frequency is lower than target frequency, the range of adjustment values is （F6，F5，F4，F3，F2，F1，F0）=（1，1，1，1，1，1，1）to（1，0，0，0，0，1，0）and actual adjustable amount shall be 3.05ppm to 189.2ppm (3.125ppm to 193.7ppm for 32000Hz crystal).

5.5 User Registers

Addresses [14h to 1Fh]

SD2068 provides 12 bytes of general-purpose RAM for the user to store data.

5.6 Other control / status bits

(1) **WRITE RTC ENABLE BIT (**WRTC1 ,WRTC2,WRTC3):

Registers (00H ~ 1FH) RTC write enable bits. When the three bits are set to "1", RTC is enable to be written.

Write enable: Setting the three bits must follow the sequencing: Set the WRTC1 bit to "1" first, then set the WRTC2 and WRTC3 to "1".

Write disable: Setting the three bits must follow the sequencing: Set the WRTC2 and WRTC3 bits to "0" first, then set the WRTC1 to "0".

(2) **AUTO RESET ENABLE BIT** (ARST): Enables/disables the automatic reset of the INTAF and INTDF status bits . When ARST bit is set to "1", these status bits are reset to "0" after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to "0", the user must reset the INTAF and INTDF bits.by your program

(3) **FREQUENCY OUTPUT AND INTERRUPT BIT** (FOBAT): This bit is used for enables/disables the INT pin during battery backup mode (i.e. VBAT power source active). When the FOBAT is set to “1” the INT pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBAT is cleared to “0”, the INT pin is enabled during battery backup mode.

(4) **POWER ON BIT (**RTCF): when the dual power(both Vdd add Vbat) reset,the RTCF bit will be set to “1” . this bit can be read only.

6. I2C Serial Interface

The SD2068 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the SD2068 operates as a slave device in all applications.

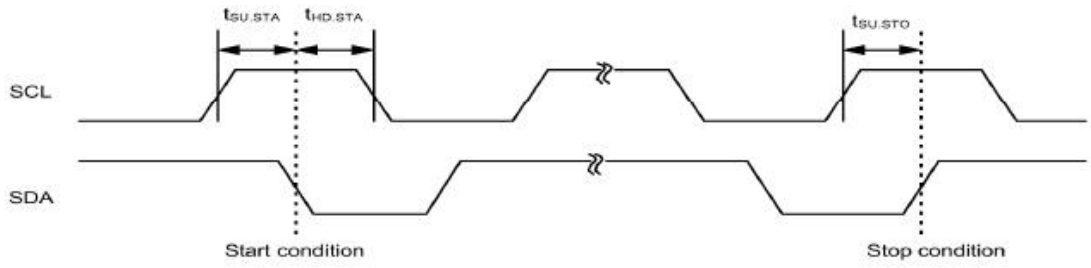
6.1 **Protocol Conventions**

(1) Start condition

The SCL and SDA pins are at the “H” level when no data transmission is made. Changing the SDA from “H” to “L” when the SCL and the SDA are “H” activates the start condition and access is started.

(2) Stop condition

Changing the SDA from “L” to “H” when the SCL is “H” activates stop condition and accessing stopped.



VALID START AND STOP CONDITIONS

(3) Data valid:

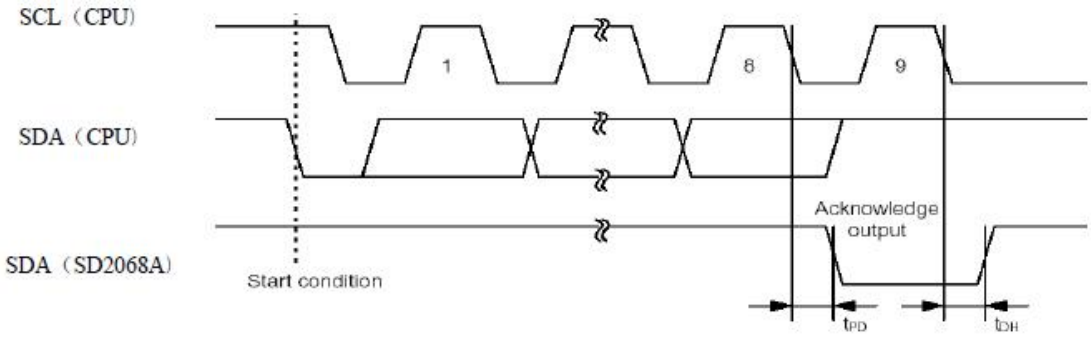
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

(4) Acknowledge:

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data.

The SD2068 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The SD2068 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.



VALID DATA CHANGES, AND ACKNOWLEDGE RESPONSE FROM RECEIVER

6.2 The transmission format of data/command

(1)Device address

The high effective 7 bits (bit7---bit1) in the address byte are defined as device type ID. In SD2068, these 7 bits are 0110010. The lowest bit0 is defined as R/W mode. When this bit is “1”, it is read mode, while “0” is write mode.

The slave address:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	1	1	0	0	1	0	R/W

BIT7—BIT1：The slave address of the SD2068 is defined as 0110010

BIT0： R/W definition

“1” is read mode.

“0” is write mode.

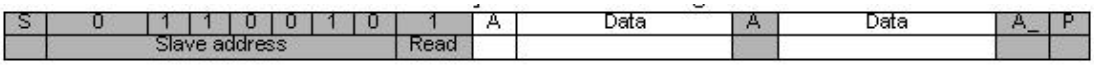
(2) Data transmission format

At the end of data transmission/receiving stop condition is generated to complete transmission. However, if start condition is generated without generating stop condition, repeated start condition is met and transmission/receiving data may be continued by setting the slave address again. Use this procedures when the transmission direction needs t be changed during one transmission.

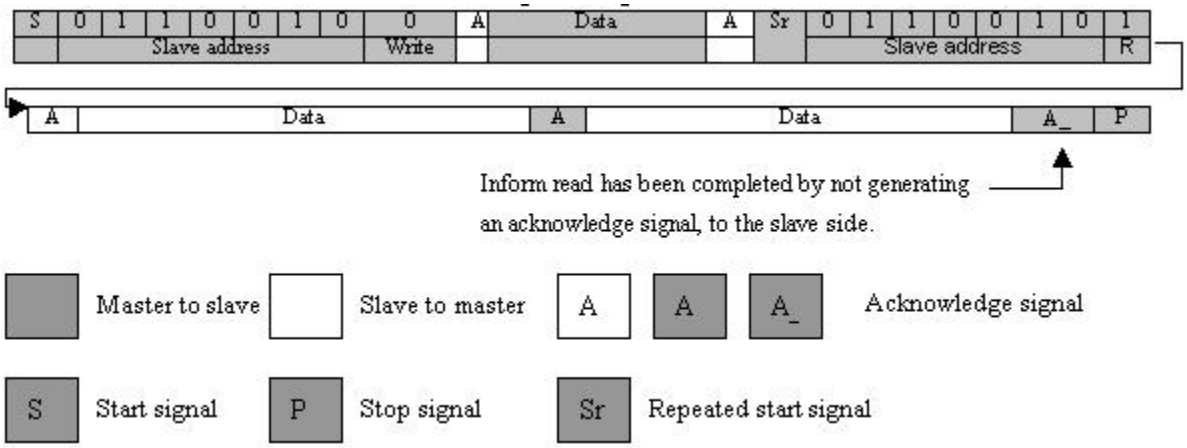
Data is written into the slave from the master

S	0	1	1	0	0	1	0	0	A	Data	A	Data	A	P
	Slave address							Write						

When data is read from the slave immediately after 7bit addressing from the master



When the transmission direction is to be changed during transmission



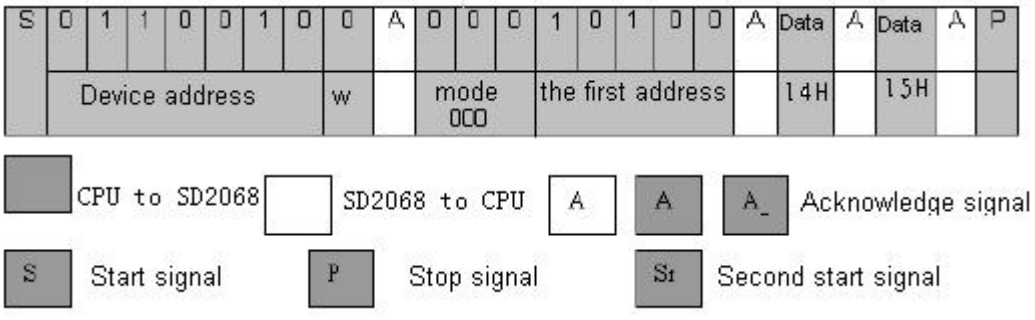
(3)Data Transmission Write Format in the SD2068

1）First send 7 address bit(0110010), the eighth bit is write command “0”. when the ninth bit is ACK signal, SD2068 is under writing condition.

2) In the following byte, the low 5 bits are determined as internal address in SD2068(00H-1FH), the high 3 bits are transmission mode .

3）After writing 1 byte data, there will be 1 bit ACK signal and then writing data in next 1 byte starts. Only when there is a stop signal in the bit after ACK signal, can the writing operation be stopped.

Example of data writing (When writing to internal address 14H to 15H)



(4)Data Transmission Read Format in the SD2068

The SD2068 allows the following two readout methods of data from an internal register.

Ⅰ）The first method to reading data from the named internal address

1) The first two steps are the same as write mode.after one bit ACK signal, a new start signal will be produced to change the direction of data transmission in INTERFACE connection.

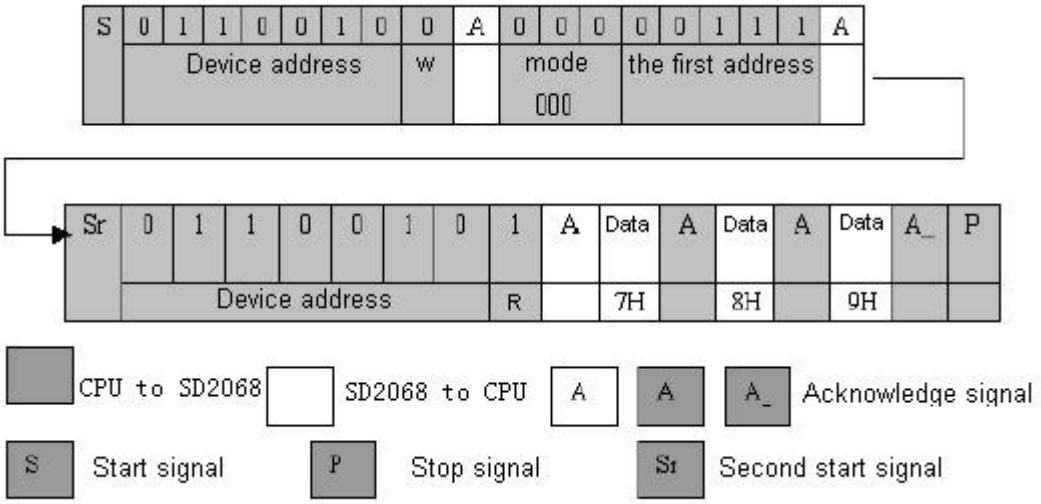
2) Then send 7 address bit(0110010), the eighth bit command is “1”, SD2068 is under

data reading condition.

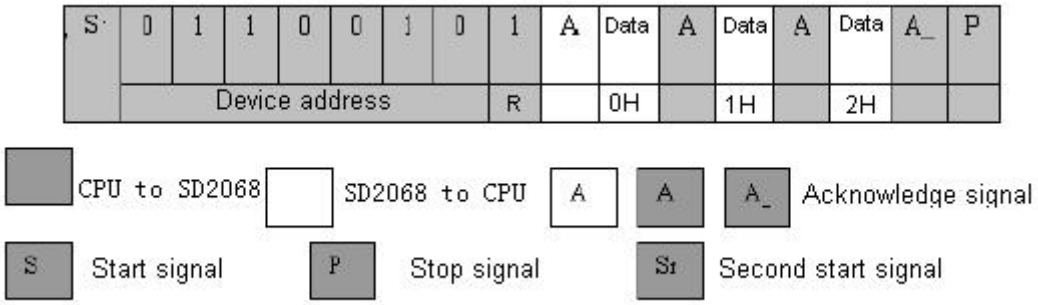
3) After another bit's ACK signal, it starts reading data normally.

4) When a byte data is read and CPU sends 1 bit ACK signal, a next byte data can be read. Only when the 1 bit ACK signal which is sent by CPU is high voltage, can the reading operation be stopped and then CPU sends stop signal.

Example 1 of data read (when data is read from 7H to 9H)



II) The second method to reading data from the internal register is to start reading immediately after writing to the slave address(0110010) and the (R/W) bit. Since the internal address pointer is set to 00h by default, this method is only effective when reading is started from the internal address 00h.



(5)Data Transmission Under Special Condition

The SD2068 hold the clock tentatively for duration from start condition to stop condition to avoid invalid read or write clock on carrying clock. To prevent invalid read or write clock shall be made during one transmission operation. When 0.5 seconds elapses after start condition any access to the SD2068 is automatically released to release tentative hold of the clock and access from the CPU is forced to be terminated (automatic resume function from the interface).

Also a second start condition after the first condition and before the stop condition is

regarded as the “repeated start condition”. Therefore, when 0.5 seconds passed after the first start condition, access to the SD2068 is automatically released.

The user shall always be able to access the real-time clock as long as the following two conditions are met.

1）No stop condition shall be generated until clock read/write is started and completed.

2) One cycle read/write operation shall be completed within 0.5 second.

7. Power Control Operation

The power control circuit accepts a VDD and a VBAT input.

Normal Mode (VDD) to Battery Backup Mode (VBAT)

To transition from the VDD to VBAT mode, the following condition must be met:

$V_{DD} < V_{BAT} – V_{BATHYS}$， where $V_{BATHYS} \approx 100mV$

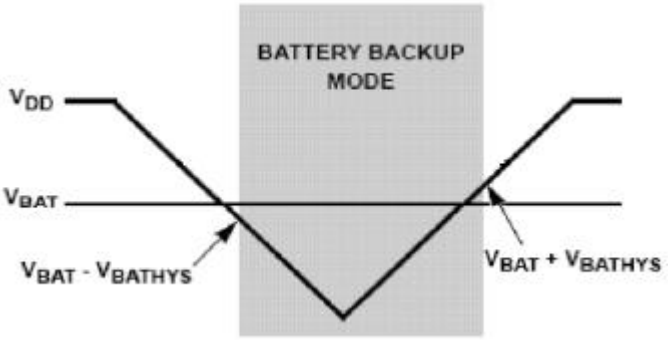
Battery Backup Mode (VBAT) to Normal Mode (VDD)

The SD2068 device will switch from the VBAT to VDD mode when the following condition

occurs:

$V_{DD} > V_{BAT} + V_{BATHYS}$, where $V_{BATHYS} \approx 100mV$

These power control situations are illustrated in the following figure

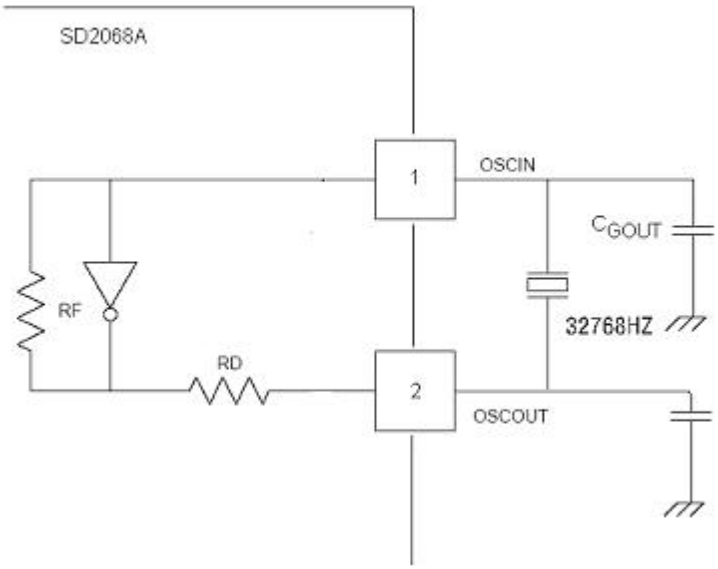


BATTERY SWITCHOVER

In order to reduce the power consumption and impove the reliabilityt,the I2C bus is disable in battery backup mode , but the function of internal counter is normal during battery backup mode. Except the pin SCL and SDA, all the inputs and outputs of the ISD2068 are active during battery backup mode unless disabled via the control register. The User SRAM is operational in battery backup mode down to 1.8V

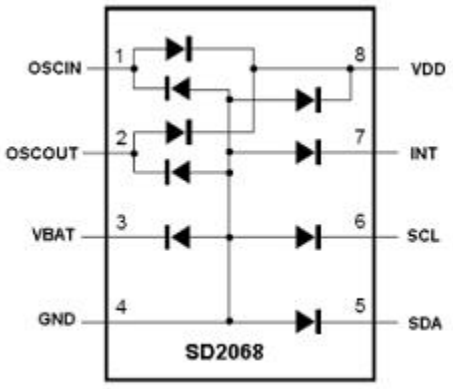
8. Oscillating Circuit

The internal oscillating circuit as following figure:



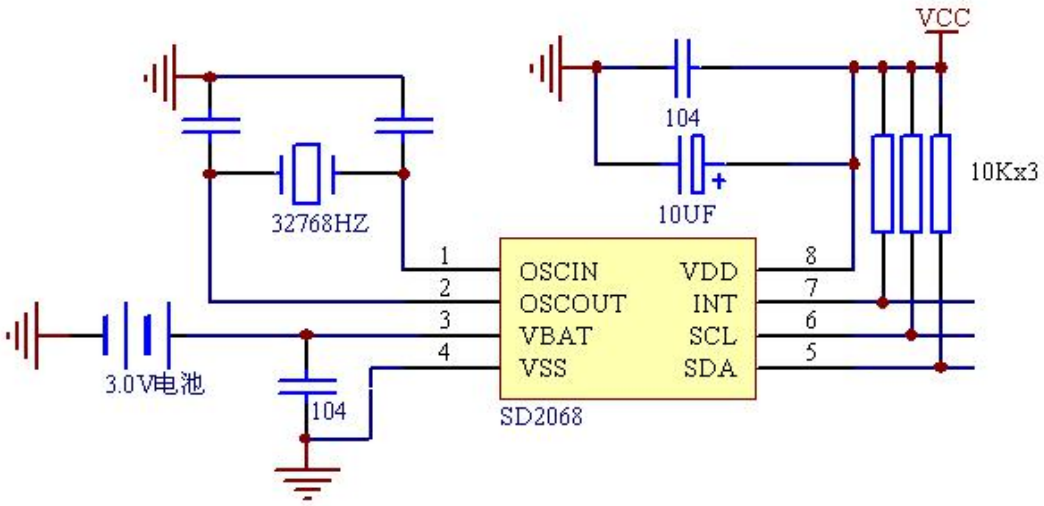
A 32.768Khz crystal can be connected to the SD2068 via pin 1 and 2(OSCIN, OSCOUT),the minimum load capacitance value of the crystal is 6pf.

9.Device diode protection circuit (for reference)

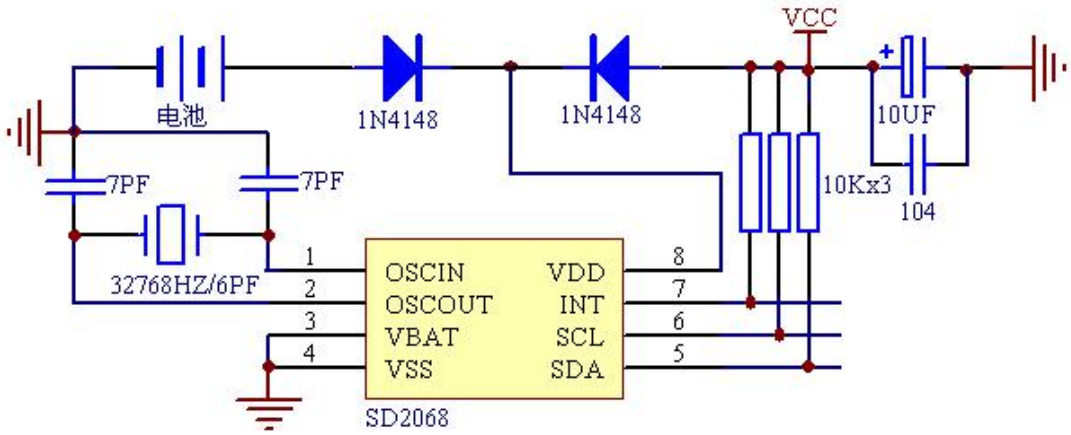


10. Application reference circuit

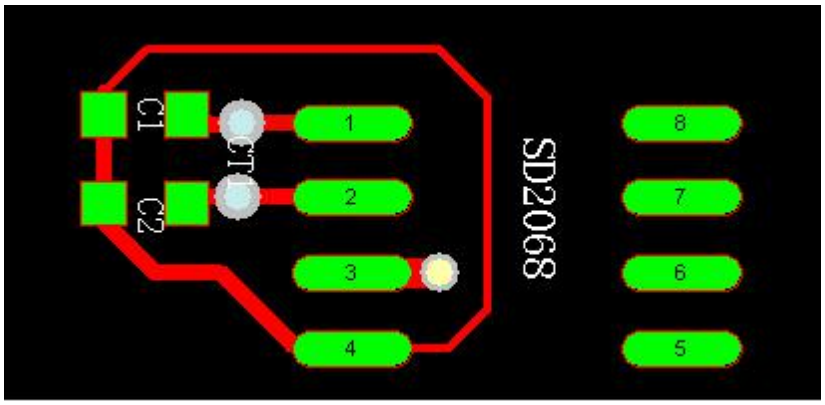
(1) $V_{DD}-V_{Battery}$ > 0.3V:



(2) $V_{DD}-V_{Battery}$ <= 0.3V:



11. PCB layout example



12. Characteristics

Absolute Maximum Ratings

Voltage on VDD,SCL,SDA,and INT pins(Respect to Ground)……...……-0.3V to 6.0V

Storage Temperature……...……－40℃to +85℃

Lead Temperature(Soldering,10s)……...……...……...……260℃/10s

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

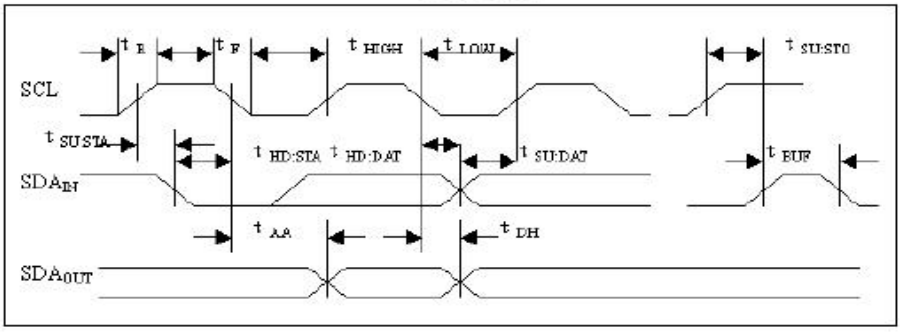
(1)DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Main Power Supply		1.8		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	
I_{DD1}	Supply Current	V_{DD}=5V		1.6	3.0	μA	
		V_{DD}=3V		1.0	1.2	μA	
I_{DD2}	Supply Current win I IC Active	V_{DD}=5V		40	120	μA	
I_{BAT}	Battery Supply Current	V_{BAT}=3V		800		nA	
I_{L1}	Input Leakage Current On SCL			100		nA	
I_{LO}	I/O Leakage Current On SDA			100		nA	
V_{BATHYS}	V_{BAT} Hysteresis		15	50	100	mV	
INT V_{OL}	Output Low Voltage	V_{DD}=5V I_{OL}=3mA			0.4	V	
		V_{DD}=5V I_{OL}=3mA			0.4	V	

(2)AC CHARACTERISTICS

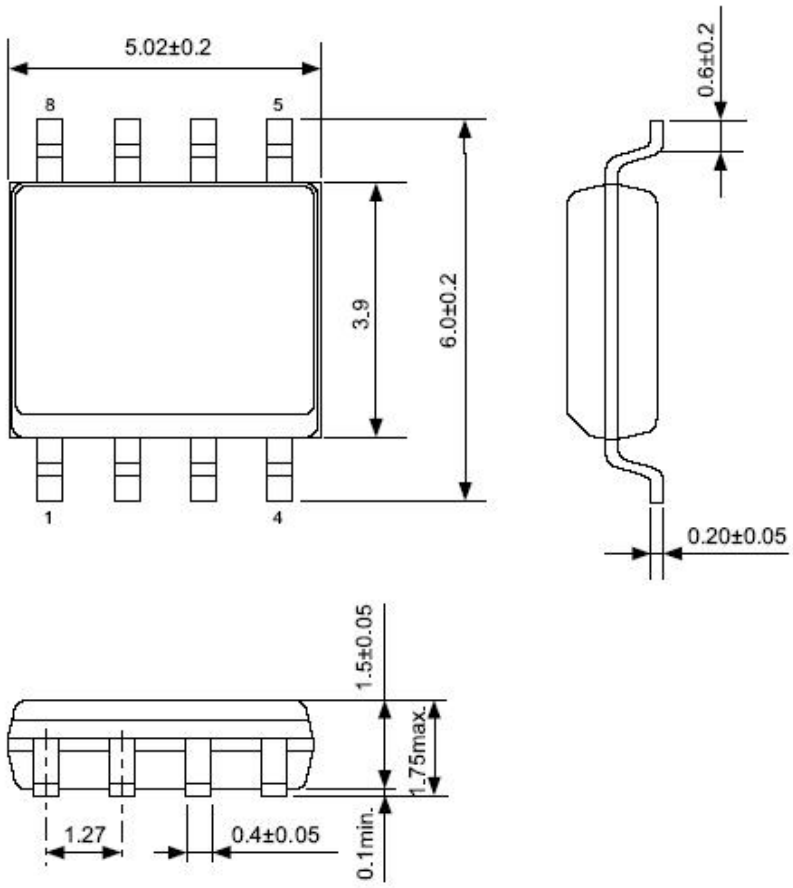
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{IL}	SDA and SCL input buffer LOW voltage		-0.3		0.3×V_{DD}	V	
V_{IH}	SDA and SCL input buffer HIGH voltage		0.7×V_{DD}		V_{DD}+0.3	V	
Hyteresis	SDA and SCL input buffer hysteresis		0.05×V_{DD}			V	
V_{OL}	SDA output buffer LOW voltage sinking 3mA		0		0.4	V	
C_{pin}	SDA and SCL pin capacitance	T_A=25℃ f=1MHZ V_{DD}=5V V_{IN}=0V V_{OUT}=0V			10	pF	
f_{SCL}	SCL frequency				400	kHZ	
t_{IN}	Pulse width suppression time at SDA and SCL inputs				50	ns	
t_{AA}	SCL falling edge to SDA output data valid	SCL falling edge crossing 30%of V_{DD} until SDA exits the 30%to 70%of V_{DD} window			900	ns	
t_{BUF}	Time the bus must be free before the start of a new transmission	SDA crossing 70%of V_{DD} during a STOP condition, to SDA crossing 70%of V_{DD} during the following START condition	1300			ns	
t_{LOW}	Clock LOW time	Measured at the 30% of V_{DD} crossing	1300			ns	
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{DD} crossing	600			ns	
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge Both crossing 70% of V_{DD}	600			ns	
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns	
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{DD} window ,to SCL rising edge crossing 30% of V_{DD}	100			ns	
$t_{HD:DAT}$	Input data hold time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70%of V_{DD} window	0		900	ns	
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{DD} ,to SDA rising edge crossing 30% of V_{DD}	600			ns	
$t_{HD:STO}$	Output condition hold time	From SDA rising edge to SCL falling edge .Both crossing 70% of V_{DD}	600			ns	
t_{DH}	Output data hold time	From SCL falling edge crossing 30% of V_{DD} ,until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL rise time	From 30% to 70% of V_{DD}	20+0.1×Cb		300	ns	
t_F	SDA and SCL fall time	From 70% to 30% of V_{DD}	20+0.1×Cb		300	ns	
Cb	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	PF	
R_{PU}	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F For Cb=400pF,max is about 2~2.5k Ω For Cb=40pF,max is about 15~20k Ω	1			k Ω	

总线时序图



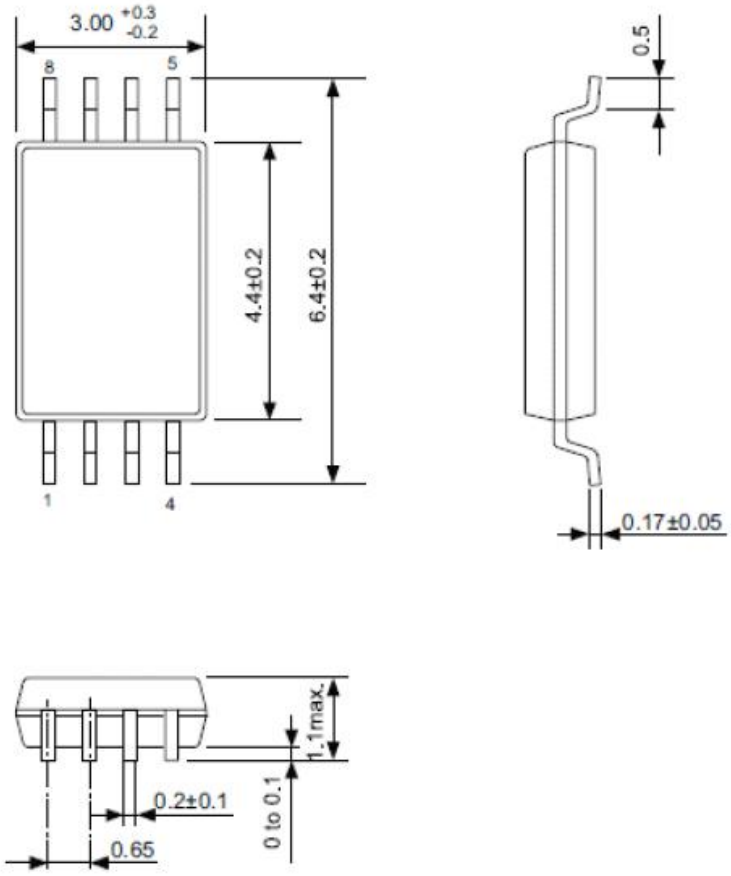
13.Packaging Information(unit:mm)

(1)



SD2068 ,SOP8 Package

(2)



SD2068 ,TSSOP8 Package