Valens
First in HDBaseT™

VS3000 Family
Data Sheet

Version 1.2

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Revision History

Revision	Date	Author	Description
0.1	May 2018	Yaki Sfadya	First Draft
0.2	August 2018	Yaki Sfadya	Second draft. Updated wording for all paragraphs. Updated electrical info: • Table 4: VS3000 Functional Signal Table ; needs further editing • Table 6: Reference Resistor Values • 2.3.4 Ball Diagram • Electrical specification: Absolute Maximum Rating • Table 17: VS3000 Absolute Maximum Rating • Table 19: VS3000 Power Supply • Reference Clock Requirements • Electrical Characteristics (DC Specifications) • Table 25: VS3000 Electrical Specification • Table 27: VS3000 AC Specification • Power on Reset Signal Timing edited note
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0.31	January 2019	Yaki Sfadya	• Corrected mistake in pin out of HDBT swap (N) and (P)
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			• Added description for interrupt signals for matrix design application support – GPIO7, GPIO64, GPIO65
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1.1	January 2022	Yaki Sfadya	• Updated Table 1 – CAT cable and range • Added description to HDMI LED - When partner device is backward, LED indicates DDC transactions on HDCP addresses (0x74/0x75).
1.2	May 2022	Yaki Sfadya	• Added support for 64Mbit Flash • Updated the description of Mem BISR STRAP • Added MSIO compatibility table with VS2000 • Removed STRAP[0]

Glossary

Term	Definition
ARC	Audio Return Channel
AFE	Analog Front End
AV	Audio Video / Audio-Visual
CE	Consumer Electronics
CEC	Consumer Electronic Control
CIR	Consumer Infrared
EVK	Evaluation Kit
CTS	Compliance Test Specification
DDC	Display Data Channel
DVI	Digital Visual Interface
EEPROM	Electronically Erasable Programmable Read-Only Memory
GPIO	General Purpose Input Output
HD	High Definition
HDBT	HDBaseT
HDCD	HDBaseT Configuration Database
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HIF	Host Interface
HLIC	HDBaseT Link Internal Controls
HPD	Hot Plug Detect
I/F	Interface
IC	Integrated Circuit
I^2C	Inter IC
I^2S	Inter IC Sound
KVM	Keyboard / Video / Mouse
LPPF	Low Power Partial Functionality
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MSIO	Multi Serial Input Output
MAC	Media Access Control Layer
MCU	Microcontroller Unit
RoHS	Restriction of Hazardous Substances Directive
SNR	Signal-to-Noise Ratio
MIB	Management Information Base
MSB	Most Significant Bit
OM	Operation Mode

Term	Definition
PHY	Physical Layer
PoE	Power Over Ethernet
PRBS	Pseudo Random Bit Stream
SERDES	SERializer DESerializer
SPDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
STB	Set-Top Box
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

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1 Introduction

This specification provides a detailed description of the Valens VS3000 ProAV IC. The specification provides essential information required for designing a VS3000 embedded application.

1.1 About the VS3000

Valens Semiconductor developed the VS3000 to enable high-quality, wired connectivity of a 5Play feature set over a single CATx cable. The 5Play feature set includes:

- Uncompressed high-definition (HD) video content, including HDMI 2.0 traffic
- High-fidelity digital audio
- 1000BaseTX Ethernet
- Various control/data formats including USB2.0, SPDIF and I^2S audio, I^2C, RS232 and consumer infrared (CIR).
- Up to 100W of power using PoH (Power over HDBaseT)

The VS3000 is based on HDBaseT™ technology – which enables simplified, long-distance wired connectivity of uncompressed HD multimedia content, running at 16 Gbps over a single, standard CATx (CAT5e/6/6a/7) cable.

1.2 Main Benefits

The main benefits of the Valens VS3000 include:

- 16Gbps on main and 2Gbps on return link, support for uncompressed HDMI2.0 4K/60/4:4:4/8bit
- Port Duality: Each VS3000 IC can be configured as an HDBaseT transmitter (TX) or receiver (RX).
- Concurrent, “HDMI in” and “HDMI out” native interfaces
- Backward compatibility with Valens VS1xx and VS2xxx series ICs.
- Support HDCP2.2 termination and conversion capabilities enhance video content security.
- Support USB 2.0 up to 350Mbps data rate
- 1000Mbps/100Mbps Ethernet interface
- Integrated I2S-4: In and Out ports for High-fidelity digital audio
- Audio Extract and Insert on HDMI In, HDMI Out and HDBaseT
- DHDI - Dual High speed digital interface for Multi-Chip interconnection
- Supports multiple ProAV topologies – daisy chain, switch matrix, video wall, and redundant HDBaseT ring.

1.3 Main Applications

The VS3000 is ideal for the following applications:

- HDMI 2.0 extension over CATx cables
- NxK A/V matrixes
- A/V receivers
- HD projectors
- Industrial PCs
- Single wire TVs and two-box TVs
- KVM (Keyboard, Video, Mouse) extension
- Digital signage displays
- Multi-stream video switching / distribution / aggregation, and daisy chaining

1.4 Supported Protocols

The VS3000 uses Valens' T-Adaptor technology to tunnel a wide variety of protocols over an HDBaseT link:

- Video: HDMI 2.0, HDCP 2.x/1.4
- Audio: I^2S-4, SPDIF
- Ethernet: 1000Mbps/100Mbps over SGMII/RMII
- Control: USB, I^2C, UART, CIR
- Multi-chip interconnection: DHDI

1.5 Block Diagram

The figure below is a block diagram illustrating the main functional blocks of the VS3000 IC:

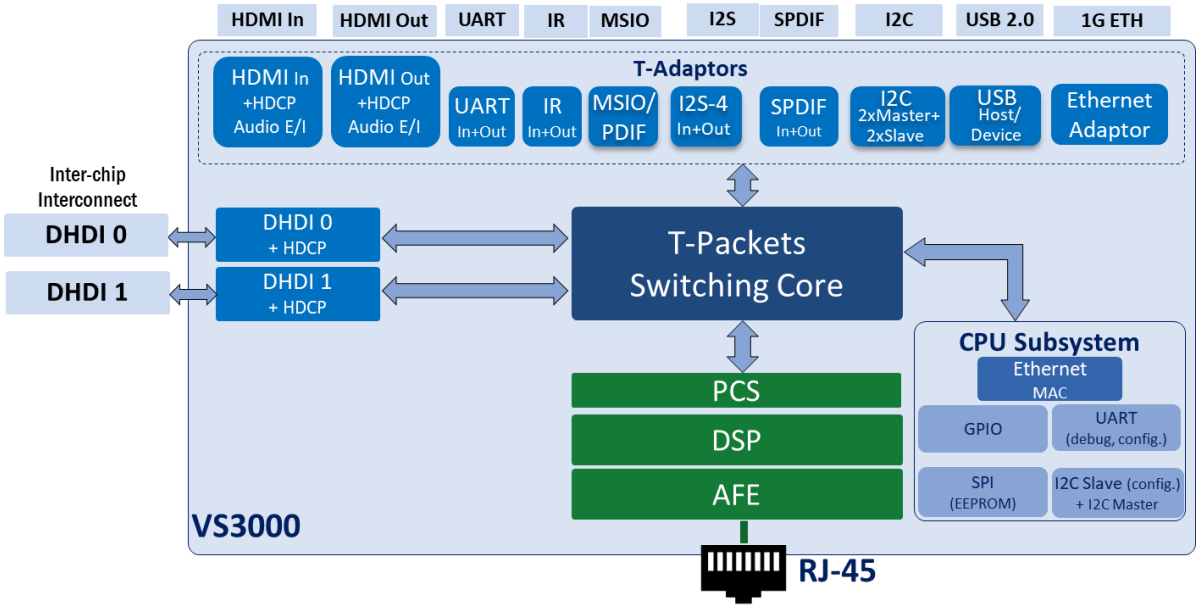


Figure 1: VS3000 Block Diagram

1.6 Features

This section contains an in-depth look at the features of the VS3000.

- Port duality: A single VS3000 IC can be configured to operate as either a TX device on the video source side, or an RX device on the video sink side:
- Compliant with HDBaseT 2.0 Specification supporting 5Play™convergence over a single CATx (CAT5e/6/6a) cable.
    - Audio, Video, Control, 1Gbps Ethernet, USB 2.0 and Power
- Concurrent HDMI In and HDMI Out Native ports with all its components:
    - Fully compliant with HDMI 2.0 (4K 60Hz with 4:4:4 coding) and compatible with HDMI 1.4
    - EDID adjustment mechanism for pixel clock higher than 594 MHz
    - HDCP 2.x/1.4 compliant
    - Audio Extract and Insert function on HDMI ports (future support)
    - Glueless interface: directly connectable to all TMDS, DDC, CEC and HPD HDMI signals (TMDS, DDC, CEC, 5V and HPD)
- Ethernet Interface
    - Delivers 1000BaseTX Ethernet auxiliary channel alongside the HDBaseT channel in both directions (upstream and downstream)

- Support for E-Adaptor SGMII for 1GbE. SGMII and RMII 100MbE for MAC interfaces (connectable to Phy / Switch)

- USB 2.0 interface
  - Configurable either as Host or as a Device USB functionality per HDBaseT standard
- Transfer various control and audio formats over the HDBaseT link including:
  - USB 2.0
  - High quality audio over I2S-4 standard I/F
  - High quality audio over S/PDIF standard I/F
  - RS232 for standard UART control protocol
  - IR – for infra-red control unit
  - I2C – both slave and master interfaces
  - 12 MSIO Pinouts: 6 In and 6 Out – general purpose fast serial channels for delivering any proprietary user format
- Coexistence with IEEE802.3af, IEEE802.3at, IEEE802.3bt and PoH
- Backward compatible to HDBaseT 1.0 Specification and legacy HDBaseT products based on VS2000 and VS100 chip set families
- System Interfaces
  - UART for external debugger
  - I2C slave for External Host interface
  - SPI boot Flash Interface
  - Ethernet 100Mbps MAC
- 2 x DHDI proprietary digital interface for on-board inter-chip connectivity and applications
  - Support for 16Gbps inter-device on-board connectivity
  - HDBaseT Packets over inter-chip interconnection for additional flexibility
- Package Dimensions:
  - VS3000: HSBGA 21 mm x 21 mm, 400-ball grid (20 x 20)
  - Ball pitch 1 mm
- Operational maximum rated junction temperature: minimum 0°C, maximum +125°C
- HDBaseT transmission ranges according to CATx cable type:
  - For max HDMI2.0 resolution recommended cable is: CAT6a U/FTP.
  - The table indicates the total cable length supported (combination of straight cable and with cable patches).
  - Patches used in all cases: 2 X patch cable of 5 meters each. Standard CAT6A, U/FTP, 26AWG.

- For CAT5e/ CAT6 cable a UTP, 24AWG type used
- All cases tested with real traffic– HDMI Video, 1Gbpe and USB2.0.

Table 1: VS3000 CATx Cable Range Specification

Cable Type	Mega-characters per second, per channel (Mcsc)	HDBaseT Link Rate	Max Video resolution	Range - Typical
CAT6a (U/FTP)	450 < Mcsc <= 594	16Gbps	4K/60Hz/4:4:4 video formats	100 meters (straight) 70 meters (with patches)
	<=450	12Gbps	4K/60Hz/4:2:0 HDR 12bit video formats	100 meters (with patches)
CAT5e/CAT6 (UTP)	450 < Mcsc <= 594	16Gbps	4K/60Hz/4:4:4 video formats	40 meters (straight) 30 meters (with patches)
	<=450	12Gbps	4K/60Hz/4:2:0 HDR 12bit video formats	70 meters (with patches)

1.7 Typical Application Examples

1.7.1 HDMI Extender Application

Using the VS3000, HDBaseT links can forward uncompressed HDMI 2.0 traffic at rates of up to 16 Gbps, fully supporting 4K/60fps/4:4:4/8bit video.

In the example in Figure 2 below, an HDBaseT link serves as an HDMI/KVM extender.

On the transmitter/source side, a Full HD or Ultra HD HDMI audiovisual source is connected to the HDMI input interface of the VS3000. An Ethernet device connected via the VS3000's SGMII interface, connects the system to the Ethernet network. The PC, acting as a KVM server, connects to the HDBaseT link as a USB2.0 host.

On the receiver/sink side, a monitor, display, or Ethernet-enabled smart-TV device is connected to the HDMI interface of the VS3000 to receive audiovisual content. The device is connected to the home network via the VS3000's SGMII interface. USB2.0 devices, such as a keyboard and mouse, connect to the USB2.0 host over the HDBaseT link.

Infrared control signals transmitted from the sink side are forwarded over the HDBaseT link and are blasted at the source side by the IR blaster.

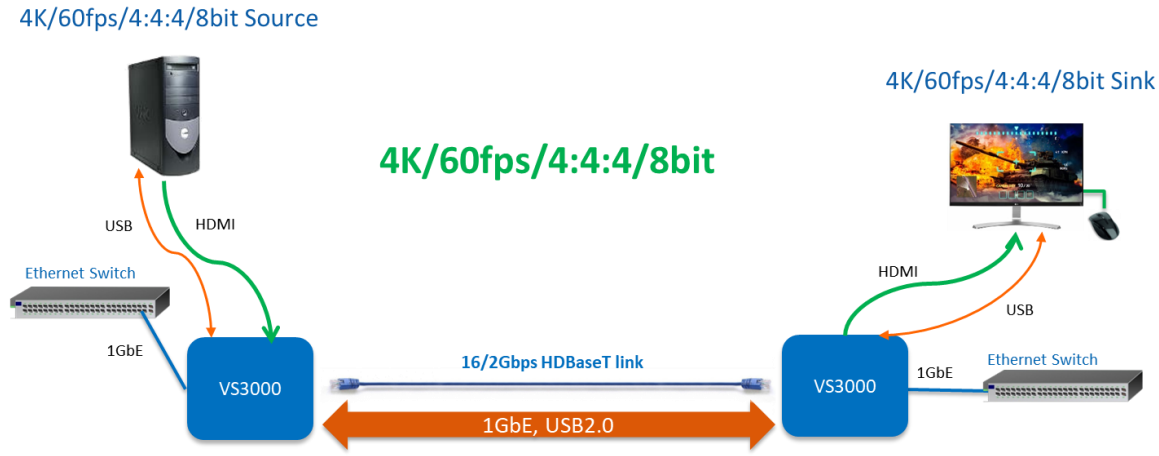


Figure 2: HDMI Extender Application with USB and Ethernet Support

1.7.2 Daisy-Chain Applications (future support)

In a daisy chain application, a video/audio source is introduced at the beginning of the chain to a Valens ProAV device. At every node in the chain, the content is forwarded in a drop-and-continue paradigm:

- **Drop**. The content is restored to its native format by the RX-configured VS3000, and displayed in the sink device
- **Continue**. The content remains in HDBaseT format and is forwarded by the RX-configured VS3000 over the DHDI channel to the TX-configured VS3000, where it is forwarded over the next HDBaseT link in the chain.

Each node in the HDBaseT daisy-chain can be placed at a distance of up to 100 meters from the previous node.

The HDBaseT daisy chain forwards uncompressed 4K/60fps/4:4:4/8bit video and provides full HDCP support.

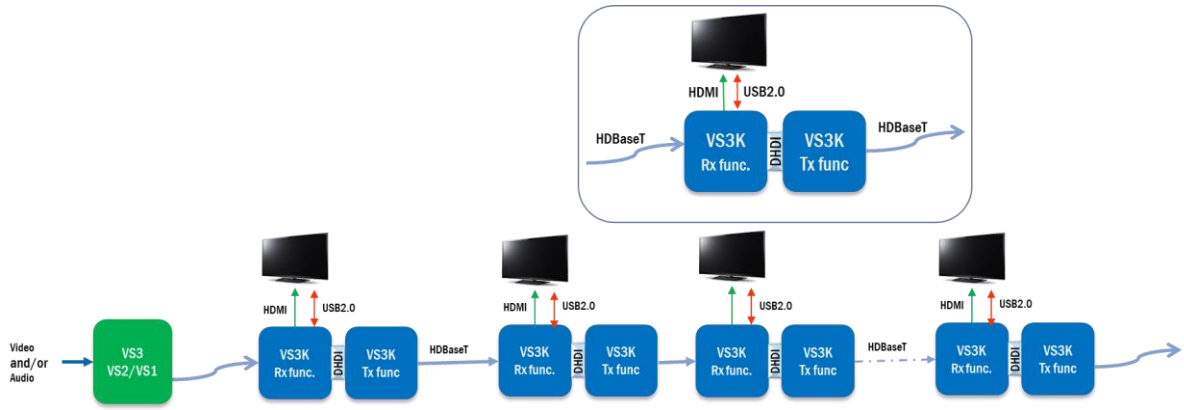


Figure 3: Daisy-Chain Signage Application

1.7.3 Video Wall Multicasting (future support)

In video wall applications, a video source is introduced at the beginning of a daisy chain to a Valens V3000 device that is configured as a TX node. The video source transmits unique content for each display in the video wall.

At every node in the chain, the content intended for that node is restored to its native format by the RX-configured VS3000. The rest of the content is forwarded by the RX-configured VS3000 over the DHDI channel to the TX-configured VS3000, where it is transmitted over the next HDBaseT link in the chain for use in other nodes.

Each HDBaseT link supports 16 Gbps of bandwidth for video wall applications.

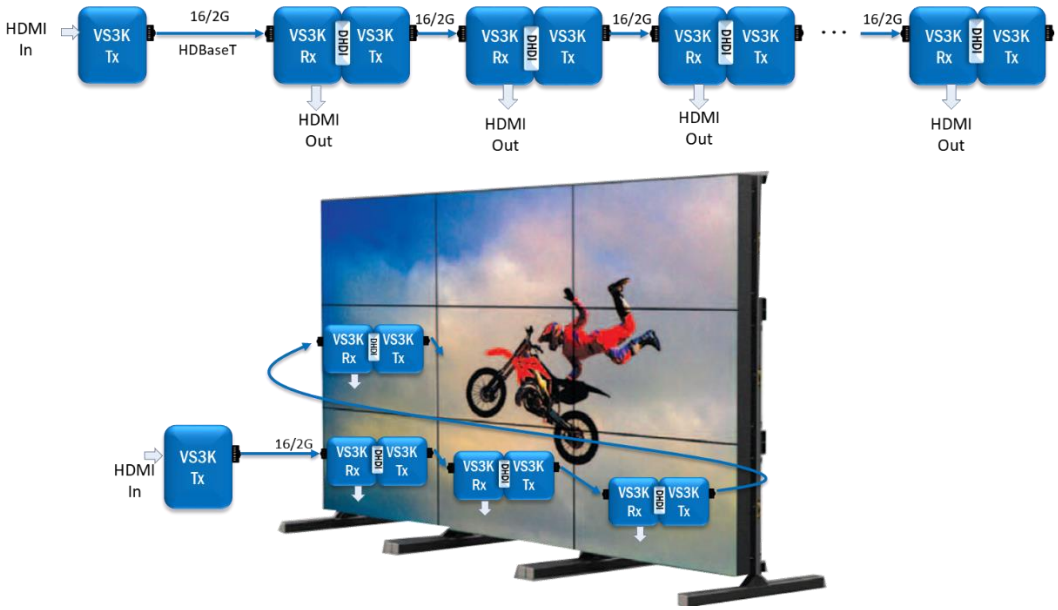


Figure 4: Video Wall Multicasting

1.7.4 KVM Extension/Switching System (future support)

A KVM (keyboard/video/mouse) extension and switching system allows users to access a remotely deployed PC using dedicated peripheral devices installed at a workstation. This setup is excellent for Internet café applications, in which the users have no physical access to computing hardware.

In the example depicted below, three users access remote PC systems over an HDBaseT link supporting asymmetric bandwidth of 16Gbps downstream and 2Gbps upstream.

On the transmitter side, the PCs are connected to a node containing multiple TX-configured VS3000 devices that aggregate traffic using a DHDI link. An Ethernet device is connected via the SGMII interface to connect the system to the Ethernet network.

On the receiver side, a monitor, display, or Ethernet-enabled smart-TV device is connected to the HDMI interface in order to display audiovisual content. The device is connected to the local area network via the SGMII interface. A mouse and keyboard are connected via the USB device interface.

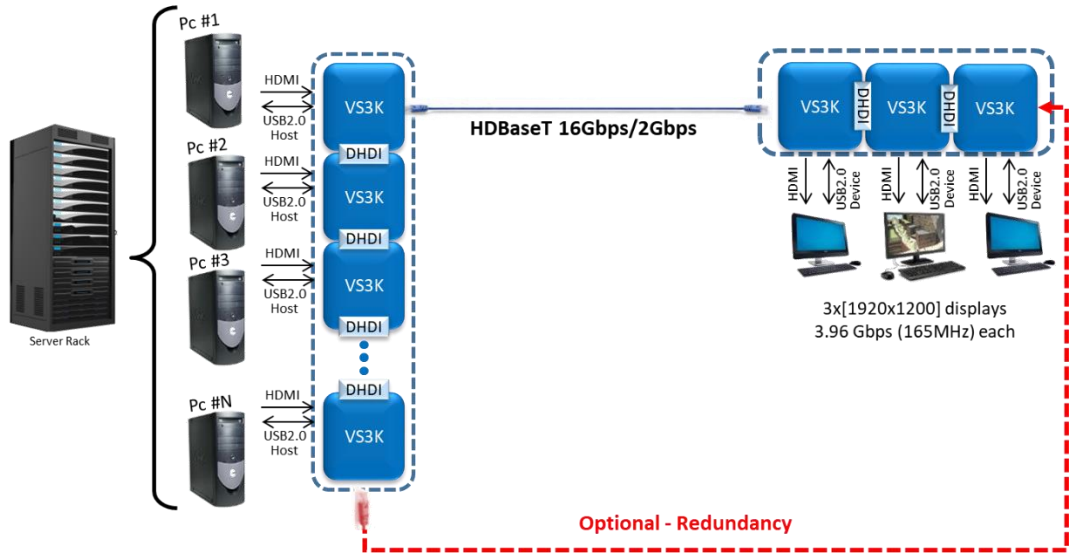


Figure 5: KVM Extender Application with Ethernet Support

1.7.5 Audio Extract and Insert

Audio extraction and insertion functions allow you to extract audio signals in an audiovisual transmission, and insert a replacement signal. These functions are useful when it is necessary to replace an inferior audio signal, or when there is no signal at all.

To implement this feature, a VS3000 IC – either on the source side or the sink side of the HDBaseT link, receives an HDMI source transmission. The extracted audio can be delivered over the VS3000's I^2S OUT T-adaptor to a DSP processor, which replaces the audio content, and returns the alternate content over the I^2S IN T-adaptor to the VS3000, where the signal is reconnected to the HDMI transmission and forwarded to the sink device. The extracted Audio can be transmitted over the HDBaseT link to other devices, instead of I^2S OUT T-adaptor.

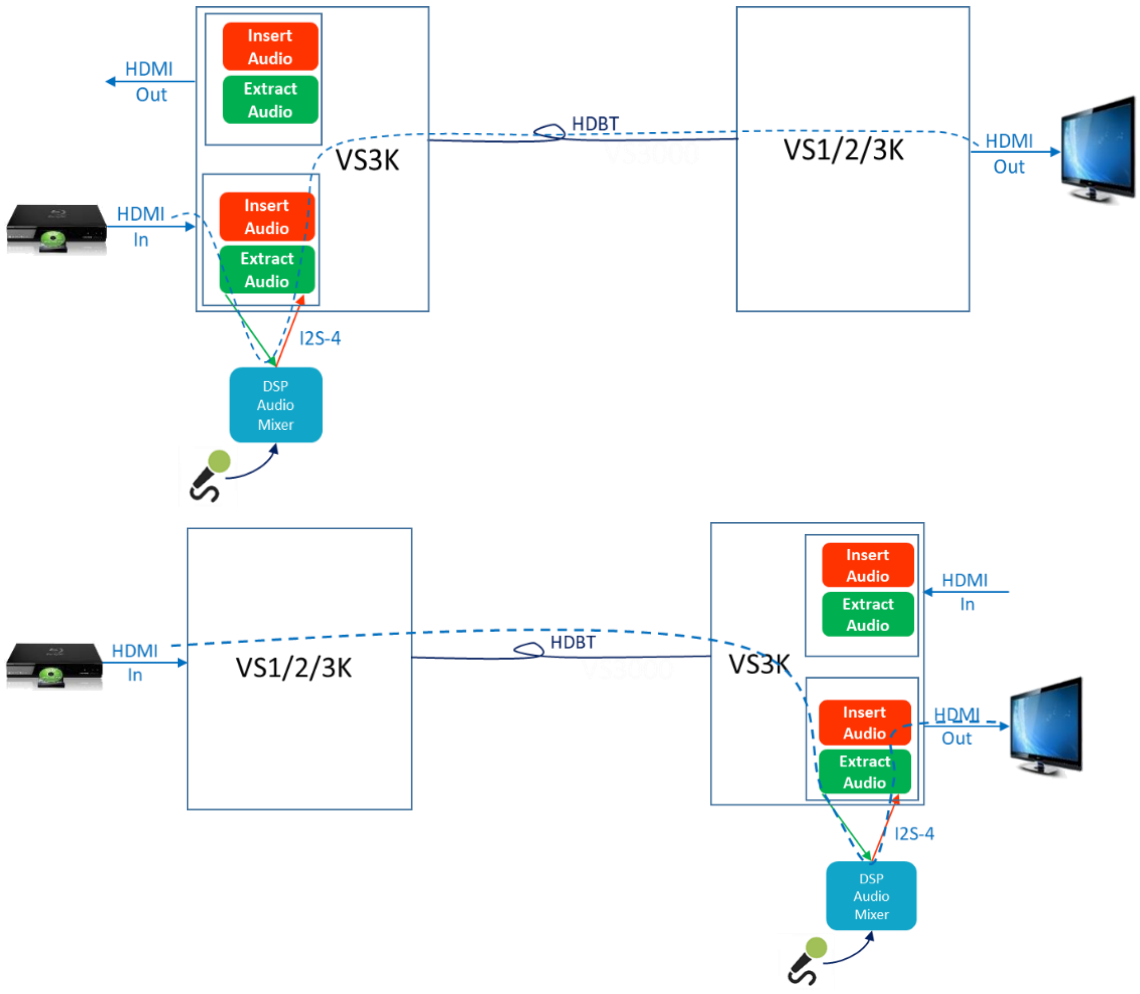


Figure 6: Audio Extract and Insert HDMI In and HDMI Out

1.8 HDBaseT Technology Overview

Valens HDBaseT™ technology empowers **5Play™** digital connectivity between high-definition video sources and remote displays. HDBaseT™ enables plug-and-play delivery of multimedia traffic over a single 100 meter (328 foot) CATx cable:

- Video – Uncompressed high-definition/3D video in up to 4K resolution
- Audio – Any standard digital audio format
- Ethernet – 100BaseTX Ethernet
- Control – Various control signals including USB, CEC, RS-232, and IR
- Power – Up to 100W using Power-over-HDBaseT (PoH) technology

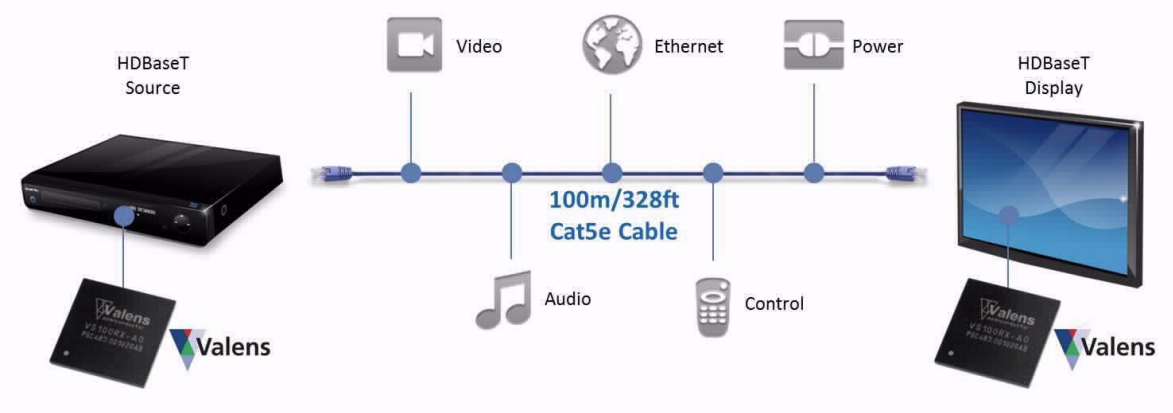


Figure 7: HDBaseT Technology

Video

HDBaseT™ delivers up to 16 Gbps of bandwidth, supporting transmission of uncompressed HDMI2.0 4K/60/444/8bit video – to a network of devices, or over a point-to-point connection. HDBaseT™ provides a transparent transport mechanism for HDMI traffic, thus supporting all key features of HDMI 2.0, including HPD, 5V, CEC, EDID and HDCP. Valens' proprietary video coding scheme ensures the highest video quality with zero latency.

Audio

As with video, HDBaseT™ Audio is transparently transported directly from the HDMI device, thus supporting all standard formats, such as Dolby Digital, DTS, Dolby TrueHD, DTS HD-Master Audio and more.

Ethernet

HDBaseT™ supports 1000Mbps or 100Mbps Ethernet capabilities, enabling televisions, hi-fi equipment, computers, and other consumer electronic devices to communicate with each other and access stored multimedia content, including video streaming, images and music.

Controls

HDBaseT™ delivers a variety of multipurpose control signals, including USB2.0, Consumer Electronic Controls (CEC), RS-232, USB, and infrared. Since HDBaseT™ also supports an Ethernet channel, IP-based control can be employed as well. This opens up endless possibilities for equipment manufacturers, from remote device control to fully managed networks.

The control plane supports additional bandwidth of up to 250 Mbps for applications requiring extra capacity.

Power

As part of its 5Play™ feature-set, HDBaseT™ supports transmission of up to 100W of DC power over the same CATx cable. Now, you can provide power without requiring access to an electric outlet – enhancing device mobility.

1.9 HDBaseT Channel Terminology

The HDBaseT channel consists of two distinct asymmetric unidirectional channels:

- *Main Channel* – Directed downstream from the HDBaseT transmitter to the HDBaseT receiver, carrying uncompressed multimedia content (HDMI, USB, SPDIF, GP MSIO, UART, CIR, I^2S) as well as the transmitter to receiver portion of the Ethernet data content and multimedia controls.
- *Auxiliary Return Channel* – Directed upstream from the HDBaseT receiver to the HDBaseT transmitter, carrying the return channel controls and the receiver to transmitter portion of the data content.

1.10 VS3000 Port duality

The VS3000 IC can be configured (software or hardware) to act as an HDBaseT Transmitter or an HDBaseT Receiver – Port duality. The HDBaseT transmitter connects to the audiovisual source equipment (STBs, Blu-ray / DVD players, etc.) while the HDBaseT receiver connects to the audiovisual sink equipment (monitors, TVs, projectors, etc.). The term ‘gender’ selection (TX or RX) is used in the data sheet document.

2 Pin and Signal Configuration

2.1 VS3000 Interface Diagram

The interface diagram below details various interfaces by signal groups.

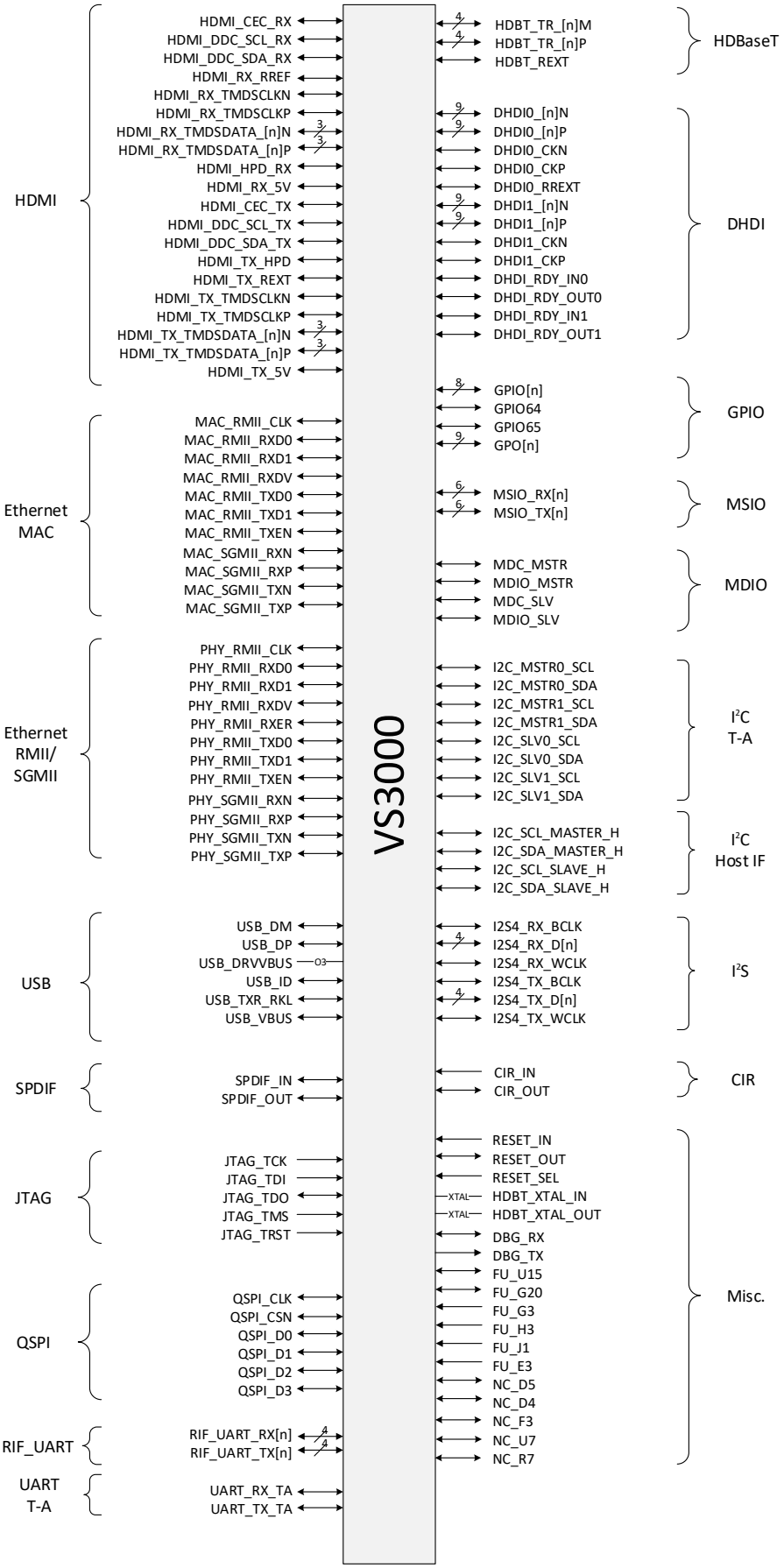


Figure 8: VS3000 I/F Signal Block Diagram

2.2 Pin Type Convention

2.2.1 IO Pad Types

The VS3000 pin types and their descriptions are listed below:

Table 2: VS3000 Pin Types

Pin Type	Description
Input	Digital input pad
Output	Digital output pad
IO	Bidirectional IO digital pad
Input [PU/PD]	Digital input pad [with integrated pull-up/pull-down resistor]
Output [PU/PD]	Digital output pad [with integrated pull-up/pull-down resistor]
IO, PU	Bidirectional IO digital pad with integrated pull-up resistor
IO, PD	Bidirectional IO digital pad with integrated pull-down resistor
AIO	Analog bidirectional pad
AI	Analog input pad
AO	Analog output pad
03State	Digital output pad with tri-state buffer
XTAL	Crystal I/O pad

2.2.2 Unused Pins

If your application does not use one or more interfaces, you should implement the connectivity of the interface's balls according to the *If Not Used* column in Table 4.

The following conventions are used to connect unused pins:

Table 3: VS3000 Unused Pin Types

Category	Connection Requirement
NC	Safe to leave unconnected (floating)
GND	Must be connected to a ground
1KPD	Must be connected to a ground via 1Kohm resistor
1KPU	Must be connected to a 1.8V supply via 1Kohm resistor

2.3 VS3000 Signal Description

Table 4 below provides information on each pin of the VS3000 chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS3000 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 4 that corresponds with the relevant interface category.

2.3.1 Functional Signals

Table 4: VS3000 Functional Signal Table

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
HDMI_CEC_RX	T15	IO	PU, Input	CEC	NC	HDMI RX – CEC
HDMI_CEC_TX	T17	IO	PU, Input	CEC	NC	HDMI TX- CEC
CIR_IN	L3	Input	PD, Input	CIR	4.7KΩ PU to VDDIO_18	Consumer IR, input. Should connect to a 4.7KΩ pull up resistor.
CIR_OUT	L2	IO	PD, Input	CIR	4.7KΩ PU to VDDIO_18	Consumer IR, output. Should connect to a 4.7KΩ pull up resistor.
FU_E3	E3	Input	No pull, Input	Reserved	GND	Must be tied to ground
HDMI_DDC_SCL_RX	U14	IO	PU, Input	DDC I2C	NC	HDMI Rx, display data channel (DDC), clock
HDMI_DDC_SCL_TX	U17	IO	PU, Input	DDC I2C	NC	HDMI Tx, display data channel (DDC), clock
HDMI_DDC_SDA_RX	T14	IO	PU, Input	DDC I2C	NC	HDMI Rx, display data channel (DDC), data
HDMI_DDC_SDA_TX	U16	IO	PU, Input	DDC I2C	NC	HDMI Tx, display data channel (DDC), data
NC_D5	D5	AIO	N/A	Reserved	NC	Reserved
NC_D4	D4	AIO	N/A	Reserved	NC	Reserved
DHDI0_0N	B1	AIO	N/A	DHDI0	NC	DHDI 0, channel 0, (N)
DHDI0_0P	C1	AIO	N/A	DHDI0	NC	DHDI 0, channel 0, (P)
DHDI0_1N	A2	AIO	N/A	DHDI0	NC	DHDI 0, channel 1, (N)
DHDI0_1P	B2	AIO	N/A	DHDI0	NC	DHDI 0, channel 1, (P)
DHDI0_2N	A3	AIO	N/A	DHDI0	NC	DHDI 0, channel 2, (N)
DHDI0_2P	B3	AIO	N/A	DHDI0	NC	DHDI 0, channel 2, (P)
DHDI0_3N	A4	AIO	N/A	DHDI0	NC	DHDI 0, channel 3, (N)
DHDI0_3P	B4	AIO	N/A	DHDI0	NC	DHDI 0, channel 3, (P)
DHDI0_4N	A6	AIO	N/A	DHDI0	NC	DHDI 0, channel 4, (N)
DHDI0_4P	B6	AIO	N/A	DHDI0	NC	DHDI 0, channel 4, (P)
DHDI0_5N	A7	AIO	N/A	DHDI0	NC	DHDI 0, channel 5, (N)
DHDI0_5P	B7	AIO	N/A	DHDI0	NC	DHDI 0, channel 5, (P)
DHDI0_6N	A8	AIO	N/A	DHDI0	NC	DHDI 0, channel 6, (N)
DHDI0_6P	B8	AIO	N/A	DHDI0	NC	DHDI 0, channel 6, (P)
DHDI0_7N	A9	AIO	N/A	DHDI0	NC	DHDI 0, channel 7, (N)
DHDI0_7P	B9	AIO	N/A	DHDI0	NC	DHDI 0, channel 7, (P)
DHDI0_8N	A10	AIO	N/A	DHDI0	NC	DHDI 0, channel 8, (N)
DHDI0_8P	B10	AIO	N/A	DHDI0	NC	DHDI 0, channel 8, (P)
DHDI0_CKN	A5	AIO	N/A	DHDI0	NC	DHDI 0, clock, (N)

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
DHDI0_CKP	B5	AIO	N/A	DHDI0	NC	DHDI 0, clock, (P)
DHDI0_RREXT	E6	AIO	N/A	DHDI0_RREXT	1KΩ PD	DHDI bias external resistor, Should be tied to a 1KΩ (1%) pull down resistor.
DHDI1_0N	B20	AIO	N/A	DHDI1	NC	DHDI 1, channel 0, (N)
DHDI1_0P	C20	AIO	N/A	DHDI1	NC	DHDI 1, channel 0, (P)
DHDI1_1N	A19	AIO	N/A	DHDI1	NC	DHDI 1, channel 1, (N)
DHDI1_1P	B19	AIO	N/A	DHDI1	NC	DHDI 1, channel 1, (P)
DHDI1_2N	A18	AIO	N/A	DHDI1	NC	DHDI 1, channel 2, (N)
DHDI1_2P	B18	AIO	N/A	DHDI1	NC	DHDI 1, channel 2, (P)
DHDI1_3N	A17	AIO	N/A	DHDI1	NC	DHDI 1, channel 3, (N)
DHDI1_3P	B17	AIO	N/A	DHDI1	NC	DHDI 1, channel 3, (P)
DHDI1_4N	A15	AIO	N/A	DHDI1	NC	DHDI 1, channel 4, (N)
DHDI1_4P	B15	AIO	N/A	DHDI1	NC	DHDI 1, channel 4, (P)
DHDI1_5N	A14	AIO	N/A	DHDI1	NC	DHDI 1, channel 5, (N)
DHDI1_5P	B14	AIO	N/A	DHDI1	NC	DHDI 1, channel 5, (P)
DHDI1_6N	A13	AIO	N/A	DHDI1	NC	DHDI 1, channel 6, (N)
DHDI1_6P	B13	AIO	N/A	DHDI1	NC	DHDI 1, channel 6, (P)
DHDI1_7N	A12	AIO	N/A	DHDI1	NC	DHDI 1, channel 7, (N)
DHDI1_7P	B12	AIO	N/A	DHDI1	NC	DHDI 1, channel 7, (P)
DHDI1_8N	A11	AIO	N/A	DHDI1	NC	DHDI 1, channel 8, (N)
DHDI1_8P	B11	AIO	N/A	DHDI1	NC	DHDI 1, channel 8, (P)
DHDI1_CKN	A16	AIO	N/A	DHDI1	NC	DHDI 1, clock, (N)
DHDI1_CKP	B16	AIO	N/A	DHDI1	NC	DHDI 1, clock, (P)
GPIO0	G4	IO	PU, Input	GPIO	NC	General purpose IO - bit 0
GPIO1	G5	IO	PU, Input	GPIO	NC	General purpose IO - bit 1
GPIO2	H4	IO	PU, Input	GPIO	NC	Interrupt to Host interface CPU reduced I2C stretching ST: General purpose IO - bit 2
GPIO3	H5	IO	PU, Input	GPIO	NC	General purpose IO - bit 3
GPIO4	P1	IO	PU, Input	GPIO	NC	General purpose IO - bit 4
GPIO5	R1	IO	PU, Input	GPIO	NC	General purpose IO - bit 5
GPO9/SW_STRAP[15]	T1	IO	PU, Input	GPIO	Must use	General purpose Output - bit 9 ST: MAC SGMII AC/ DC coupling
GPIO64	F5	IO	PD, Input	GPIO	NC	Interrupt to Host interface CPU matrix support ST: General purpose IO - bit 64
GPIO65	J3	IO	PU, Input	GPIO	NC	Interrupt to Host interface CPU matrix support ST: General purpose IO - bit 65

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
GPIO7	T2	IO	PU, Input	GPIO	NC	Interrupt to Host interface CPU matrix support ST: General purpose IO - bit 7
GPO0/STRAP[2]	M5	IO	PD, Input	GPIO	Must use	Firmware LED ST: I2C address - bit 0
GPO1/STRAP[3]	M4	IO	PD, Input	GPIO	Must use	HDBT link LED ST: I2C address - bit 1
GPO2/STRAP[4]	M3	IO	PD, Input	GPIO	Must use	Interrupt to Host interface CPU ST: I2C address - bit 2
GPO3/SW_STRAP[7]	M2	IO	PD, Input	GPIO	Must use	HDMI out status LED ST: MAC SGMII/RMII selection
GPO4/STRAP[1]	M1	IO	PD, Input	GPIO	Must use	HDMI in status LED ST: Flash SPI 4/3 byte
GPO5	L1	IO	PD, Input	GPIO	1-2KΩ PD	HDBaseT Gender LED
GPO6/STRAP[11]	K1	IO	PD, Input	GPIO	Must use	General purpose output - bit 6 ST: Memory BISR enable
GPO7/MCLK2/SW_STRAP[5]	N19	IO	PU, Input	GPIO /I2S	Must use	I2S Tx MCLK ST: HDBaseT Gender definition - bit 0
GPO8/MCLK1/SW_STRAP[9]	M20	IO	PU, Input	GPIO /I2S	Must use	I2S Rx MCLK ST: External Flash not Present
HDBT_TR_0M	Y3	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 0, (N)
HDBT_TR_0P	W3	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 0, (P)
HDBT_TR_1M	Y5	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 1, (N)
HDBT_TR_1P	W5	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 1, (P)
HDBT_TR_2M	Y7	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 2, (N)
HDBT_TR_2P	W7	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 2, (P)
HDBT_TR_3M	Y9	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 3, (N)
HDBT_TR_3P	W9	AIO	N/A	HDBT	NC	HDBaseT Transceiver Channel 3, (P)
NC_U7	U7	AIO	N/A	Reserved	NC	Reserved
NC_R7	R7	AIO	N/A	Reserved	NC	Reserved
HDBT_REXT	T8	AIO	N/A	HDBT	4.12KΩ PD	HDBT current Source Resistor, Should be tied to a 4.12KΩ (1%) PD.
HDBT_XTAL_IN	W1	XTAL	N/A	XTAL	Must use	25MHz oscillator or crystal input
HDBT_XTAL_OUT	V1	XTAL	N/A	XTAL	NC	25MHz crystal output
HDMI_RX_RREF	R11	AIO	N/A	HDMI_RX	1.62KΩ PD	HDMI Rx external reference resistor, Should be tied to a 1.62KΩ (1%) PD.
HDMI_RX_TMDSCLKN	Y11	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line clock, Receive, (N)
HDMI_RX_TMDSCLKP	W11	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line clock, Receive, (P)

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
HDMI_RX_TMDSDATA_0N	Y12	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 0, (N)
HDMI_RX_TMDSDATA_1N	Y14	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 1, (N)
HDMI_RX_TMDSDATA_2N	Y15	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 2, (N)
HDMI_RX_TMDSDATA_0P	W12	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 0, (P)
HDMI_RX_TMDSDATA_1P	W14	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 1, (P)
HDMI_RX_TMDSDATA_2P	W15	AIO	N/A	HDMI_RX	NC	HDMI Rx, TMDS differential line data, Receive, channel 2, (P)
HDMI_TX_HPD*	R15	AIO	N/A	HDMI_TX	NC	HDMI Tx, hot plug detect, 5V signal
HDMI_TX_REXT	R13	AIO	N/A	TX_REXT	1.62KΩ PD	HDMI Tx external reference resistor, Should be tied to a 1.62KΩ (1%) PD.
HDMI_TX_TMDSCLKN	Y17	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line clock, Transmit, (N)
HDMI_TX_TMDSCLKP	W17	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line clock, Transmit, (P)
HDMI_TX_TMDSDATA_0N	Y18	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 0, (N)
HDMI_TX_TMDSDATA_1N	V20	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 1, (N)
HDMI_TX_TMDSDATA_2N	U20	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 2, (N)
HDMI_TX_TMDSDATA_0P	W18	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 0, (P)
HDMI_TX_TMDSDATA_1P	V19	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 1, (P)
HDMI_TX_TMDSDATA_2P	U19	AIO	N/A	HDMI_TX	NC	HDMI Tx, TMDS differential line data, Transmit, channel 2, (P)
HDMI_HPD_RX	U12	IO	PD, Input	HDMI_RX	NC	HDMI Rx, hot plug detect
FU_U15	U15	IO	PD, Input	Reserved	GND	Reserved
I2C_SCL_MSTR0_TA	R4	IO	PU, Input	I2CM T-A	NC	I2C T-A, Master 0, clock
I2C_SDA_MSTR0_TA	R5	IO	PU, Input	I2CM T-A	NC	I2C T-A, Master 0, data
I2C_SCL_MSTR1_TA	K4	IO	PU, Input	I2CM T-A	NC	I2C T-A, Master 1, clock
I2C_SDA_MSTR1_TA	K5	IO	PU, Input	I2CM T-A	NC	I2C T-A, Master 1, data
I2C_SCL_MSTR_H	T3	IO	PU, Input	I2C MSR HOST	NC	I2C host interface, Master, clock
I2C_SCL_SLV_H	P4	IO	PU, Input	I2C SLV HOST	NC	I2C host interface, Slave, clock
I2C_SDA_MSTR_H	U3	IO	PU, Input	I2C MSR HOST	NC	I2C host interface, Master, data

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
I2C_SDA_SLV_H	P5	IO	PU, Input	I2C SLV HOST	NC	I2C host interface, Slave, data
I2C_SCL_SLV0_TA	J4	IO	PU, Input	I2CS T-A	NC	I2C T-A, Slave #0, clock
I2C_SDA_SLV0_TA	J5	IO	PU, Input	I2CS T-A	NC	I2C T-A, Slave #0, data
I2C_SCL_SLV1_TA	L4	IO	PU, Input	I2CS T-A	NC	I2C T-A, Slave #1, clock
I2C_SDA_SLV1_TA	L5	IO	PU, Input	I2CS T-A	NC	I2C T-A, Slave #1, data
I2S4_RX_BCLK/GPIO24	L20	IO	PD, Input	I2S IN	NC	F1: I2S receive bit clock F2: General purpose IO - bit 24
I2S4_RX_D0/GPIO29	K18	IO	PD, Input	I2S IN	NC	F1: I2S receive data - bit 0 F2: General purpose IO - bit 29
I2S4_RX_D1/GPIO28	K17	IO	PD, Input	I2S IN	NC	F1: I2S receive data - bit 1 F2: General purpose IO - bit 28
I2S4_RX_D2/GPIO27	J18	IO	PD, Input	I2S IN	NC	F1: I2S receive data - bit 2 F2: General purpose IO - bit 27
I2S4_RX_D3/GPIO26	J17	IO	PD, Input	I2S IN	NC	F1: I2S receive data - bit 3 F2: General purpose IO - bit 26
I2S4_RX_WCLK/GPIO25	L19	IO	PD, Input	I2S IN	NC	F1: I2S receive word clock F2: General purpose IO - bit 25
I2S4_TX_BCLK/GPIO18	N20	IO	PD, Input	I2S OUT	NC	F1: I2S transmit bit clock F2: General purpose IO - bit 18
I2S4_TX_D0/GPO23/ SW_STRAP[12]	M18	IO	PD, Input	I2S OUT	Must use	F1: I2S transmit data - bit 0 F2: General purpose output - bit 23 ST: Long Reach Mode - bit 0
I2S4_TX_D1/GPO22/ SW_STRAP[13]	M17	IO	PD, Input	I2S OUT	Must use	F1: I2S transmit data - bit 1 F2: General purpose output - bit 22 ST: Long Reach Mode - bit 1
I2S4_TX_D2/GPO21/ SW_STRAP[6]	L18	IO	PD, Input	I2S OUT	Must use	F1: I2S transmit data - bit 2 F2: General purpose output - bit 21 ST: HDBaseT Gender definition - bit 1
I2S4_TX_D3/GPO20/ SW_STRAP[10]	L17	IO	PD, Input	I2S OUT	Must use	F1: I2S transmit data - bit 3 F2: General purpose output - bit 20 ST: Wait for HostIF
I2S4_TX_WCLK/GPIO19	M19	IO	PD, Input	I2S OUT	NC	F1: I2S transmit word clock F2: General purpose IO - bit 19
JTAG_TCK	D7	Input	PU, Input	JTAG	NC	JTAG test clock
JTAG_TDI	E9	Input	PU, Input	JTAG	NC	JTAG test data in
JTAG_TDO	D9	IO	No pull, Input	JTAG	NC	JTAG test data out
JTAG_TMS	D8	Input	PU, Input	JTAG	NC	JTAG test mode select
JTAG_TRST	E8	Input	PD, Input	JTAG	1KΩ PD	JTAG test reset
MAC_RMII_CLK/GPIO33	G19	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC clock F2: General purpose IO - bit 33

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
MAC_RMII_RXD0/GPIO36	G17	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC receive data -bit 0 F2: General purpose IO - bit 36
MAC_RMII_RXD1/GPIO35	H17	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC receive data -bit 1 F2: General purpose IO - bit 35
MAC_RMII_RXDV/GPIO34	H18	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC receive data valid F2: General purpose IO - bit 34
MAC_RMII_TXD0/GPIO32	G16	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC transmit data -bit 0 F2: General purpose IO - bit 32
MAC_RMII_TXD1/GPIO31	G18	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC transmit data -bit 1 F2: General purpose IO - bit 31
MAC_RMII_TXEN/GPIO30	H16	IO	PD, Input	MAC	NC	F1: Host interface RMII MAC transmit enable F2: General purpose IO - bit 30
DHDI_RDY_IN0	D11	IO	PU, Input	DHDI	NC	DHDI 0, channel ready input
DHDI_RDY_IN1	D12	IO	PU, Input	DHDI	NC	DHDI 1, channel ready input
DHDI_RDY_OUT0	E11	IO	PU, Input	DHDI	NC	DHDI 0, channel ready output
DHDI_RDY_OUT1	E12	IO	PU, Input	DHDI	NC	DHDI 1, channel ready output
MDC_MSTR	D13	IO	PD, Input	Ethernet MAC	NC	Ethernet host interface registers management clock, master
MDC_SLV/GPIO9	R18	IO	PU, Input	Ethernet T-A	NC	F1: Ethernet T-A registers management clock, slave F2: General purpose IO - bit 9
MDIO_MSTR	E13	IO	PU, Input	Ethernet MAC	NC	Ethernet host interface registers management data input output, master
MDIO_SLV/GPIO8	R17	IO	PU, Input	Ethernet T-A	NC	F1: Ethernet T-A registers management data input output, slave F2: General purpose IO - bit 8
MSIO_RX0/GPIO43	D14	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 0 F2: General purpose IO - bit 43
MSIO_RX1/GPIO44	E14	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 1 F2: General purpose IO - bit 44
MSIO_RX2/GPIO45	F14	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 2 F2: General purpose IO - bit 45
MSIO_RX3/GPIO46	D15	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 3 F2: General purpose IO - bit 46

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
MSIO_RX4/GPIO47	E15	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 4 F2: General purpose IO - bit 47
MSIO_RX5/GPIO48	F15	IO	PD, Input	MSIO_RX	NC	F1: Multi Serial Input - bit 5 F2: General purpose IO - bit 48
MSIO_TX0/GPIO37	D17	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 0 F2: General purpose IO - bit 37
MSIO_TX1/GPIO38	E17	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 1 F2: General purpose IO - bit 38
MSIO_TX2/GPIO39	F17	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 2 F2: General purpose IO - bit 39
MSIO_TX3/GPIO40	D16	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 3 F2: General purpose IO - bit 40
MSIO_TX4/GPIO41	E16	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 4 F2: General purpose IO - bit 41
MSIO_TX5/GPIO42	F16	IO	PD, Input	MSIO_TX	NC	F1: Multi Serial Output - bit 5 F2: General purpose IO - bit 42
DBG_RX	T5	Input	PU, Input	UART PMS	4.7KΩ PU	Tied to a 4.7KΩ pull up resistor to VDDIO_18. Test point for debug purposes
DBG_TX	U5	Output	Output	UART PMS	NC	Test point for debug purposes
QSPI_CLK	K20	IO	PU, Input	QSPI	NC	QSPI clock for external flash
QSPI_CSN	K19	IO	PU, Input	QSPI	NC	QSPI chip select for external flash
QSPI_D0	J20	IO	PU, Input	QSPI	NC	QSPI Data 0 for external FLASH
QSPI_D1	H20	IO	PU, Input	QSPI	NC	QSPI Data 1 for external FLASH
QSPI_D2	J19	IO	PU, Input	QSPI	NC	QSPI Data 2 for external FLASH
QSPI_D3	H19	IO	PU, Input	QSPI	NC	QSPI Data 3 for external FLASH
RESET_IN	D10	Input	No pull, Input	Reset	4.7KΩ PU	Reset In (Active only when RESET_SEL=1)
RESET_OUT	F13	AIO	N/A	RESET	4.7KΩ PU	Power on reset bi-directional pin (open drain). 4.7KΩ PU resistor to 1.8V Analog and 1nF capacitor to GND close to the pin are needed when active (RESET_SEL=0)
RESET_SEL	E10	Input	No pull, Input	RESET	Must use	Power on reset bypass. RESET_SEL=0: RESET_OUT (POR enabled). RESET_SEL=1:RESET_IN (POR bypass)
RIF_UART_RX0	T4	IO	PU, Input	UART Logger	NC	Logger interface UART port 0, Receive
RIF_UART_RX1	R3	IO	PU, Input	Host IF UART	NC	Host IF UART port 1, Receive
RIF_UART_RX2	P3	IO	PU, Input	UART	NC	Interface UART 2, Receive
RIF_UART_RX3	N5	IO	PU, Input	UART	NC	Interface UART 3, Receive

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
RIF_UART_TX0	U4	IO	PU, Input	UART Logger	NC	Logger interface UART 0, Transmit
RIF_UART_TX1	R2	IO	PU, Input	Host RIF UART	NC	Host IF UART 1, Transmit
RIF_UART_TX2	P2	IO	PU, Input	UART	NC	Interface UART 2, Transmit
RIF_UART_TX3	N4	IO	PU, Input	UART	NC	Interface UART 3, Transmit
PHY_RMII_CLK/GPIO 13	R20	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII clock F2: General purpose IO - bit 13
PHY_RMII_RXD0/GPIO17	P20	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII receive data - bit 0 F2: General purpose IO - bit 17
PHY_RMII_RXD1/GPIO16	R19	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII receive data - bit 1 F2: General purpose IO - bit 16
PHY_RMII_RXDV/GPIO14	P19	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII receive data valid F2: General purpose IO - bit 14
PHY_RMII_RXER/GPIO15	P18	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII receive error F2: General purpose IO - bit 15
PHY_RMII_TXD0/GPIO12	N18	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII transmit data - bit 0 F2: General purpose IO - bit 12
PHY_RMII_TXD1/GPIO11	N17	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII transmit data - bit 1 F2: General purpose IO - bit 11
PHY_RMII_TXEN/GPIO10	P17	IO	PD, Input	Ethernet T-A	NC	F1: Ethernet T-A RMII transmit enable F2: General purpose IO - bit 10
MAC_SGMII_RXN	F2	AIO	N/A	Ethernet MAC	NC	Host interface SGMII MAC receive data (N)
MAC_SGMII_RXP	F1	AIO	N/A	Ethernet MAC	NC	Host interface SGMII MAC receive data (P)
MAC_SGMII_TXN	E2	AIO	N/A	Ethernet MAC	NC	Host interface SGMII MAC transmit data (N)
MAC_SGMII_TXP	E1	AIO	N/A	Ethernet MAC	NC	Host interface SGMII MAC transmit data (P)
NC_F3	F3	AIO	N/A	Reserved	NC	Reserved
PHY_SGMII_RXN	H2	AIO	N/A	Ethernet T-A	NC	Ethernet T-A SGMII PHY receive data (N)
PHY_SGMII_RXP	H1	AIO	N/A	Ethernet T-A	NC	Ethernet T-A SGMII PHY receive data (P)
PHY_SGMII_TXN	G2	AIO	N/A	Ethernet T-A	NC	Ethernet T-A SGMII PHY transmit data (N)

Signal Name	Ball#	Pad Type	Reset State	I/F category	If Not Used	Functional Description
PHY_SGMII_TXP	G1	AIO	N/A	Ethernet T-A	NC	Ethernet T-A SGMII PHY transmit data (P)
SPDIF_IN	K3	IO	PD, Input	SPDIF	NC	SPDIF input
SPDIF_OUT	K2	IO	PD, Input	SPDIF	NC	SPDIF output
FU_G20	G20	IO	PU, Input	Reserved	GND	Reserved. Must be tied to ground
FU_G3	G3	Input	No pull, Input	Reserved	GND	Reserved. Must be tied to ground
FU_H3	H3	Input	No pull, Input	Reserved	GND	Reserved. Must be tied to ground
FU_J1	J1	Input	No pull, Input	Reserved	GND	Reserved. Must be tied to ground
UART_RX_TA/GPIO53	N2	IO	PU, Input	UART T-A	NC	F1: UART T-A, Receive F2: General purpose IO - bit 53
UART_TX_TA/GPO54/SW_STRAP[8]	N1	IO	PU, Input	UART T-A	Must use	F1: UART T-A, Transmit F2: General purpose output - bit 54 ST: Ethernet T-A SGMII/RMII selection
USB_DM	E20	AIO	N/A	USB 2.0	NC	USB DM signal
USB_DP	E19	AIO	N/A	USB 2.0	NC	USB DP signal
USB_DRVVBUS	F18	O3State	PD, Input	USB 2.0	NC	VBUS charge pump control, active high.
USB_ID/SW_STRAP[14]	D19	AIO	PU, Input	USB 2.0	Must use	ST: USB device/host selection
USB_TXR_RKL	G12	AIO	N/A	USB 2.0	200Ω PD	USB external reference resistor, Should be tied to a 200Ω pull down (1% tolerance) resistor.
USB_VBUS*	D18	AIO	N/A	USB 2.0	NC	USB 5V signal
HDMI_RX_5V	U13	IO	PD, Input	HDMI	NC	HDMI Rx, 5V indication
HDMI_TX_5V	T16	IO	PD, Input	HDMI	NC	HDMI Tx, 5V indication

* 5V signals

2.3.2 Non-Functional Signals

Table 5: VS3000 Non-Functional Signal Table

Symbol	Description	Ball Numbers
HDBT_VDDA	0.98 V Analog supply	M8, M10, N8, N10
VDDA_33	3.3V analog supply	P9, P13,H12
VDD	0.95 V digital supply	H8, H10, H14, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M12, M14
VDDA	0.95 V analog supply	N12, N14, G7, G9, G11, K6
VDDA_18	1.8 V analog supply	G6, G8, G10, N7, N9, N11, N13
VDDIO_18	1.8 V digital supply	H6, M6, G14, J15, L15
VSS	Ground	A1, A20, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, D1, D2, D3, D6, D20, E4, E5, E7, E18, F4, F6, F7, F8, F9, F10, F11, F12, F19, F20, G13, G15, H7, H9, H11, H13, H15, J2, J6, J8, J10, J12, J14, J16, K7, K9, K11, K13, K15, K16, L6, L8, L10, L12, L14, L16, M7, M9, M11, M13, M15, M16, N3, N6, N15, N16, P6, P7, P8, P10, P11, P12, P14, P15, P16, R6, R8, R9, R10, R12, R14, R16, T6, T7, T9, T10, T11, T12, T13, T18, T19, T20, U1, U2, U6, U8, U9, U10, U11, U18, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, W2, W4, W6, W8, W10, W13, W16, W19, W20, Y1, Y2, Y4, Y6, Y8, Y10, Y13, Y16, Y19, Y20

2.3.3 Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 6: Reference Resistor Values in VS3000

Pin Name	Ball #	Resistor Value [ohms] (1% tolerance)	PU/PD
DHDI0_RREXT	E6	1K	PD to VSS
HDBT_REXT	T8	4.12K	PD to VSS
HDMI_RX_RREF	R11	1.62K	PD to VSS
HDMI_TX_REXT	R13	1.62K	PD to VSS
USB_TXR_RKL	G12	200	PD to VSS

2.3.4 Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix
A	VSS	DHDI0_1N	DHDI0_2N	DHDI0_3N	DHDI0_CKN	DHDI0_4N	DHDI0_5N	DHDI0_6N	DHDI0_7N	DHDI0_8N	DHDI1_8N	DHDI1_7N	DHDI1_6N	DHDI1_5N	DHDI1_4N	DHDI1_CKN	DHDI1_3N	DHDI1_2N	DHDI1_1N	VSS	A
B	DHDI0_0N	DHDI0_1P	DHDI0_2P	DHDI0_3P	DHDI0_CKP	DHDI0_4P	DHDI0_5P	DHDI0_6P	DHDI0_7P	DHDI0_8P	DHDI1_8P	DHDI1_7P	DHDI1_6P	DHDI1_5P	DHDI1_4P	DHDI1_CKP	DHDI1_3P	DHDI1_2P	DHDI1_1P	DHDI1_0N	B
C	DHDI0_0P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DHDI1_0P	C
D	VSS	VSS	VSS	NC_D4	NC_D5	VSS	JTAG_TCK	JTAG_TMS	JTAG_TDO	RESET_IN	MAIN_HDI_RDY_IN0	MAIN_HDI_RDY_IN1	MDC_M	MSIO_RX0	MSIO_RX3	MSIO_TX3	MSIO_TX0	USB_VBUS0	USB_ID0	VSS	D
E	SGMAC_T_TXP	SGMAC_T_TXN	FU_E3	VSS	VSS	DHDI0_RREXT	VSS	JTAG_TRST	JTAG_TDI	RESET_SEL	MAIN_HDI_RDY_OUT0	MAIN_HDI_RDY_OUT1	MDIO_M	MSIO_RX1	MSIO_RX4	MSIO_TX4	MSIO_TX1	VSS	USB_DP	USB_DM	E
F	SGMAC_T_RXP	SGMAC_T_RXN	NC_F3	VSS	GPIO64	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RESET_OUT	MSIO_RX2	MSIO_RX5	MSIO_TX5	MSIO_TX2	USB_DRVVBUS	VSS	VSS	F
G	SGMPHY_TXP	SGMPHY_TXN	FU_G3	GPIO0	GPIO1	VDDA8	VDDA	VDDA8	VDDA	VDDA8	VDDA	USB_TXR_RKL	VSS	VDDIO18	VSS	MAC_RMII_TXD0	MAC_RMII_RXD0	MAC_RMII_TXD1	MAC_RMII_CLK	FU_G20	G
H	SGMPHY_RXP	SGMPHY_RXN	FU_H3	GPIO2	GPIO3	VDDIO18	VSS	VDD	VSS	VDD	VSS	VDDA_33	VSS	VDD	VSS	MAC_RMII_TXEN	MAC_RMII_RXD1	MAC_RMII_RXDV	QSPI_D3	QSPI_D1	H
J	FU_J1	VSS	GPIO65	I2C_SLV0_SCL	I2C_SLV0_SDA	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO18	VSS	I2S4_RX_D3	I2S4_RX_D2	QSPI_D2	QSPI_D0	J
K	GPO6	SPDIF_OUT	SPDIF_IN	I2C_MSTR1_SCL	I2C_MSTR1_SDA	VDDA	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	I2S4_RX_D1	I2S4_RX_D0	QSPI_CSN	QSPI_CLK	K
L	GPO5	CIR_OUT	CIR_IN	I2C_SLV1_SCL	I2C_SLV1_SDA	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO18	VSS	I2S4_TX_D3	I2S4_TX_D2	I2S4_RX_WCLK	I2S4_RX_BCLK	L
M	GPO4	GPO3	GPO2	GPO1	GPO0	VDDIO18	VSS	HDBT_VDDA	VSS	HDBT_VDDA	VSS	VDD	VSS	VDD	VSS	VSS	I2S4_TX_D1	I2S4_TX_D0	I2S4_TX_WCLK	GPO8	M
N	UART_TX_T	UART_RX_T	VSS	RIF_UART_TX3	RIF_UART_RX3	VSS	VDDA8	HDBT_VDDA	VDDA8	HDBT_VDDA	VDDA8	VDDA	VDDA8	VDDA	VSS	VSS	RMII_TXD1	RMII_TXD0	GPO7	I2S4_TX_BCLK	N
P	GPO4	RIF_UART_TX2	RIF_UART_RX2	I2C_SCL_SLAVE_H	I2C_SDA_SLAVE_H	VSS	VSS	VSS	VDDA_33	VSS	VSS	VSS	VDDA_33	VSS	VSS	VSS	RMII_TXEN	RMII_RXER	RMII_RXDV	RMII_RXD0	P
R	GPO5	RIF_UART_TX1	RIF_UART_RX1	I2C_MSTR0_SCL	I2C_MSTR0_SDA	VSS	NC_R7	VSS	VSS	VSS	HDMI_RX_RREF	VSS	HDMI_TX_REXT	VSS	HDMI_TX_HPD	VSS	MDIO_S	MDC_S	RMII_RXD1	RMII_CLK	R
T	GPO6	GPO7	I2C_SCL_MASTER_H	RIF_UART_RX0	DBG_RX	VSS	VSS	HDBT_REXT	VSS	VSS	VSS	VSS	VSS	DDC_SDA_RX	CEC_RX	V5_TX	CEC_TX	VSS	VSS	VSS	T
U	VSS	VSS	I2C_SDA_MASTER_H	RIF_UART_TX0	DBG_TX	VSS	NC_U7	VSS	VSS	VSS	VSS	HPD_RX	V5_RX	DDC_SCL_RX	FU_U15	DDC_SDA_TX	DDC_SCL_TX	VSS	HDMI_TX_TMDSDATAP2	HDMI_TX_TMDSDATAN2	U
V	HDBT_XTAL_OUT	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HDMI_TX_TMDSDATAP1	HDMI_TX_TMDSDATAN1	V
W	HDBT_XTAL_IN	VSS	HDBT_0_TR_P	VSS	HDBT_1_TR_P	VSS	HDBT_2_TR_P	VSS	HDBT_3_TR_P	VSS	HDMI_RX_TMDSCLKPA	HDMI_RX_TMDSDATAPA0	VSS	HDMI_RX_TMDSDATAPA1	HDMI_RX_TMDSDATAPA2	VSS	HDMI_TX_TMDSCLKP	HDMI_TX_TMDSDATAP0	VSS	VSS	W
Y	VSS	VSS	HDBT_0_TR_M	VSS	HDBT_1_TR_M	VSS	HDBT_2_TR_M	VSS	HDBT_3_TR_M	VSS	HDMI_RX_TMDSCLKNA	HDMI_RX_TMDSDATANA0	VSS	HDMI_RX_TMDSDATANA1	HDMI_RX_TMDSDATANA2	VSS	HDMI_TX_TMDSCLKN	HDMI_TX_TMDSDATAN0	VSS	VSS	Y
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix

Figure 9: VS3000 Ball Diagram

3 Functional Description

3.1 HDBaseT Interface

The native application flows (Ethernet, USB, Video, Audio, Control) that are connected to the VS3000 IC are converted inside the IC into HDBaseT packets and then transmitted over the HDBaseT link to a VS3000 IC on the other side of the link, where the HDBaseT packets are converted back their native application flows.

The HDBaseT packets are transmitted over the HDBaseT link using Dynamic PAM Modulation, (PAM16/PAM8/PAM4) – depending on the payload type. This ensure the delivery quality of specific types of data or control information.

VS3000 chips use a four-pair STP/UTP cable to transfer HDBaseT data over a CATx cable. Figure 10 illustrates conceptual schematics of how the VS3000 devices should be connected to the UTP cable when the link is not used to transfer power.

The four-differential HDBaseT pairs in the VS3000 are connected to a transformer and to pull-up resistors. The transformer is connected to the STP/UTP cable via an RJ45 connector.

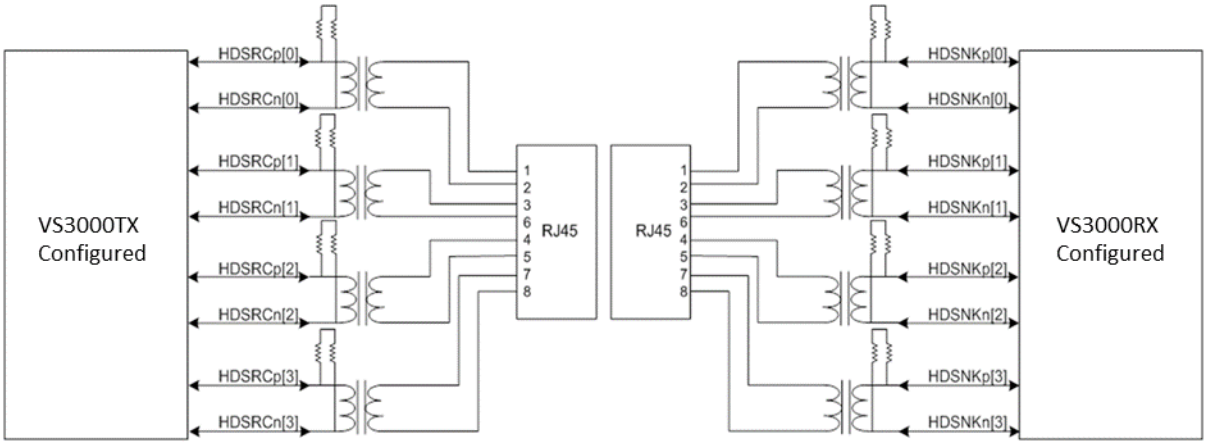


Figure 10: Link Connection Example

The pair order in the VS3000 HDBaseT interface may be swapped. The HDBaseT PHY automatically detects pairs coupling. Three different configurations are supported: straight, crossover and semi-crossover as shown below:

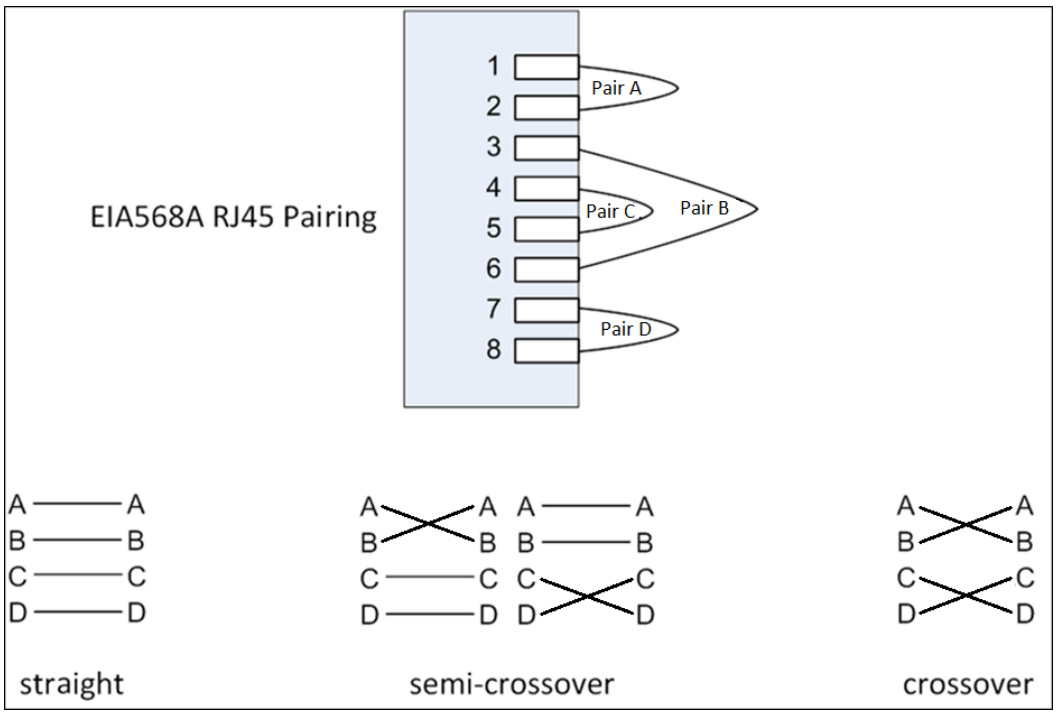


Figure 11: RX and TX Pair Coupling

Additional swapping of the **A -> D and B ->C pairs** to simplify PCB layout in cases that RJ45 connector is installed beneath the PCB (avoid crossover of lanes). This swapping is configured using firmware parameter: PCB_Swap_Config (0.3.1.21). Refer to AN3015 for detailed description.

3.1.1 HDBaseT Operational Modes

The VS3000 runs in the following HDBaseT operation modes:

- Partner Detect mode
- Low Power Partial Functionality (LPPF), with 2 sub-modes of operation:
  - LPPF1
  - FLPPF1
- Active HDBaseT (ACTIVE)
- Long Reach (LR)

During transitions between HDBaseT Operation Modes, there is no signal continuity on the chip interfaces.

3.1.1.1 Partner Detect

Partner Detect (PD) mode is an operation mode of the VS3000 PHY and is one of its low power modes. In this mode, the HDBaseT port detect and identify its link partner and resolve the next mode of operation.

3.1.1.2 Low Power Partial Functionality (LPPF)

In Low Power Partial Functionality (LPPF) mode, a low-power communication link is established between two HDBaseT devices:

- LPPF1 – the link is operated at 3.9Mbps over C&D pairs allowing only slow bit rate T-Adaptor to operate
- FLPPF1 – Same as for LPPF1, but operating in 20Mbps.

3.1.1.3 Active HDBaseT (ACTIVE)

In Active HDBaseT (ACTIVE) mode, the HDBaseT port establishes a high throughput link with its link partner using downstream/upstream sub-links.

3.1.1.4 Long Reach (LR)

Long Reach (LR) mode enables operation over longer cable runs (up to 150m/492ft) through the reduction of the symbol rate over the HDBaseT link. The VS3000 is fully interoperable with VS2000 and VS100 IC, Long Reach mode.

3.1.1.5 Events

The table below describes the events leading to Operating Mode changes.

Table 7: Operating Mode Events

Event Name	Description
Link Loss	Any event that causes a link loss
Operation Change Mode Request	As defined in the HDBaseT Specification
Wakeup	Event causing a transition from LPPF to ACTIVE
Standby	Event causing a transition from ACTIVE to LPPF

3.1.1.6 Auto-LPPF Functionality

Mode transitions between Active and Low-Power modes are possible through different mechanisms:

- Manual control using Host Interface parameters to specify the required operating mode. Mismatches between the requested operating modes of the link partners are resolved.
- Automatic mode transitions based on certain events (“Auto-LPPF”)

Auto-LPPF allows for VS3000 devices to enter and exit LPPF mode without the intervention of any external control element (such as an on-board controller). Trigger events can be defined, the presence - or absence - of which result in the mode transition. These triggers are as follows:

- HDMI video (TMDS clock)
- USB traffic

The triggers are configurable via boot-time (bring-up) parameters, which in turn defines the exact behavior of the Auto-LPPF mechanism. Auto-LPPF can interoperate with devices based on VS2000 and VS100 link partners, as well as with link partners operating in manual mode.

Refer to *Valens Application Note AN3015 – Firmware Parameter Descriptions* for information on the Auto-LPPF configuration settings.

3.2 Double High Definition Digital Interface (DHDI)

The VS3000 IC contain two independent DHDI digital ports for inter-chip interface, which is used to deliver HDBT T-Packets. Each DHDI port enables the transfer of HDBaseT packets (at speeds of 16 Gbps) directly between the VS3000 and another device that supports the DHDI interface.

DHDI is a multi-purpose high-speed interface that contains 10 bi-directional high speed lanes (LVDS). 9 lanes are data lanes and 1 lane is the clock lane. Each lane can support up to 2Gbps with 8b/10b coding.

The VS3000 IC's DHDI bus provides an interconnection interface to other VS3000 ICs on the same PCB. And is used to transfer HDBaseT packets between two ICs on a board in a way similar to the transfer of HDBaseT packets over an HDBaseT link.

The DHDI interface is composed of 9 Lane x 2Gbps for data, where each Lane is bi-directional, differential, plus a single clock line. While two devices are connected via their DHDI interface, one side is defined as the master and the other as the slave, where the master is the side that is providing the clock. The number of Lanes that are active and the direction of each is programmable.

3.2.1 Setting DHDI Bus Mode of operation

The DHDI bus rate of operation and direction can be configured together with its master/slave link functionality.

3.2.2 Setting DHDI Bus Rate of Operation

The DHDI bus can operate at different rates. In the VS3000, the DHDI bus can be configured to operate at a rate following rates:

- 16G TX / 2G RX (T8R1)
- 2G TX / 16G RX (T1R8)
- 8G TX / 2G RX (T4R1)
- 2G TX / 8G RX (T1R4) The rate of the DHDI bus is pre-determined, static and is specified in each IC's configuration file.

3.2.3 Setting the DHDI Bus Link Master/Slave Role

A VS3000 IC is assigned a role when establishing a DHDI link with its partner.

One of the VS3000 ICs is assigned a DHDI master role, while the second VS3000 IC is assigned a DHDI slave role. The partnering role is predetermined and is part of each IC's configuration file.

The figure below depicts the DHDI connectivity between two VS3000 ICs, example for DHDI0:

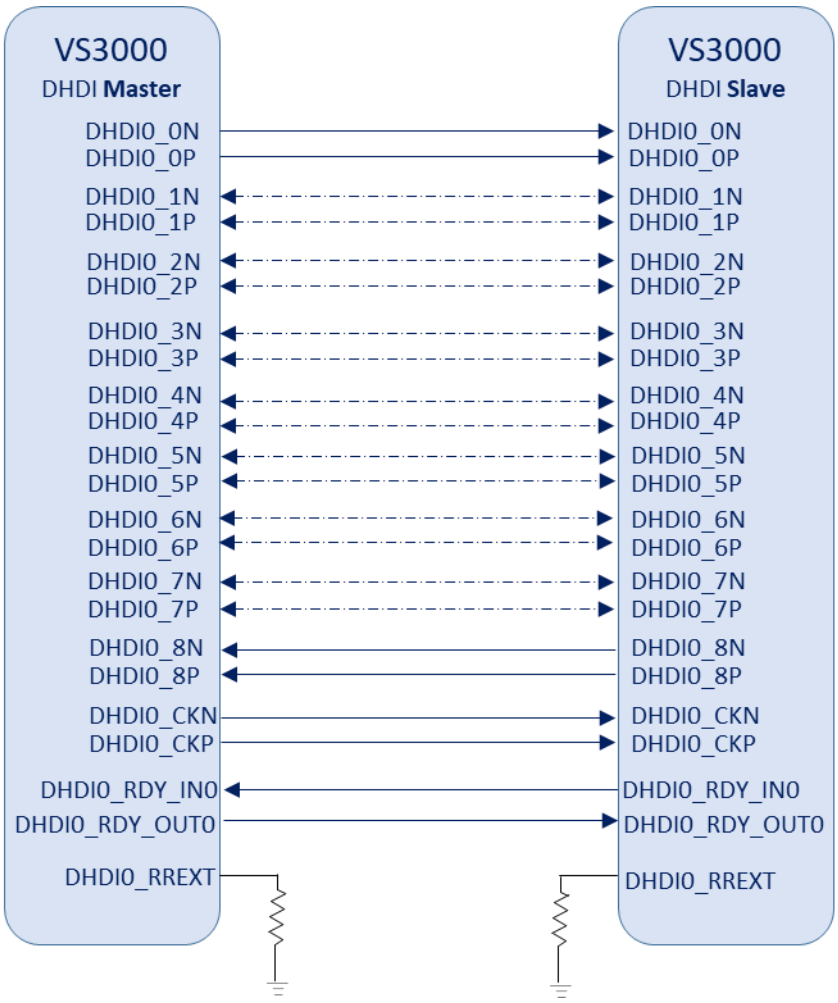


Figure 12: DHDI Bus Detailed Signals Connectivity

The DHDI_RDY_IN to DHDI_RDY_OUT and DHDI_RDY_OUT to DHDI_RDY_IN connectivity option can also be supported using the configuration file. The default configuration is DHDI_RDY_IN to DHDI_RDY_IN and DHDI_RDY_OUT to DHDI_RDY_OUT

NOTE

Further details are provided in *Valens AN3015 - Management application note*.

3.3 T-Adaptors

The VS3000 uses T-Adaptors to tunnel native traffic over HDBaseT links. The VS3000 supports the following T-Adaptors:

- HDMI (see section 3.3.1)
- Ethernet (see section 3.3.2)
- USB (see section 3.3.3)
- UART (see section 3.3.4)
- I^2C (see section 3.3.5)
- S/PDIF (see section 3.3.6.2)

- I²S-4 (see section 3.3.6.3)
- IR - Infrared (see section 3.3.7)
- MSIO (see section 3.3.8)

3.3.1 HDMI Interface

The VS3000 HDMI interfaces, are HDMI 2.0-compatible. The HDMI T-Adaptor interface ports are composed of:

- HDMI-In Port
- HDMI-Out Port

HDMI In and HDMI-Out ports can be activated concurrently

Receiving HDMI In traffic from a source, converting the traffic into HDBaseT packets (T-packets) and forwarding them to the link. On the sink side, the HDMI Out interface extracts T-packets with HDMI traffic from the HDBaseT link, converts them back to HDMI and transmits them via the HDMI Out port. Concurrent operation of the HDMI In and HDMI Out is supported and can be used for local monitoring.

Each of the HDMI Ports support the following:

- 18Gbps HDMI 2.0 TMDS
- Data Display Chanel (DDC)
- Consumer Electronic Control (CEC)
- Audio Return Channel (ARC)
    - The VS3 support for the “HDMI Ethernet and Audio Return Channel (HEAC)” is only for the ARC signal. The support is provided over the SPDIF audio T-Adaptor at the upstream direction. There is a need for external device to convert the ARC signal to SPDIF.

Two types of HDMI signals:

- TMDS Signals – includes differential data signals and the differential clock signal.
- HDMI Control Signals – includes all control signals defined in the HDMI 2.0 standard (DDC [EDID, HDCP, SCDC], 5V, HPD, and CEC)

The TMDS signal might be encrypted for security reasons. The HDCP model, defined by the HDMI standard, together with the HDCP model, defined by the HDBT standard, are used, as defined by paragraph 3.3.1.5

3.3.1.1 TMDS Signals

This group contains four pairs of unidirectional differential signals:

- Three differential pairs are used for the HDMI serial data transfer. The data is driven by a TMDS transmit PHY on the VS3000 chip or received by the VS3000 chip. The data rate on the TMDS data line can reach up to 6 GHz.

- The fourth differential pair is the TMDS clock that is generated by the HDMI transmitter. The frequency of the clock signal is one tenth of the actual serial data rate. The HDMI PHY receiver uses this clock signal to generate the serial clock used for HDMI data recovery.

The VS3000 HDMI incorporate specialized capabilities suited to dealing with the broad bandwidth of TMDS signals and varying HDMI cable lengths in order to maintain signal quality. For example:

- A TMDS driver with configurable signal pre-emphasis capabilities.
- The VS3000 transmitter supports a double termination feature.
- The VS3000 HDMI receiver uses an internal adaptive equalizer to improve its signal detection capabilities. The adaptive equalization process is done automatically after the receiver powers up and the optimal equalizer (in terms of BER) is selected.
- The receiver handles two termination types – AC and DC termination.
- The 3 HDMI data lanes in the VS3000 are swappable (1, 2, 3 <-> 2, 3, 1).

3.3.1.2 HDMI Control Signals

The VS3000 provides 2 HDMI interfaces – HDMI IN and HDMI OUT. The following HDMI signals are supported:

- **HPD** – This signal is an HDMI Rx device output that is sent by sink HDMI equipment in the direction of source HDMI equipment, indicating that the sink E-EDID memory is available for reading. The Hot Plug Detect pin can be asserted only when the +5V Power signal from the source is detected.
- **5V** – This signal is an HDMI Tx device output sent by source HDMI equipment in the direction of sink HDMI equipment. The HDMI 5V signal is pass-through (by default) – that is, it is only shown on the VS3000 output when an HDBaseT link is established and the HDMI Source is connected and is outputting its 5V control signal.
- **CEC** – The CEC line is used for high-level user control of HDMI-connected devices.
- **DDC** – This is a two-wire bidirectional I^2C interface used for HDMI control. Any HDMI device connected to a VS3000 must support the I^2C clock stretching mechanism.

Note that the HDMI specification requires special treatment for these signals such as pull-up or pull-down resistors. You must implement these requirements on your board according to the HDMI specification.

3.3.1.3 HDMI DDC Control Behavior

HDMI Control Behavior, to include 5V and HPD indications and EDID information exchange, is as follows:

- When connected to VS100:
  the EDID information exchange process is starting when HPD signal is detected by the VS3 at the source or sink side. The DDC bus is delivered over the HDBT link using T-Packet. This method is involved with longer DDC turnaround time, and subjected to DDC stretching.

- When connected to VS2000 or VS3000:
  The DDC bus is terminated by the VS3000 and by the VS2000 at each side and the EDID information is delivered to the device at the source side over HDBaseT link. The VS3000 (or VS2000) device at the source side is providing the EDID information, received over the Link, on its local DDC bus, towards the source device.

3.3.1.3.1 EDID Manipulation

The VS3000 is able to manipulate the EDID information fetched from the screen, and is crossing the HDBT domain. EDID manipulation is required to make sure that the display resolution will not exceed the maximum VS3000 supported resolution and pixel rate. Configuration Options:

- No EDID manipulation is activated
- Dynamic EDID manipulation is activated: The Sink EDID information is replaced with a lower resolution EDID information, to make sure that the source will not send Video signal that exceed the max VS3000 supported resolution, for example delivery of HDMI 2.1 non supported resolutions.
- Static EDID manipulation is enforced: The VS3000 at the source side reply with a static pre-configured EDID information, regardless of the EDID received from the sink side.

3.3.1.3.2 SCDC Support

The VS3000 support termination of the SCDC channel over the DDC bus, as defined the HDMI 2.0 standard, in order to manage, control and operate an HDMI 2.0 link segment.

Support SCDC “Read Request” (RR) feature, to enable a sink side to notify a source side, in real time, on link status change.

3.3.1.4 HDMI CEC Control

VS3000 support the delivery of the CEC bus in between the two ends of the HDBaseT domain, using the termination mode:

- The CEC bus is terminated by the VS3000 on each side. The CEC data detected by VS3000 over the bus is send using HDBaseT packets to the peering VS3000. The peering VS3000 is sending the data over its CEC bus, once detecting that the bus is free.

3.3.1.5 HDCP

The VS3000 HDMI-In and HDMI-Out interfaces support HDCP for delivery of secured HDMI signal end-to-end, using encryption. Supporting HDCP 1.4 and HDCP 2.2.

Each HDCP session is started with security negotiation, to include authentication and authorization, to validate the peering device and to exchange cryptographic keys. The negotiation may be done end-to-end, between the encryption device on the source side and the decryption device on the sink side. In case that one or more HDMI repeaters are located along the path between source and sink nodes, then the negotiation is done in “segments”, i.e. between the source device and the first HDMI repeater, then between the 1st HDMI repeater to the next HDMI repeater, and so on until the last HDMI repeater negotiate with the sink device.

The HDMI HDCP negotiation is defined over the HDMI DDC channel, and the negotiation sessions are subjected to transaction timeouts defined by the HDMI HDCP standard.

The HDCP configuration support:

- Pass-through mode – security negotiation is done between the peers directly, this require longer DDC turnaround time and is subject to the DDC stretching time.
- Termination/conversion mode – negotiation is done in “segments” and VS3000 act as HDCP repeater. Conversion between HDCP2.2 (source device) to HDCP1.4 (sink device) can take place as allowed by the HDCP standard (if Stream Type is not "Type 1").

In case that an HDMI signal is delivered over HDBaseT domain (link/daisy chains/network), it is desired that the edge nodes of the HDBT domain play as termination points for the HDCP session (emulating the functionality of HDMI repeater), shortening the HDCP negotiation turnaround time, guaranteeing successful negotiation process with the source/sink devices.

The HDBaseT standard have defined video security mode to deliver HDCP sessions over HDBaseT domain, to enable interoperability in between different HDCP types (1.4 or 2.2) of sink and source devices. This also includes the case that a single encrypted video stream is duplicated by the HDBaseT domain to multiple sink devices, each with different type of HDCP encryption. This mode is designated as HDCP 2.2T and is tolerated to longer negotiation timeouts.

To deliver encrypted video stream over an HDBaseT domain, an HDMI HDCP stream received from the source side and encoded as HDCP 1.4 or HDCP2.2, is converted by the edge nodes of the HDBT domain to HDCP 2.2T. On the sink side, this stream is converted back to HDMI HDCP 1.4/2.2 towards the sink device. This conversion at the ingress side is involved with termination of the incoming HDBT 1.4/2.2 session and initiating of an HDCP 2.2T continuation session. The VS3000 is involved in two negotiation processes; one with the source device to terminate the received HDCP session and one with the VS3000 on the sink side, to initiate the HDCP 2.2T session. On the egress side, the conversion is involved with negotiation to termination the incoming HDBaseT 2.2T session and with another negotiation to initiate HDCP 1.4/2.2 continuation session towards the sink device.

3.3.2 Ethernet PHY System

3.3.2.1 General

The VS3000 functions as a 1GbE or a 100BaseTX PHY device, enable to seamlessly deliver the Ethernet signal end-to-end over an HDBaseT link. The VS3 Ethernet port support SGMII (1000BaseT or 100BaseT) or RMII (100BaseT) interfaces, supporting Full Duplex mode.

Figure 13: VS3000 Ethernet Interfaces

Selecting the preferred interface is done by:

- Automatic negotiation with the peer
- Pre-configured option based on strap pin or configuration file

The VS3 supports the Serial Management I/F (MDIO) to an external Ethernet PHY. The MDIO is a PHY management interface, used to read and write the control and status registers of the PHY which are used to configure each PHY before operation, and to monitor the link status during operation.

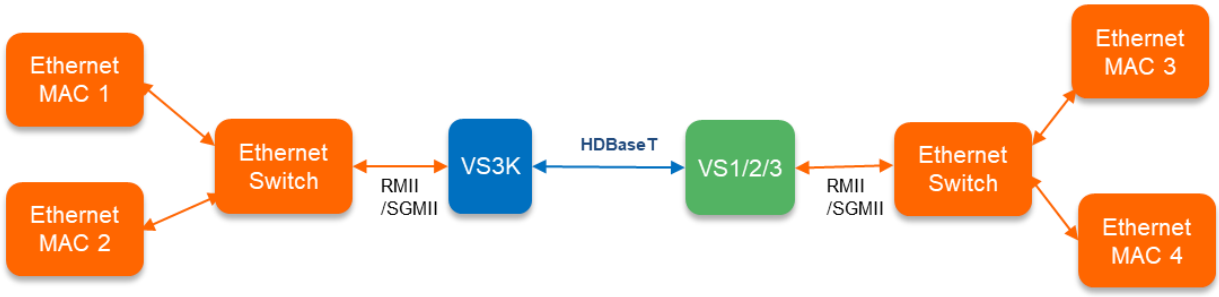


Figure 14: VS3000 Ethernet System

3.3.2.1.1 RMII

The VS3000 supports also the Reduced Media Independent Interface (RMII). This interface includes signals transmitted by the Ethernet MAC entity and to the Ethernet MAC entity.

Similarly to the Ethernet MAC notation, signals with the prefix “PHY_RMII_TX” are input signals to the VS3000 IC, while signals with the prefix “PHY_RMII_RX” are output signals from the VS3000 IC.

The default speed mode of the RMII interface is 100 Mbps and cannot be changed.

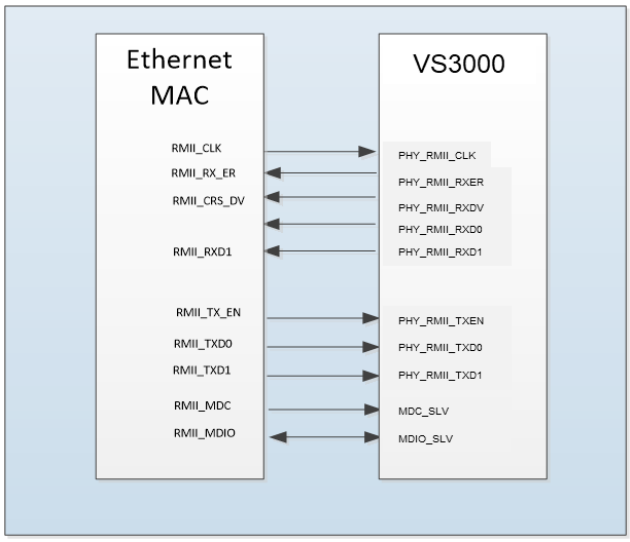


Figure 15: VS3000 RMII Interface

3.3.2.1.2 SGMII

The VS3000 IC supports the Serial Gigabit Media Independent Interface (SGMII). This interface includes two differential pairs of signals – a receive data pair and a transmit data pair. Signals with the prefix “PHY_SGMII_RX” are input signals to the while signals with the prefix “PHY_SGMII_TX” are output signals from the VS3000 IC.

The default speed mode of the SGMII interface is 1Gbps. It can also be configured to work in 100Mbps mode.

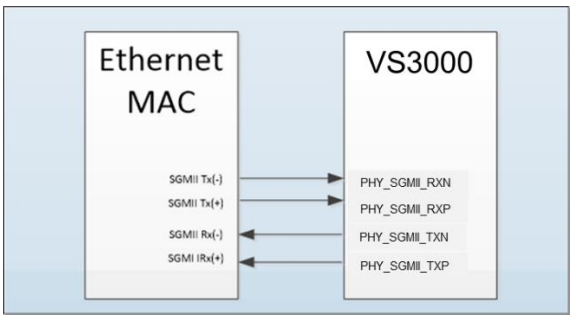


Figure 16: VS3000 SGMII interface

NOTES

A MAC device must be present on both sides of each HDBaseT link segment. In other words, there must be Ethernet termination next to each HDBaseT port since HDBaseT networking does not handle Ethernet packet routing and switching.

3.3.2.2 Serial Management I/F (MDIO)

The VS3000 chip supports the MII management interface over the MII_MDIO and MII_MDC pins. This is a two-bit interface (a bidirectional serial data bit and a clock signal) that allows addressing the PHY management registers by a MAC device. Only the MAC can initiate MDIO transactions, which can be either write (to control registers) or read (from status registers).

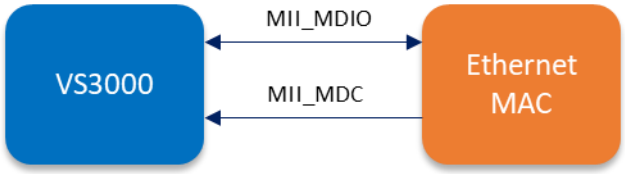


Figure 17: MDIO Topology

The IEEE 802.3 standard defines three different register groups:

- Basic (addresses 0 – 1)
- Extended (addresses 2 – 15)
- Vendor Specific (addresses 16 – 31)

The VS3000 supports SMI registers 0 through 6 as required by Clause 22 of the IEEE 802.3 standard. Non-supported Extended registers and Vendor Specific registers will be read as hexadecimal “FFFF”.

The device’s MDIO/MDC PHY Address default value is '00000'. It may be configured using the parameter.

MDC/MDIO timing, frame structure and a full registers description is as defined by clause 22 of the IEEE 802.3 standard.

3.3.3 USB Interface

The VS3 includes USB2.0 support for seamlessly extending USB2.0 connectivity over the HDBaseT domain. These components include:

- Embedded USB2.0 PHY transceiver
- Two types of USB interfaces: USBD (Device) and USBH (Host)

The VS3000 IC provides:

- Simple plug-and-play user experience
- USB tunneling over an HDBaseT link
- Point-to-point connectivity and daisy chain topologies (multiple hops)
- Multiple, concurrent USB device sessions with a single USB host
- Support for multiple USB hosts in daisy chain topologies
- Supports smart devices with role reversal applications (car play like – future support)

USB over HDBaseT, point-to-point connectivity is illustrated in the figure below.

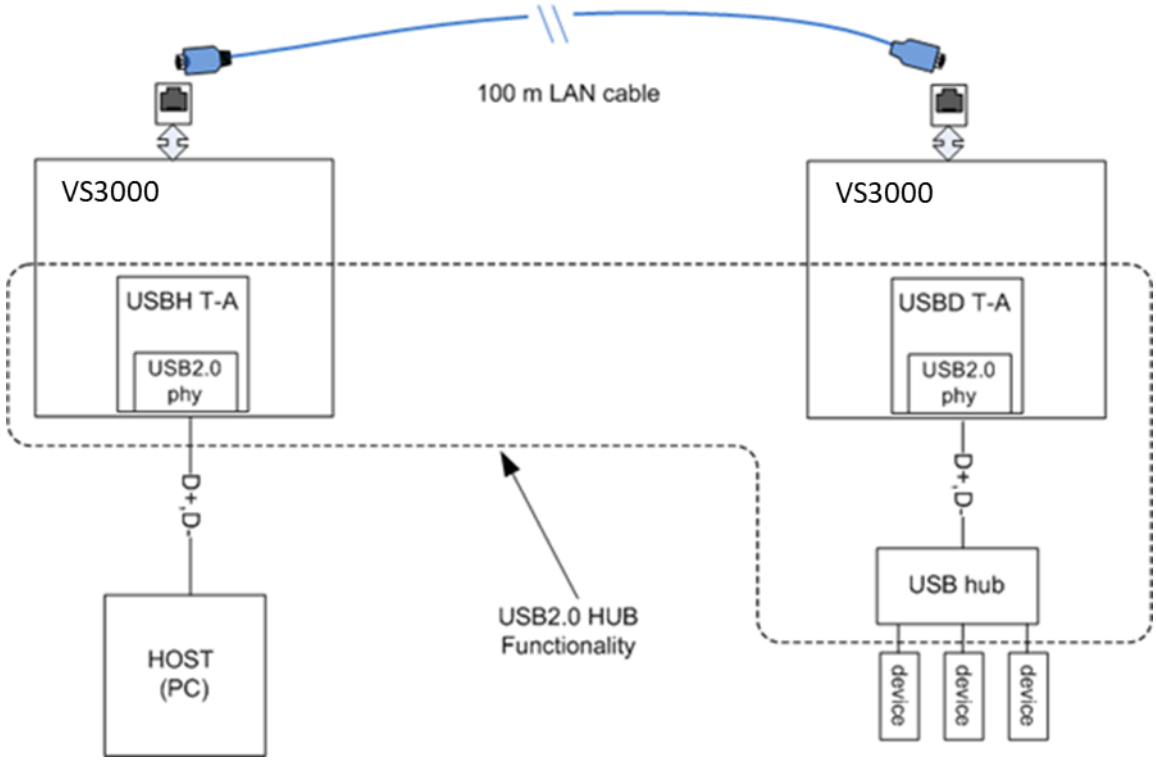


Figure 18: USB2.0 Extension Over HDBaseT Link

3.3.3.1 Functional Description

The VS3000 IC includes a USB 2.0 T-Adaptor block. The T-adaptor block is responsible for converting USB 2.0 traffic into T-packets for transfer over the HDBaseT link. The block is configured by VS3000 firmware as either:

- A USB T-Adaptor to which a USB *host* can be connected to (USBH T-Adaptor), or
- A USB T-Adaptor to which a USB *device* can be connected to (USBD T-Adaptor)

3.3.3.2 Modes of HDBaseT USB T-Adaptors

3.3.3.2.1 Virtual USB Hub mode

An HDBaseT link with a USB Host T-adaptor on one end and a USB Device T-adaptor on the other end can be considered by the USB 2.0 Host as a USB 2.0 Hub with an upstream port and downstream port.

In a Virtual USB Hub mode, the USBH T-Adaptor (the VS3000 interface to which a USB host can be connected) emulates a USB hub to the USB host that it is connected to. It also performs an enumeration of the USB device connected to the remote end node (or to several USB devices when using HDBaseT daisy chain topology). As a result, the USB host sees a flattened tree that includes all USB devices.

By default, the USBH T-Adaptor is configured to operate in Virtual USB Hub mode.

In a daisy chain topology, several USB hosts can be connected and each can be configured (via HDBaseT configuration) to work with unique, specific USB device ports.

3.3.3.2.2 Plain USB Device Mode

An HDBaseT link with a USB Host T-adaptor on one end and a USB Device T-adaptor on the other end can be considered as a transparent wire.

Plain USB device mode can be applied to a USBH T-Adaptor via the VS3000 IC configuration file.

In this mode, called Plain USB Device Mode, only a single USB device is supported on the downstream port. (In this mode, there is no HDBaseT enumeration process that takes place)

3.3.3.2.3 Hybrid mode

An HDBaseT USBH T-Adaptor may be configured to work in a Hybrid mode. In the Hybrid mode, the Host USB T-Adaptor starts to work in a Virtual USB Hub mode. This mode can be dynamically changed to a Plain USB Device mode. (Either by an external host controller command or when certain conditions are met such as a unique USB device which is being connected to the system). If the topology is supported by the host includes several USB ports, the transition from USB Virtual Hub mode to Plain USB Device mode will stop USB services to all USB ports except a single USB port which was set to work in this mode. (Either by an external host controller command or when certain conditions are met)

Once returning to a USB Virtual Hub mode (Either by an external host controller command or when certain conditions are met), USB services to all other USB ports will be resumed.

3.3.3.3 Supporting Smart Devices with role reversal Applications

When operating as a USBD T-Adaptor, the VS3000 IC can detect on its USB port, hand-held devices with applications that require USB Host and USB Device role reversal. Upon such detection, the VS3000 IC can reconfigure itself (if needed) to work as a USBH T-Adaptor, just as the remote VS3000 IC simultaneously performs the opposite role reversal, reconfiguring itself to work in USBD T-Adaptor mode.

When the smart device is disconnected from the port, both VS3000 ICs will re-configure themselves to work in their original USB T-Adaptor modes.

Only a single smart device can be serviced at once. If additional smart devices will be connected, they will be treated as standard USB devices.

3.3.3.4 Number and Type of USB 2.0 Devices Supported

The VS3000 supports USB 2.0 High Speed, Full Speed and Low Speed devices. The total number of devices connected and working simultaneously (in a combination of USB device types) is configurable but cannot exceed a total of 7 devices. Refer to the table below for the number of supported endpoints:

	HS Host		FS Host	
	IN Endpoints	**OUT Endpoints**	**IN Endpoints**	**OUT Endpoints**
HS Devices	14	15	N/A	
FS/LS Devices	15	15	14	15

3.3.3.5 USB Performance

The VS3000 IC tunnels USB traffic using its built-in VLSI transport engines and internal firmware that support the USB traffic termination on both ends of the link.

The performance level of the USB channel can be tuned and is dependent on the VS3000 internal System/CPU frequency. The table below specifies the expected USB channel speed based on the VS3000 internal system/CPU clock:

Table 8: Expected USB Performance

USB Bulk Sessions	Interrupt and Control	Total USB Performance (CPU@500MHz)
1	Few Mbps	280 - 300Mbps
2 and more	Few Mbps	300Mbps

3.3.3.6 USB Bandwidth Management

The VS3000 IC supports USB bandwidth control management. USB bandwidth management can be disabled if not needed, or operated in one of two modes:

- Static bandwidth allocation
- Semi-dynamic bandwidth allocation.

USB bandwidth management settings can be specified for each specific topology use case:

- Point-to-point

- Daisy chain (and the number of USB ports in each daisy chain)

NOTE

Further details are provided *in* AN2050 – USB *application note*.

3.3.3.6.1 Static Bandwidth Allocation

When configuring the VS3000 IC to use static USB bandwidth allocation, each USB device port is given a predetermined bandwidth for USB transfers.

The USB device will then allocate the bandwidth according to the type of endpoints connected to its port. A higher priority is given to periodic transfer type endpoints than to non-periodic transfer type endpoints.

3.3.3.6.2 Semi-Dynamic Bandwidth Allocation

Initially, before any USB devices are attached, each session is allocated a minimal amount of bandwidth.

When the first active USB device is identified, its session will be given the maximum required available bandwidth. (Periodic data transfers are allotted fixed bandwidth as described in the previous sections).

When additional USB devices become active, the allocated bandwidth for each device will be re-calculated.

Bandwidth allocation is managed by the VS3000's USB Host.

3.3.3.7 USB Interoperability

The VS3000 USB2.0 is fully interoperable with the VS2000 IC's USB2.0 T-Adaptor, enable to connect USB Host and Devices between VS2000 and VS3000 devices.

3.3.4 UART T-Adaptor Functionality

The UART T-adaptor converts native UART traffic from the UART interface into HDBaseT packets. UART HDBaseT packets may be transmitted over the link to the partner device. The UART T-adaptor may be configured to two modes of operation:

- Pre-configured
- Oversampled

3.3.4.1 UART Operating Clock Frequency

The UART T-adaptor is configured to work in a specific baud rate, which can be set to any of the supported baud rate values. The supported baud rates are: 38400, 57600, 115200, 230400, 460800, and 921600.

In addition, the UART T-Adaptor can be configured to support specific character length, stop bit and parity bit information.

3.3.4.2 Working in Pre-configured mode

In this mode, the UART baud rate is known a priori to both partners. This mode is more efficient with respect to data rate consumption. It is recommended to use this mode when high UART rates are

required in LPPF1 HDBaseT modes. The table below illustrates how to configure a system to preconfigured UART mode:

Table 9: UART Pre-configured Parameter Settings

Parameter Name	Description
TAConf.UART.Mode	Pre-configured
TAConf.UART.BaudRate	The required discrete baud rate
TAConf.UART.CharLen	The required character length (5,6,7 or 8 bits)
TAConf.UART.OversampleRate	Don’t care (leave as default)
TAConf.UART.ParityBit	The required parity true/false
TAConf.UART.StopBit	The required number of stop bits (none, one or two bits)

3.3.4.3 Working in Oversampled Mode

In this mode, the UART baud rate is unknown a priori. This mode is typically used when a PC with DTE client is connected and the baud rate depends on the managed equipment which may change between setups. In oversampled mode, the UART TX and RX lines are sampled using a 1.5MHz sampling clock on one side and recovered using a recovery clock on the partner's side.

The table below illustrates how to configure a system to oversampled UART mode:

Table 10: UART Oversampled Parameter Settings

Parameter Name	Value
TAConf.UART.Mode	Oversampled
TAConf.UART.BaudRate	Don’t care (leave as default)
TAConf.UART.CharLen	Don’t care (leave as default)
TAConf.UART.OversampleRate	Fixed, read only field
TAConf.UART.ParityBit	Don’t care (leave as default)
TAConf.UART.StopBit	Don’t care (leave as default)

NOTE

When using oversampled UART in LPPF mode, the maximum supported baud rate is 115.2 Kbps.

3.3.5 I²C T-Adaptor Functionality

The VS3000 IC have two I²C master ports and two I²C slave ports. A slave port function as an I²C slave port in front of an external I²C master and a master port can function as a master I²C port in front of external I²C slaves. The I²C signals produced by an external master at one end of the session are delivered by the VS3000 over the HDBaseT domain to the slaves at the other end of the link. The I²C signals are converted to HDBaseT packets.

A VS3000 Master port should be connected to an external Slave, whilst a VS3000 Slave port should be connected to an external Master.

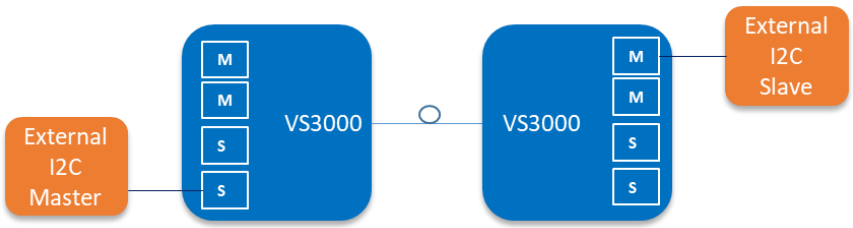


Figure 19: Valens VS3000 I²C T-Adaptors

3.3.5.1 I2C Operating Clock Frequency

The VS3000 support rates of:

- 100KHz, backwards interoperable to VS2
- 400KHz
- 800KHz

Data is transferred across the HDBaseT link bit-by-bit at the rate set by the external Master's SCL clock, and output at the far-end of the link on the VS3000's Master port.

3.3.5.2 I²C Clock Stretching

When the VS3000 acts as a slave in front of the external master for Read commands, it stretches the I²C clock to compensate for the relatively long delay of delivering the command over the HDBaseT domain to the slave side.

The host with the master I²C interface must support stretching to ensure proper functionality when working with remote devices having the I²C Slave interface.

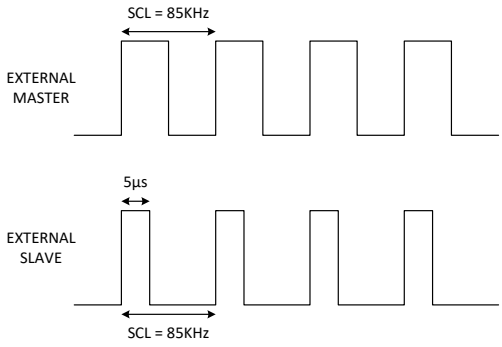


Figure 20: I²C Interface Timing Representation (Example)

Note that the Valens VS3000 I²C T-Adaptors support stretching of up to 250µS by an I²C external Slave.

3.3.6 Audio T-Adaptor

The VS3000 support the following Audio T-Adaptors.

3.3.6.1 Audio Interoperability

The VS3000 support HDBaseT sessions in between identical audio ports, as follows:

- I2S: VS3000-to-VS3000 and VS3000 to VS2000
- SPDIF: VS3000-to-VS3000 and VS3000 to VS2000
- I2S-4: VS3000-to-VS3000

3.3.6.2 SPDIF Functionality

Two SPDIF audio T-adaptors are available on VS3000 chips – one for SPDIF IN and one for SPDIF OUT. These T-adaptors convert native SPDIF audio traffic from the SPDIF input interface: *SPDIF_IN* pins, into HDBaseT packets. On the other side of the link, the SPDIF output signal is recovered via the pins: *SPDIF_OUT*.

The configuration of the SPDIF T-Adaptor is fixed. The maximum allowed audio frame rate for this interface is 192K frames per seconds.

3.3.6.3 I²S-4 T-Adaptor Functionality

Two I²S-4 audio T-adaptors are available on VS3000 chips – one IN and one OUT. These T-adaptors convert native I²S audio traffic from the I²S input interface into HDBaseT packets.

The I²S -4 bus is a serial I/F based on the original I²S bus, with additional 3 data lines. The original I²S bus is built of 3 lines: Clock, WS and Data. The I²S -4 BUS is thus built of 6 lines: Clock, WS and 4xData.

The Data bit on the data line are clocked by the I²S clock line, while the audio channels over the data line are clocked by the WS line.

The I²S-4 audio interface can be configured to work in several modes providing a wide flexibility to the system designer:

- Programmable Data Width interface (1 or 4 data lanes)
- Programmable direction of Bit Clock and Word Clock signaling
- Independent Master Clock generation for devices that require 2 or 4 times the basic bit clock frequency
- Delayed-Bit/Standard I²S audio, Left justified, Right Justified and TDM audio modes support
- Multi-stream I²S audio support in daisy chain topologies
- Session configuration: Static/pre-determined configuration, or dynamic on-the-fly configuration

- Each tunneled digital audio stream can have its own transport format/data alignment, independently of the formats in other streams (however both ends of single tunneled digital audio stream has identical transport format/data alignment).

3.3.6.3.1 Master Clock

Two additional Master Clock lines are available, one per I²S-4 port (MCLK1 and MCLK2). The Master Clock signal is generated from a PLL and can be a x1, x2 or x4 multiple of the port's Bit Clock. It can be used to provide a Master Clock input to CODEC devices with no PLL.

Clocks are re-generated with high precision and low jitter to guarantee accurate audio transmission over a wide frequency range.

Generation of the Master Clock signal and its frequency is controlled by preset configuration.

3.3.6.3.2 Supported Transport Formats/Data Alignments

The VS3000 I²S support the following formats:

- Stereo Channels: 2 audio channels are delivered on each of the I2S data lines, one for the "left speaker" and one for the "right speaker", with a total of 8 channels over the 4 data lines (7.1). The WC is used to sign the start/end of 32 bits audio block per channel. The 32 bit audio blocks may be right justified or left justified.
- TDM Channels: 16 channels are delivered on a single data line of the I²S bus, where the channels boundaries are clocked by the WC line.

The transport formats supported by different operation modes:

- A Delayed-Bit/Standard I²S audio frame
- Left Justified audio frame
- Right justified audio frame

3.3.6.3.3 Delayed-Bit/Standard I²S Audio Frame

Data is sampled on the rising edge of the Bit Clock, starting with the second clock after the transition of the Word Clock from high to low. MSB first, LSB last. Alternating left and right channel data words are transmitted over a serial data line where:

- Left Channel: Word Clock (WC) = LOW
- Right Channel: Word Clock (WC) = HIGH.

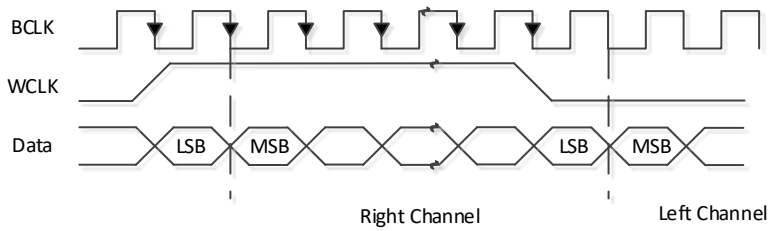


Figure 21: Delayed-Bit/Standard I²S Transport Format

The designer can configure the Polarity of the Word Clock signal.

3.3.6.3.4 Left-Justified Audio Frame

Data is sampled on the rising edge of the Bit Clock, starting with the first clock after the transition of the Word Clock from high to low. MSB first, LSB last.

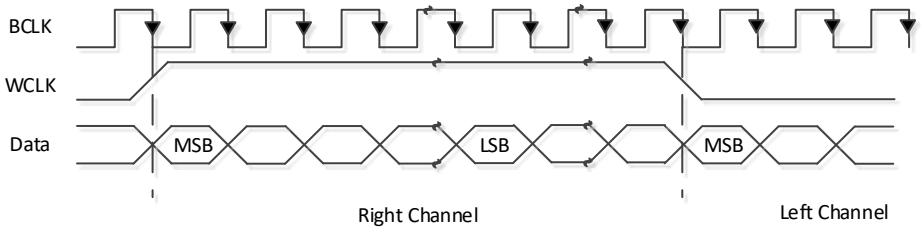


Figure 22 : Left Justified Transport Format

The designer can configure the following:

- Number of valid bits per channel (the rest are considered as non-valid)
- Polarity of the Word Clock signal

3.3.6.3.5 Right-Justified Audio Frame

Data is sampled on the rising edge of the Bit Clock and the Left channel data word may begin at any point depending upon the word length, but LSB of this data word appears after the rising edge of the Word Clock signal. Similarly, LSB of the right channel data word appears after falling edge of the Word Clock signal.

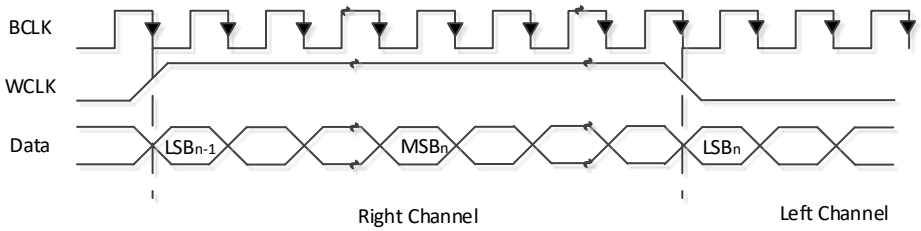


Figure 23: Right Justified Transport Format LSB outside the frame

The designer can configure the following:

- Number of valid bits per channel (the rest are considered as non-valid)
- Polarity of the Word Clock signal

3.3.6.3.6 TDM Based Audio Frames

Data is sampled on the rising edge of the Bit Clock. Number of channels and bits per channel are detected automatically by the VS3000 device based on the Word Clock (but not the number of valid bits per channel). The Word Clock in TDM mode must wrap the first TDM channel as described below. Within the channel, the number of valid bits and the data alignment (delayed-bit/left-justified/right-justified) can be configured.

A maximum of 32 TDM channels are supported. The minimum number of bits per channel is 8, the maximum number of bits per channel is 32.

An example is given in the figure below with 8 TDM channels:

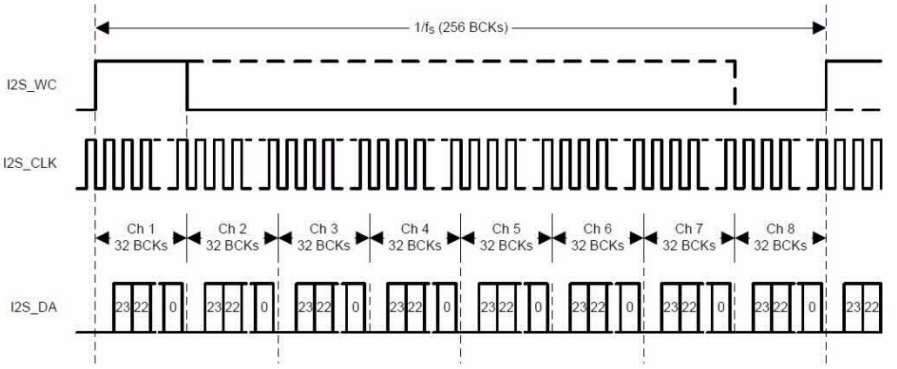


Figure 24: TDM Mode

TDM mode is automatically being detected by the VS3000 device. To allow this, the Word Clock high needs to **mark the first channel within the TDM frame** (see above).

The designer can configure the following:

- The transport format/data alignment
- In justified mode - Number of valid bits per channel (the rest are considered as non-valid)
- Polarity of the Word Clock signal

3.3.6.3.7 Frequency of operation

The maximum Bit Clock frequency of the I²S-4 interface is 25 MHz.

The I²S bit rate is calculated as follows:

Br = M * N * Fs, in which:

- Br – Bit Rate
- M – Number of bits per channel (supported: 8, 16, 18, 20, 24, 32)
- N – Number of channels (Max. 32)
- Fs – Sampling Rate (supported: 32KHz, 44.1KHz, 48KHz, 96KHz, 192KHz, 88.2KHz, 176.4KHz)

For example, in an audio stream with a sampling rate of 48 KHz, 32 bits per channel, and a total of 16 channels, the I²S bit rate in this case is 24.576 Mbps.

3.3.6.3.8 HDMI 2.0 Audio Formats (Future support)

The HDMI 2.0 Audio formats at the downstream direction are richer, comparing to those of HDMI 1.4. HDMI2.0 extracted audio, can be deliver over the I2S-4 interface to remote location. The VS3000 support the HDMI 2.0 audio formats of 1536 KHz.

3.3.6.4 ARC Support

The VS3000 can deliver the ARC (Audio return Channel) channel, from sink device to source device, using one of the VS3000 Audio channels (SPDIF, I2S-4, I2S).

Delivering of the ARC using the VS3000 SPDIF Interface is interoperable with VS2000 IC family.

3.3.7 IR T-Adaptor

The VS3000 have two independent IR interfaces and T-adaptors that may operate simultaneously, CIR-In and CIR-Out. Both CIR T-Adaptors can handle modulated and non-modulated IR signal.

The CIR T-Adaptor convert native infrared traffic from the CIR interface into HDBaseT packets at the CIR-In side and vice versa at the CIR-out side. CIR HDBaseT packets are transmitted over the link to the partner device. The IR signal input from the CIR-in signal is oversampled by the VS3000 CIR-Tx T-adaptor and transferred over the link in an HDBaseT packet format.

Both ends of the IR session (CIR-in and CIR-out) are pre-configured with the IR attributes, to include information about the signal type (modulated or non-modulated) and the signal rate.

The VS3000 have the ability to convert the IR signal polarity to maintain full interoperability with VS100 and VS2000 devices.

3.3.8 MSIO T-Adaptor

MSIO (Multi-Serial Input Output) channels allow for any low-speed data to be transferred across the HDBaseT link. Data is transferred asynchronously through oversampling of the input data – the sample rate is set by configuration to either 0.5MHz, 1.0MHz or 1.5MHz. It is recommended to use a sampling rate of 10:1, meaning that (for example) with a sample rate of 1.5MHz the maximum native data rate should not exceed 150Kb/s.

The VS3000 support 12 MSIO lines and T-Adaptor - 6 Inputs and 6 output ports. The following is supported:

- T-Adaptor is Interoperable with VS2000 (MSIO) and VS100 (PDIF)
- Sampling rates: 1.5Mbps and 0.5Mbps (VS100 & VS2000), 1Mbps (VS2000 only)

3.3.8.1 MSIO Compatibility with VS100 PDIF

In the event of V3000 Series – VS100 Series interoperation, the following general-purpose pins are connected over the HDBaseT link.

- VS3000 Series: MSIO[5:0] – Multi-Serial Input Output
- VS100 Series: PDIF[5:0] – Programmable Data Interface

NOTE

Not all of the pin connections are interoperable, please see the below table for details.

Table 11: PDIF-MSIO Compatibiity

VS010/VS100	VS3000 Interoperability
PDIF[0] **(UART function)**	**UART_RX_TA**/GPIO53 **UART_TX_TA**/GPO54/SW_STRAP[8]
PDIF[1]	-
PDIF[2]	-
PDIF[3] **(CIR function)**	**CIR_IN** **CIR_OUT**
PDIF[4]	MSIO[4]
PDIF[5]	MSIO[5]

The table is the default configuration of VS3000 interpretation of the VS100 PDIF [0]. Using FW parameter: *System.FeatureList.Pdif0ToMsio0* (0.1.11.30) the PDIF[0] is redirect to VS3000 MSIO [0].

3.3.8.2 MSIO Compatibility with VS2000

The following table describe the MSIO compatibility between VS3000 and VS2000

Table 12: MSIO Compatibiity with VS2000

VS3000	VS2000
MSIO_TX0	MSIO_DIN[0]/UART_IN/GPIO[4]
MSIO_TX1	MSIO_DIN[1]/I2S_IN/GPIO[5]
MSIO_TX2	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]
MSIO_TX3	MSIO_DIN[3]/CIR_IN/GPIO[7]
MSIO_TX4	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]
MSIO_TX5	MSIO_DIN[5]/SPDIF_IN/GPIO[9]
MSIO_RX0	MSIO_DOUT[0]/UART_OUT/GPIO[10]
MSIO_RX1	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]
MSIO_RX2	MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]
MSIO_RX3	MSIO_DOUT[3]/CIR_OUT/GPIO[13]
MSIO_RX4	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]

3.4 External FLASH Memory Interface

The VS3000 IC requires connectivity with an external FLASH memory device to upload its Firmware and its configuration file. The VS3000 IC has a QSPI interface to the external Flash memory and can work in either a single data lane (SPI mode) or quad data lane mode (QSPI mode) when accessing the external FLASH device.

During the boot sequence, the firmware reads the Flash Memory vendor ID and sets up the Flash driver parameters accordingly. In case the vendor ID is not identified, the Flash driver will use default, predefined parameters, for SPI mode and firmware configurable parameters once moving to QSPI mode.

The Flash Driver SPI default commands parameters are:

Table 13: SPI default commands parameters

Command	1st Byte	2nd Byte	3rd Byte	4th Byte	Action	Comment
READ	03h	AD1(8)	AD2(8)	AD3(8)	n bytes read until CS# goes high	80 cycles gap when CS# goes high
PP (page program)	02h	AD1(8)	AD2(8)	AD3(8)	program selected page	
CE (chip erase	C7h				erase whole chip	

External FLASH sizes supported are 64Mbit, 128Mbit, 256Mbit.

Bigger FLASH sizes can be used as well.

See list of supported Flash Memories in AN3001 Refer to the *Hardware Design Guideline Application Note* for additional information

Please contact Valens Technical Support for updated information.

3.5 External Host Interfaces

The VS3000 IC can be accessed by an external host for configuration and monitoring.

There are 3 interfaces that provide such access - the I^2C Host Interface, UART Host Interface and Ethernet Host interface. Only a single host interface is required for use by the external host and it is up to the system designer to choose the specific interface to be used. The configuration and monitoring capabilities are identical for all interfaces.

The external host runs a dedicated protocol called VCP – Valens Control Protocol (see details below) to communicate with the VS3000 IC. The VCP protocol runs on either one of the interfaces.

3.5.1 Managing the VS3000 IC

Management of the VS3000 IC is done by an external host using the Host Interface (HIF).

Host Interface commands may be issued to the chip either on the local or the remote side of an HDBaseT link. However, a command is relayed to the remote side *only if the link is active*.

In a daisy chain topology, HIF communication can be issued to any chip in the daisy chain.

HIF communication is supported by the Valens Control Protocol (VCP).

VCP is a simple, frame-level format used to forward data between a host device and a chip – over any physical layer – using *Get* and *Set* commands.

Each command is implemented using a pair of messages:

- A **write** message used to send the *Get* or *Set* request to the chip
- A **read** message used to receive the response from the chip

The VCP protocol is used to access the VS3000 IC's parameters.

The VA3000 IC has an internal Management Information Base (MIB) used to maintain various configuration and status parameters.

The MIB firmware parameter tree provides hierarchical access to parameters, enabling read and write operations.

The following rules apply to the firmware parameter tree:

- Operations can only be performed on a "leaf" of a tree.
- Each leaf may be accessed according to the following characterizations:
    - Read-only, write-only, or read-write
    - Local and/or remote access
    - Notes

3.5.2 I²C Host Interface

The I²C Host Interface is one of the 3 interfaces which can be accessed by an external host for configuration and monitoring.

The Host should be connected to the ***VS3000 IC - I²C slave interface***.

3.5.2.1 VS3000 I2C Slave address

The VS3000 I²C slave address is composed of 7 bits. The 3 LSB bits are set by hardware strap configuration and are defined by the system designer. The remaining bits are taken from the VS3000 IC configuration file.

3.5.2.2 I2C Interface speed

The VS3000 I²C host interface has a programmable baud rate and can operate at either 100 KHz, 400 KHz (default rate) or 800 KHz.

3.5.2.3 VS3000 I2C Master

The VS3000 CPU subsystem include also I²C Master that can be used for general purpose application, connecting to slave devices.

3.5.2.4 Reduced I2C host interface clock stretching time

Implementing switch matrix requires integration of several VS3000 devices and other devices controlled by MCU using I²C interface. In this case, stretching a clock on an I²C host for long periods of time may be a problem.

Current behavior - A VCP GET command is translated into a write command followed by a read command over the I²C . Clock stretching will occur from a read command till the data is ready to be transferred over the I²C .

The following mechanism is supported to reduce the clock stretching time:

- A VCP GET command will be translated to a single I²C write command.
- **Interrupt signal - GPIO2** is used to indicate to Host when data is ready.
- Upon receiving the Interrupt signal, Host issues a read I²C command to get the data.
- No additional VCP commands are required between the write and the read.

If a write is followed immediately by a read command – clock stretching *will* take place (same as current behavior).

3.5.3 UART Host Interface

The UART Host Interface is one of the 4 interfaces which can be accessed by an external host for configuration and monitoring of the VS3000 IC. The RIF_UART #1 is assigned as the Host interface signal pins (R3, R2):

- RIF_UART_RX1
- RIF_UART_TX1

3.5.3.1 UART Port Configuration parameters

The VS3000 IC UART host interface has a programmable baud rate as well as variable character length, stop bit and parity bits parameters that are configured and stored in the VS3000 configuration file.

The default baud rate is 115200 Kbps. Additional values are:

19200, 38400, 57600, 115200, 230400, 460800, 921600

It is possible to preset any of the baud rates above. This is done via the configuration file parameters. (The baud rate cannot be changed dynamically)

3.5.4 Logger Port

The logger port enables gathering log files from the VS3000 IC using the RIF_UART #0 as default.

The RIF Logger is a tool used to trigger and capture log files, to be sent to Valens support team for further investigation. The logger is operated and configured by the ValUE tool. The same port configuration as the UART Host Interface UART, apply to the Logger port.

The RIF_UART #0 is assigned as the Host interface signal pins (T4, U4):

- RIF_UART_RX0
- RIF_UART_TX0

3.5.5 Debug Port

The UART-based Debug port is used for debugging purposes, by Valens customer support only. The port is *always* available – even if no firmware is programmed in flash memory.

The following pins serve as the UART interface to the Debug port:

- DBG_RX
- DBG_TX

The speed of the Debug UART port is fixed at 115200.

The UART interface operates at the 1.8V LVCMOS level. Therefore, an external 1.8V LVCMOS-to-RS232 level shifter is required in order to utilize the debug port.

Recommendation for test point placement for using this port can be found in AN3001 HW design guidelines.

3.5.6 JTAG Interface

VS3000 IC has a standard, 5 pin JTAG interface with boundary scan capabilities. JTAG port is mainly used for Valens internal real-time Firmware debugging and for JTAG boundary scan.

The JTAG interface operates at the 1.8V LVCMOS level. An external 1.8V LVCMOS-to-JTAG level shifter is required.

Recommendation for test point placement for using this interface can be found in AN3001 HW design guidelines.

3.5.7 Ethernet Interface

The VS3000 include Ethernet Host Interface which can be accessed by an external host for configuration and management. The Ethernet interface is in compliance with the IEEE 802.3-2008 standard. The Ethernet MAC interface support:

- RMII/SGMII interfaces
- 100 Mb/s Full Duplex operation
- MII Management Interface - MDC/MDIO

4 Configuration and Management

Configuring the VS3000 chip can be achieved by the following methods:

- HW Strap Pins – Values are latched upon exiting reset
- Soft straps (GPIOs) – Asserting GPIO inputs during application bring-up
- Parameters – Configuring VS3000 parameter values in the external FLASH memory
- Host Interface – Configuring VS3000 parameters during run time or immediately after reset and before link establishment.

A VS3000 device is capable of managing its remote link partner using the host interface commands. Management messages are transferred over the main and auxiliary HDBaseT channels.

4.1 HW Strap Pins

Hardware strap pins are used to configure the chip's operational mode. These pins are sampled at the rise of the reset signal. After they are sampled, these pins regain their default run-time functionality.

Table 14: VS3000 HW Strap Pin Description

STRAP Pin	Pin Name	Default (Internal PU/PD)	Name	Description
HWStrap[1]	GPO[4]		spi4Byte	Define Flash memory address byte access 0: The external flash memory is 3 byte address memory 1: The external flash memory is 4 byte address SPI flash memory
HWStrap[2:4]	GPO[0:2]		I2CA0 - GPO[0] I2CA1- GPO[1] I2CA2 - GPO[2]	Strap bits 2-4 define the 3 LSB bits of the VS3000 configuration I2C slave device address. The 7 bit I2C address of VS3000 is set as follows: I2C address = {4'b0101, A2, A1, A0} Where A2, A1 and A0 are the values of GPO[0:2] during reset respectively.
HWStrap[11]	GPO[6]		Mem BISR (built in self-repair)	Enable strap – check the internal memories and write damaged cells into registers for self-repair. Extends boot time as the test is performed after each reset. 0: Disable 1: Enable

4.2 SW Strap Pins

The pins listed in Table 15 are used to configure firmware behavior. These pins may be left unconnected if the default internal pad resistor value is suitable for the application. You can assert these pins on your board (typically using dip-switch buttons or using external pullup/pulldown) to change the FW default configuration. These SW strap pins are only sampled upon reset.

Table 15: SW Strap Pin Description

STRAP Pin	Pin Name	Default (Internal PU/PD)	Name	Description
SWStrap[5:6]	[GPO[7]: I2S4_TX_D2]		HDBTG	HDBaseT Gender definition strap: '00': UPT / software defined (Automatic) '01': TX Source Device '10': RX Sink Device '11': Symmetric (future use)
SWStrap[7]	GPO[3]		MAC_SGMII_RMII	Define the Ethernet MAC interface used: '1': RMII '0': SGMII
SWStrap[8]	UART_TX_T		EAdaptor_SGMII_RMII	Strap bit defining the Ethernet T-Adaptor interface used: '1': RMII '0': SGMII
SWStrap[9]	GPO[8]		External Flash Not Present	If no external flash, then the ROM code will not try to access the external flash and instead wait for external host to load the execution code '0': flash exist '1': no flash present
SWStrap[10]	I2S4_TX_D3		WFH	WaitForHost_n soft strap: '0': The FW loads the parameters from the external memory update parameter section and resumes boot as usual. '1': The FW will pause its boot session, allowing a host to configure the VS3000 with HIF set/get commands.
SWStrap[12,13]	[I2S4_TX_D0: I2S4_TX_D1]		Long Reach Mode	Two strap pins indicating the HDBT long reach operation: Long reach (LR) mode request: '10' – Activate the link in HDBaseT mode '00' – Activate the link in long reach mode '01' – reserved for future long reach modes '11' – reserved for future long reach modes

				Must be deactivated using Update Parameters (LR function is currently enabled by default)
SWStrap[14]	USB_ID0		USB_ID	Strap pin that define if USB is connected to host or Device side: • USB_ID '0' – connected to a Device (USBD) • USB_ID '1' – connected to a Host (USBH)
SWStrap[15]	GPO9		AC or DC coupling	Strap pin that indicate if MAC Ethernet SGMII is using AC or DC coupling • 0: DC • 1: AC

IMPORTANT

Additional soft strap pins are reserved for future purposes and do not have any attached functionality. To make sure your design is future compatible, soft straps pins must not be tied to external pullup or pulldown resistors.

4.3 VS3000 Parameters

VS3000 parameters are used to configure and monitor the chip's functionality during runtime and bring up. Each parameter has a default value and a set of attributes defining the method of updating the parameter. Parameter attributes are explained below.

BU (Bring-up Parameter) Attribute

A parameter with a BU attribute attains its value once only during the boot session. There are two methods for setting BU parameters:

1. By pre-programming the external memory (FLASH) parameter section. This is done using the update parameter tool. The FW loads the parameter values from the external memory parameter section as part of the boot session.
2. By HIF (Host Interface) commands during WaitForHost_n soft strap. This option is described in detail in the document: *Host Interface Reference Guide*.

All BU parameters may be read using GET HIF commands at any time.

RT (Run-time Parameter) Attribute

Parameters with RT attribute (on local or remote devices) may be accessed anytime during runtime using SET and GET HIF commands. These parameters may only be modified using HIF commands.

- RO – read only (can be accessed using HIF GET commands)
- RW – read write (can be accessed using HIF GET and SET commands)
- W – write only (can be accessed using HIF SET commands)

4.3.1 VS3000 Initialization Flow

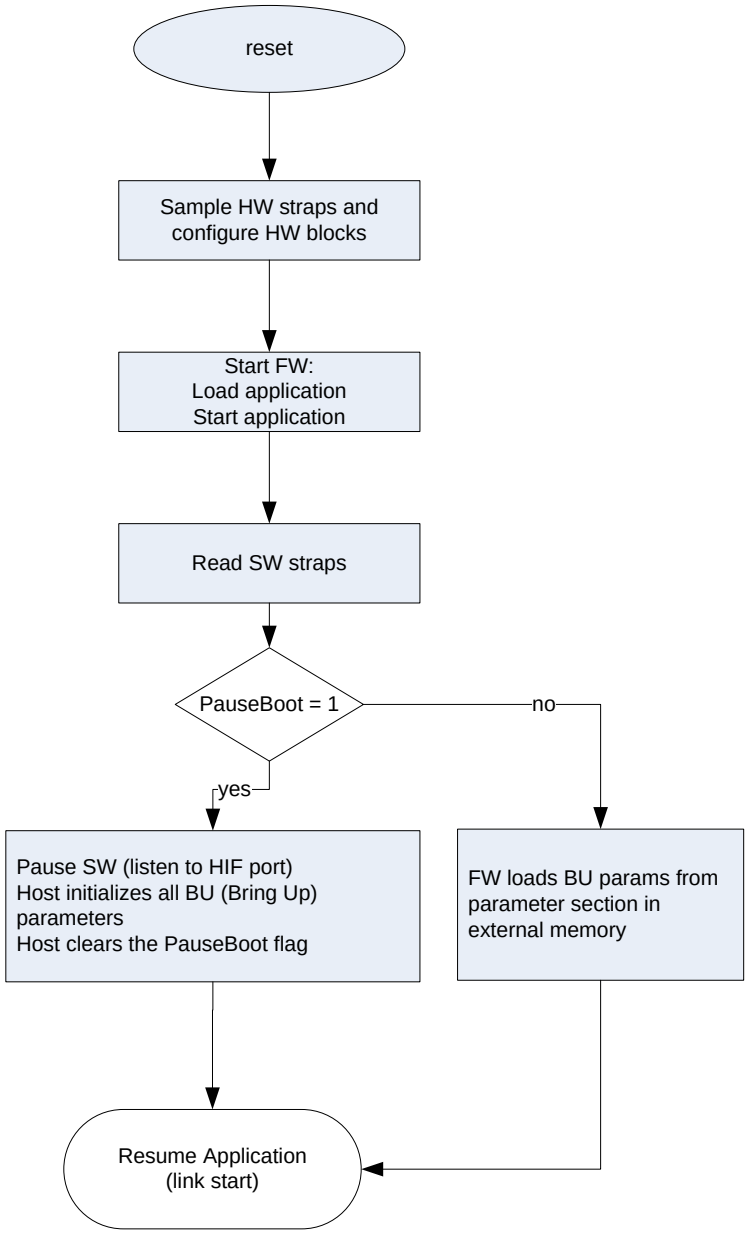


Figure 25: VS3000 Initialization Flow

4.3.2 Parameter List

For a complete guide to configuration of firmware parameters, refer to *Application Note AN3015 – Firmware Parameter Descriptions*.

4.4 GPIO Functionality

VS3000 GPIO pins are used by the FW for various input indications and status outputs. These GPIO functions are pre-assigned and detailed in this section. The following table describes the GPIO pins and functionality.

Table 16: GPIO pins and functionality

Pin Name		GPO Functionality
GPO[0]	Firmware LED	• 0 (Low – LED off): Indicates no FW operation. • 0.5Hz blink (1 second on, 1 second off): Indicates that the Full firmware is loaded and running • 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Indicates that the Internal Boot firmware is running. This should only be used during first-time programming of an empty external Flash memory. • 5Hz blink (0.1 seconds on, 0.1 seconds off): Indicates that the device entered 'Wait state' mode and FW was not uploaded. Usually indicates a failure in the system.
GPO[1]	HDBT Link LED	• 1 (High – LED on): HDBaseT Link. • 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Low Power mode LPPF1/FLPP1. • 0 (low – LED off): No link or PD • ACTIVE: LED ON
GPO[2]	Interrupt to Host CPU	• In normal operation mode - the Interrupt output goes from "0" to "1" upon getting an interrupt event.
GPO[3]	HDMI-Out status LED	• 0 (low – LED off): No HDMI/DVI video • 1 (high – LED on): HDMI/DVI Content exists – with HDCP encryption. • 1.25Hz blink (0.4 seconds on, 0.4 seconds off): HDMI/DVI Content exists – without HDCP encryption
GPO[4]	HDMI-in status LED	• 0 (low – LED off): No HDMI/DVI video • 1 (high – LED on): HDMI/DVI Content exists – with HDCP encryption. • 1.25Hz blink (0.4 seconds on, 0.4 seconds off): HDMI/DVI Content exists – without HDCP encryption
GPO[5]	"Gender" indication LED - indicate if the device is Sink or Source (or undefined)	• 0 (low – LED off): Gender is not defined yet • 1 (high – LED on): Gender is defined as TX (source) • 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Gender is defined as RX (sink)

4.4.1 FW LED (pin GPO[0])

This GPIO function indicates FW operation status as follows:

- 0 (Low – LED off): Indicates no FW operation.
- 0.5Hz blink (1 second on, 1 second off): Indicates that the Full firmware is loaded and running

- 2Hz blink (0.25 seconds on, 0.25 seconds off): Indicates that the Internal Boot firmware is running. This should only be used during first-time programming of an empty external Flash memory.
- 5Hz blink (0.1 seconds on, 0.1 seconds off): Indicates that the device is running from the Basic firmware bank. The Basic firmware does not provide full functionality and running from the Basic bank usually indicates a failure in the system.1 (high – LED off): Indicates no FW operation.

4.4.2 HDBaseT Link LED (pin GPO[1])

This GPIO function reports the link status as follows:

- 0 (low – LED off): No link or in Partner Detect mode of operation.
- 1 (High – LED on): HDBaseT Link in Active mode.
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Low Power mode LPPF1/FLPP1.

4.4.3 Interrupt to Host CPU (pin GPO[2])

This GPIO is used to provide interrupt indication for a Host CPU device. In normal operation mode - the Interrupt output goes from '0' to '1' upon getting an interrupt event.

4.4.3.1 Reduced I2C clock stretching time interrupt (pin GPIO[2])

The following mechanism is supported to reduce the clock stretching time:

- A VCP GET command will be translated to a single I^2C write command.
- **Interrupt signal - GPIO2** is used to indicate to Host when data is ready.
- Upon receiving the Interrupt signal, Host issues a read I^2C command to get the data.
- No additional VCP commands are required between the write and the read.

If a write is followed immediately by a read command – clock stretching *will* take place (same as current behavior).

4.4.3.2 Matrix designs Interrupts (pins GPIO[7], GPIO[64], GPIO[65])

In addition to the existing interrupt signal GPO2 that is defined for general indications, 3 separate interrupt signals are added to support implementation of matrix switch product: GPIO7, GPIO64 and GPIO65.

All 3 interrupt signals are identical with the same indications. Each interrupt signal can be masked separately.

4.4.4 HDMI Out LED (pin GPO[3])

This GPIO function reports the HDMI status as follows:

- 0 (low – LED off): No HDMI/DVI video.
- 1 (high – LED on): HDMI/DVI Content exists – with HDCP encryption.
    - When partner device is backward (Colligo/VS100), LED indicates that there are DDC transactions on HDCP addresses (0x74/0x75).

- 1.25Hz blink (0.4 seconds on, 0.4 seconds off): HDMI/DVI Content exists – without HDCP encryption.

4.4.5 HDMI In LED (pin GPO[4])

This GPIO function reports the HDMI status as follows:

- 0 (low – LED off): No HDMI/DVI video.
- 1 (high – LED on): HDMI/DVI Content exists – with HDCP encryption.
    - When partner device is backward (Colligo/VS100), LED indicates that there are DDC transactions on HDCP addresses (0x74/0x75).
- 1.25Hz blink (0.4 seconds on, 0.4 seconds off): HDMI/DVI Content exists – without HDCP encryption

4.4.6 Device Gender indication LED (pin GPO[5])

This LED provide indication for the selected device “Gender”- indicate if the device is set as Sink (RX) or Source (TX), or undefined.

- 0 (low – LED off): Gender is not defined yet
- 1 (high – LED on): Gender is defined as TX (source)
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Gender is defined as RX (sink)

5 Electrical Specifications

Not Final: The information in this section is preliminary and subject to change.

This chapter contains electrical specifications for the Valens VS3000 chips.

NOTE

The ratings appearing in this section are preliminary and based on tests performed under lab conditions.

5.1 Absolute Maximum Rating

Table 17: VS3000 Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VI	Digital Inputs voltage		0		2.0	V
Tj	Junction Temperature range		0		125	°C
TSTG	Storage Temperature range				150	°C
VDD	0.95V digital core voltage		-0.2		1.055	V
VDDA	0.95V analog voltage		-0.2		1.055	V
HDBT_VDDA	0.98V analog voltage for AFE		-0.2		1.055	V
VDDA_18	1.8V Analog VDD		-0.2		1.98	V
VDDIO18	1.8V Digital IO VDD		-0.2		1.98	V
VDDA_33	3.3V analog voltage		-0.2		3.465	V

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only - functional operation of the device under these or any other conditions above those indicated in the operational section of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Power Supplies

5.2.1 Power Supplies

Table 18: VS3000 Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD	0.95V digital voltage	Typ-5%	0.95	Typ+5%	V
VDDA	0.95V analog voltage	Typ-5%	0.95	Typ+5%	V
HDBT_VDDA	0.98V analog voltage	Typ-3%	0.98	Typ+3%	V
VDDA_18	1.8V analog voltage	Typ-5%	1.8	Typ+5%	V

VDDIO18	1.8 IO voltage	Typ-5%	1.8	Typ+5%	V
VDDA_33	3.3V analog voltage	Typ-5%	3.3	Typ+5%	V
VSS	Ground		0		V

5.3 Power Consumption Ratings

The following are measured Power consumption. For more details on power consumption please contact Customer Support Department.

5.3.1 Tx Power Consumption

Table 19: Tx Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (VDDA_33)	Full Operation: max resolution - 4K, 60hz including HDMI-In & HDMI-out; USB2.0; 1GEthernet(SGMII)	103	mA
IVDDA_18	1.8V Supply Current (VDDA_18)		672	mA
IVDDIO_18	1.8V Supply Current (VDDIO_18)		12	mA
IVDDA	0.95V Supply Current (VDDA)		130	mA
IVDD	0.95V Supply Current (VDD)		1582	mA
VDDA_HDBT	0.98V Supply current		571	mA
PSUPP	**Total Power Consumption**		**3750**	**mW**

Typ: Nominal voltage (0.95, 0.98, 1.8, 3.3V) at Tj = 85°C.

5.3.2 Rx Power Consumption

Table 20: Rx Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (VDDA_33)	Full Operation: max resolution - 4K, 60hz HDMI-In; USB2.0; 1GEthernet(SGMII)	8	mA
IVDDA_18	1.8V Supply Current (VDDA_18)		344	mA
IVDDIO_18	1.8V Supply Current (VDDIO_18)		10	mA
IVDDA	0.95V Supply Current (VDDA)		73	mA
IVDD	0.95V Supply Current (VDD)		2801	mA
VDDA_HDBT	0.98 Supply current		576	mA
PSUPP	**Total Power Consumption**		**3930**	**mW**

Typ: Nominal voltage (0.95, 0.98, 1.8, 3.3V) at Tj = 85°C.

5.4 Reference Clock Requirements

The VS3000 IC Clock input can be sourced by a 25MHz oscillator connecting it to the XTAL_IN pad or by connecting a 25MHz low cost crystal IC to the XTAL_IN/OUT pads.

5.4.1 CMOS Oscillator Requirements

The CMOS oscillator should comply with the following requirements:

- Frequency: 25 MHz
- Accuracy: ±100 ppm (±0.01%)

- Drive Level: 100uW
- Phase Noise must be kept below the phase noise mask specified in Table 21 below.

Table 21: CMOS Oscillator Phase Noise Mask

Frequency	Phase Noise (dBc/Hz)
1 Hz	-30
10 Hz	-60
100 Hz	-90
1 KHz	-127
10 KHz	-148
100 KHz	-150
10 GHz	-150

5.4.2 Crystal Requirements

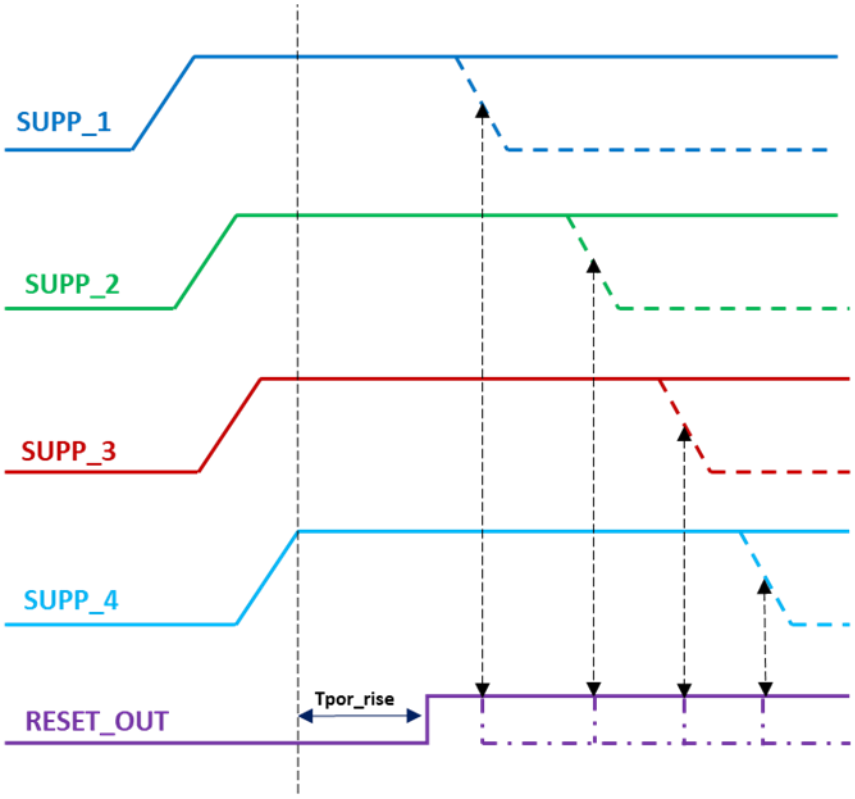
The Crystal Clock should comply with the following specification for *HDBT_XTAL_IN* clock input of the VS3000 chip:

Table 22: VS3000 Crystal Requirements

Parameter	System Crystal Value
Nominal Frequency	25MHz
Frequency Tolerance @ 25oC	±100 PPM
Drive Level	100 uW
Max. ESR	100 ohm

5.4.2.1 Power on Reset Signal Timing

Option 1: Using Internal POR (RESET_SEL = 0 'b0. Pin RESET_OUT is the system reset)



1. The SUPP_x – represents one of the voltages supplied without the importance of order between them. SUPP_x represents the VS3000 power supplies.
2. RESET_OUT = SUPP_1 & SUPP_2 & SUPP_3 & SUPP_4
3. Tpor_rise is the delay from point where all supplies are stable to RESET_OUT

Figure 26: Internal Power on Reset Timing

Table 23: Internal Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tpor_rise	Reset pulse width on RESET_OUT				170	mS

Option 2: Using External POR (RESET_SEL = 1'b1. Pin RESET_IN is the system reset)

The RESET_IN signal must be held active at least 1ms after all chip supply voltages (VDD, VDDA, VDDIO18, VDDA_18 and VDDA_33).

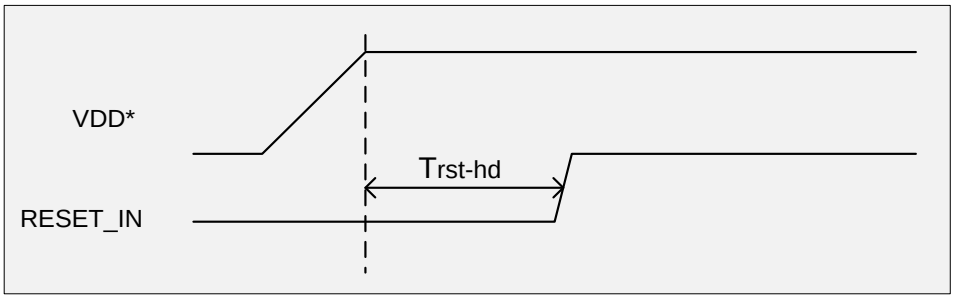


Figure 27: Reset Signal Timing

Table 24: External Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Trst_hd	Reset pulse width on RESET_IN after all 4 supplies are stable		1			mS

5.5 Recommended Operating Conditions

5.5.1 Electrical Characteristics (DC Specifications)

Table 25: VS3000 Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
Digital pads							
VIH	Input voltage high	Digital pads	1.17		1.98	V	
VIL	Input voltage low		-0.3		0.63	V	
CIN	Input capacitance				2	pF	
RPU	Pull-up resistor		54	80	120	KΩ	
RPD	Pull-down resistor		55	95	176	KΩ	
VOH	Output voltage High		1.35			V	
VOL	Output voltage Low				0.45	V	
IOH	High level Output current @VOH (min)		4.9		78.6	mA	Depends upon drive strength configuration
IOL	Low level Output current @VOL (max)		7.4		66.6	mA	Depends upon drive strength configuration
DHDI interface - DC specification							

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
Vo_se	Single ended Voltage range that can be observed on DHDI IOs.		0		0.99	V	
Vcmout	Output Common mode range		0.35	0.4	0.45	V	
Vod	Output differential voltage peak		0.25	0.3	0.35	V	
Vodo	Output differential voltage peak in overdrive mode	Txodrv=1'b1	0.3	0.36	0.42	V	
Vi_se	Single ended Voltage range that can be tolerable on DHDI IO without damage induced to DUT nor open any clamping device.		0		1.98	V	
Vid	Differential input voltage range that should be supported by DHDI receiver Over all common mode range defined as Vcmin below.		0.1		0.6	V	
RIN(DIFF)	Receiver differential input impedance		90	100	110	Ω	
CIN	Single ended Input capacitance of receiver on each DHDI pin				1.5	pF	
SGMII interface							
Vo_se	Single ended Voltage range that can be observed on LVDS IOs.		0		1.98	V	
Vcmout_lvds	Output Common mode range (LVDS mode)		1.13	1.2	1.38	V	
Vod_lvds	Output differential voltage peak, VCM = 1.2V	Standard LVDS levels	0.25	0.33	0.4	V	
Vcmout_sub_lvds	Output Common mode range (sub LVDS mode)		0.8	0.9	1	V	
Vod_sub_lvds	Output differential voltage peak, VCM = 0.9V		0.125	0.165	0.2	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
Vi_se	Single ended Voltage range that can be tolerable on SGMII IO without damage induced to DUT nor open any clamping device.		0		1.98	V	
Vid	Differential input voltage range that should be supported by LVDS receiver over all common mode range defined as Vcmin below		0.1		0.5	V	
Vcmin	Input Common mode range		0.2	1.2	(VDDIO_18 - 0.2)	V	
RIN(Diff)	Receiver differential input impedance		90	100	110	Ω	
CIN	Single ended Input capacitance of receiver on each line				1.5	pF	
TMDS Receivers DC specification							
VTH	Differential Input Threshold (+)				+75	mV	
VTL	Differential Input Threshold (-)		-75			mV	
IVID	Differential Input Voltage (pk-pk)	For details about these parameters, refer to the HDMI 2.0 specification .	150		1560	mV	
VINSE	Input voltage referred to ground		2.4		3.3	V	
Vcm	Input common mode offset		IVID / 2		3.3 – IVID / 2	V	
Vcmdif	Input common mode offset difference		-	100	-	mV	
RIN(SE)	Single ended input impedance		45	50	55	Ω	
TMDS Drivers DC specification							
VSWING	Single-ended output swing voltage RT = 50 Ω	If the attached Sink supports only < 340 MHz	400		600	mV	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
VSWING_DATA	Compliance point TP1 is as defined in the HDMI specification, version 1.3a, section 4.2.4.	If the attached Sink supports only ≥ 340 MHz and transmitted TMDS Character Rate ≥ 340MHz.	400		600		
VSWING_CLOCK			200		600		
VH	Single-ended output high voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ – 10mV	HD_AVDD_33	Typ + 10mV	V	
		if attached Sink supports TMDSCLK > 165Mhz	Typ - 200mV	HD_AVDD_33	Typ + 10mV	V	
VH_DATA		If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	Typ - 400mV	HD_AVDD_33	Typ + 10mV	V	
VH_CLOCK			Typ - 400mV	HD_AVDD_33	Typ + 10mV	V	
VL	Single-ended output low voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ - 600mV	HD_AVDD_33	Typ - 400mV	V	
		if attached Sink supports TMDSCLK > 165Mhz	Typ - 700mV	HD_AVDD_33	Typ - 400mV	V	
VL_DATA			Typ - 1000mV	HD_AVDD_33	Typ - 400mV	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
VL_CLOCK		If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	Typ - 1000mV	HD_AVDD_33	Typ - 200mV	V	
RTERM	Differential source termination load (inside HDMI Tx PHY) Although the HDMI Tx PHY includes differential source termination, the user-defined value is set for each single line. **Note**: RTERM can also be configured to be open and not present on TMDS channels.		50	-	200	Ω	
Hot plug detect specifications (HDMI_TX_HPD)							
HPD_{VH}	Hot plug detect high range		2.0	-	5.3	V	
HPD_{VL}	Hot plug detect low range		0	-	0.8	V	
HPD_{Z}	Hot plug detect input impedance		10	-	-	kΩ	
HPD_{t}	Hot plug detect time delay		-	-	100	µs	

5.5.2 Timing (AC specifications)

5.5.2.1 RMII

Table 26: RMII AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RMII						
Tr_cyc	RMII CLK IN period			20		ns
Tr_cq	Clock-to-Q from rising edge of CLKIN to: • RMII_RXD[1:0] RMII_CRS_DV RMII_RX_ER		2		13.5	ns

Tr-su	Data setup to rising edge of CLKIN RMII_TXD[1:0] RMII_TX_EN		4			ns
Tr-h	Data HOLD from rising edge of CLKIN RMII_TXD[1:0] RMII_TX_EN		2			ns

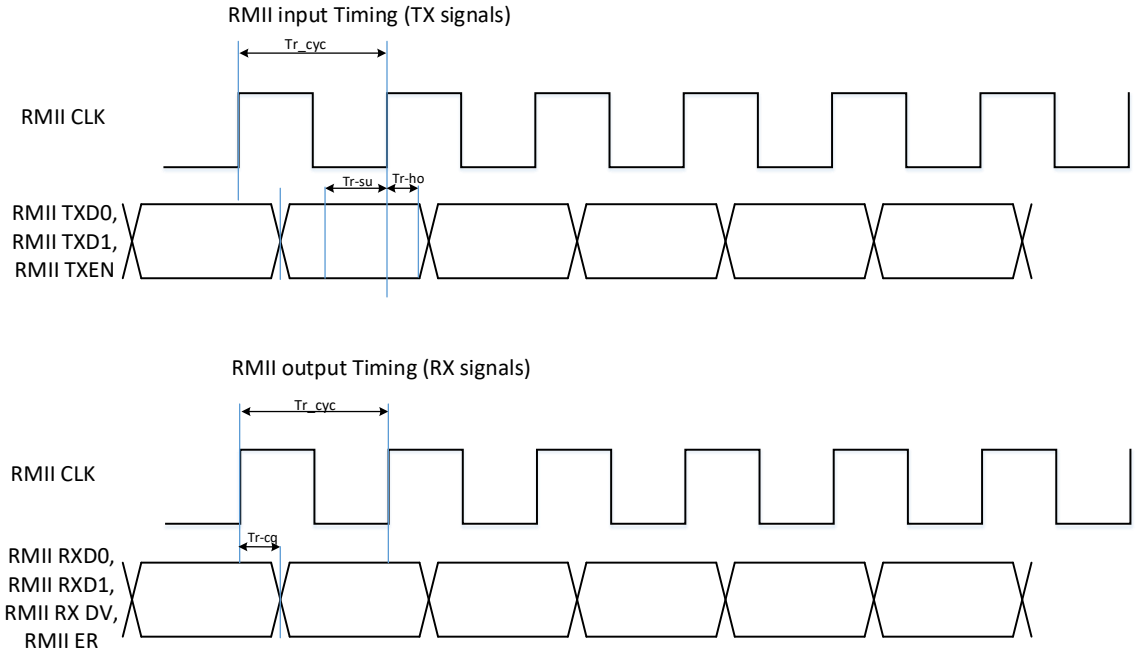


Figure 28: RMII Timing Diagram

5.5.2.2 SGMII

Table 27: SGMII AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Data rate	Data rate	SGMII Standard +/-150ppm		1250		Mbps
Tintra_skew_tx	Output intra pair skew		-10		+10	ps
Tintra_skew_rx	input intra pair skew tolerance		-25		+25	ps

5.5.2.3 MDC/MDIO

Table 28: MDC/MDIO AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tcyc	CLK Cycle		400			ns

Clk D.C	Duty Cycle		40	50	60	%
Tih	mdio input hold		10			ns
Tis	mdio input setup		10			ns
To-cq	clock to out		0		300	ns

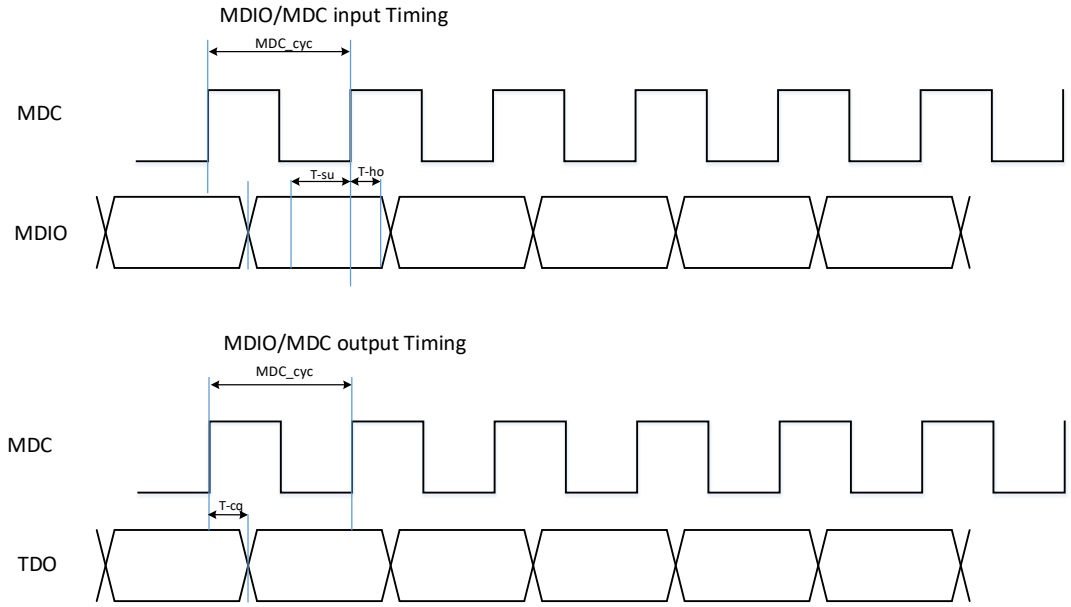


Figure 29: MDIO/MDC Timing Diagram

5.5.2.4 QSPI

Table 29: QSPI AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tspi_cyc	QSPI CCLK period		25			ns
Tspi_dc	QSPI CCLK Duty Cycle		40	50	60	%
Tspi_ho	D[3:0], CS Hold to rising edge of CCLK		2			ns
Tspi_su	D[3:0] Data setup to rising edge of CLK		2			ns
Tspi_ovn	D[3:0], CS Output not Valid from falling edge of CLK		-4		4	ns
Timing was designed for system load up to 30pF.						

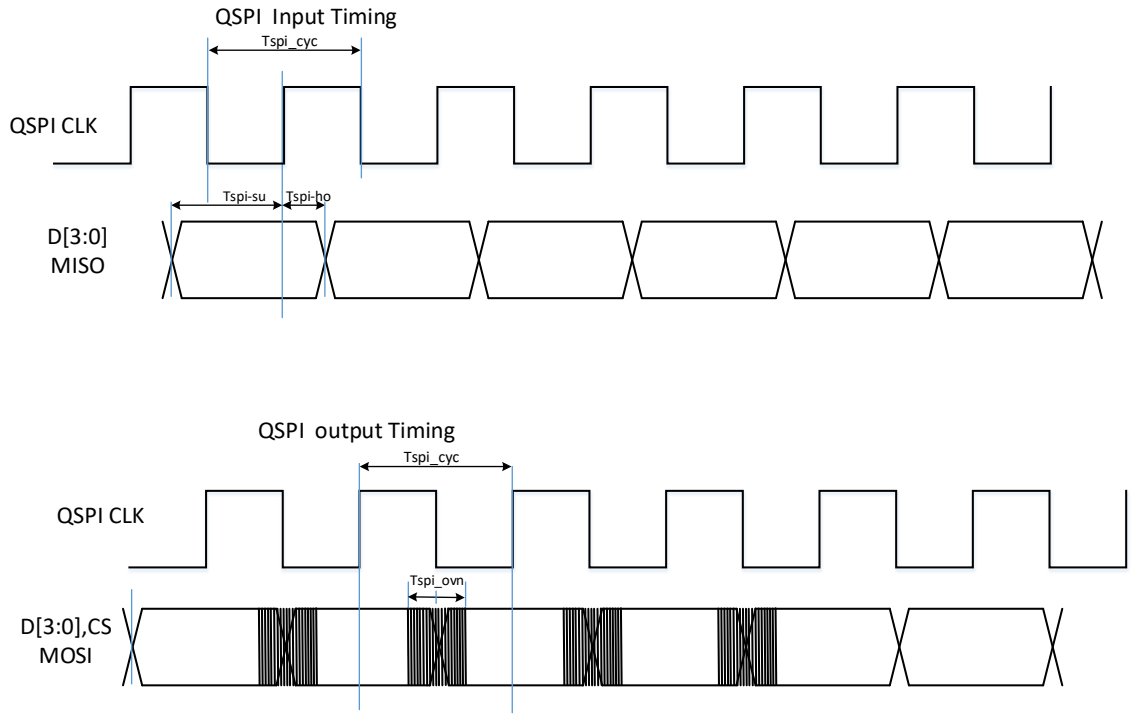


Figure 30: QSPI Timing Diagram

5.5.2.5 I²C

Table 30: I²C AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Standard Mode						
fSCL	SCL clock frequency		0		100	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0			us
tLOW	LOW period of the SCL clock		4.7			us
tHIGH	HIGH period of the SCL clock		4.0			us
tSU;STA	Set-up time for a repeated START condition		4.7			us
tHD;DAT	Data hold time		0		-	us

tSU;DAT	Data set-up time		250			ns
tr	Rise time of both SDA and SCL signals				1000	ns
tf	Fall time of both SDA and SCL signals				300	ns
tSU;STO	Set-up time for STOP condition		4.0			us
tBUF	Bus free time between a STOP and START condition		4.7			us
Cb	Capacitive load for each bus line				400	pF
Fast Mode						
fSCL	SCL clock frequency		0		400	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			us
tLOW	LOW period of the SCL clock		1.3			us
tHIGH	HIGH period of the SCL clock		0.6			us
tSU;STA	Set-up time for a repeated START condition		0.6			us
tHD;DAT	Data hold time		0		-	us
tSU;DAT	Data set-up time		100(1)			ns
tr	Rise time of both SDA and SCL signals		20		300	ns
tf	Fall time of both SDA and SCL signals		20x (VDD/5.5V)		300	ns
tSU;STO	Set-up time for STOP condition		0.6			us
tBUF	Bus free time between a STOP and START condition		1.3			us
Cb	Capacitive load for each bus line				400	pF
Fast Mode Plus						
fSCL	SCL clock frequency				800	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.26			us
tLOW	LOW period of the SCL clock		0.5			us

tHIGH	HIGH period of the SCL clock		0.26			us
tSU;STA	Set-up time for a repeated START condition		0.26			us
tHD;DAT	Data hold time		0		-	us
tSU;DAT	Data set-up time		50			ns
tr	Rise time of both SDA and SCL signals				120	ns
tf	Fall time of both SDA and SCL signals		20x (VDD/5.5V)(2)		120(3)	ns
tSU;STO	Set-up time for STOP condition		0.26			us
tBUF	Bus free time between a STOP and START condition		0.5			us
Cb	Capacitive load for each bus line				550	pF

(1) A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr(max) + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

(2) Must be backwards compatible with Fast-mode.

(3) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

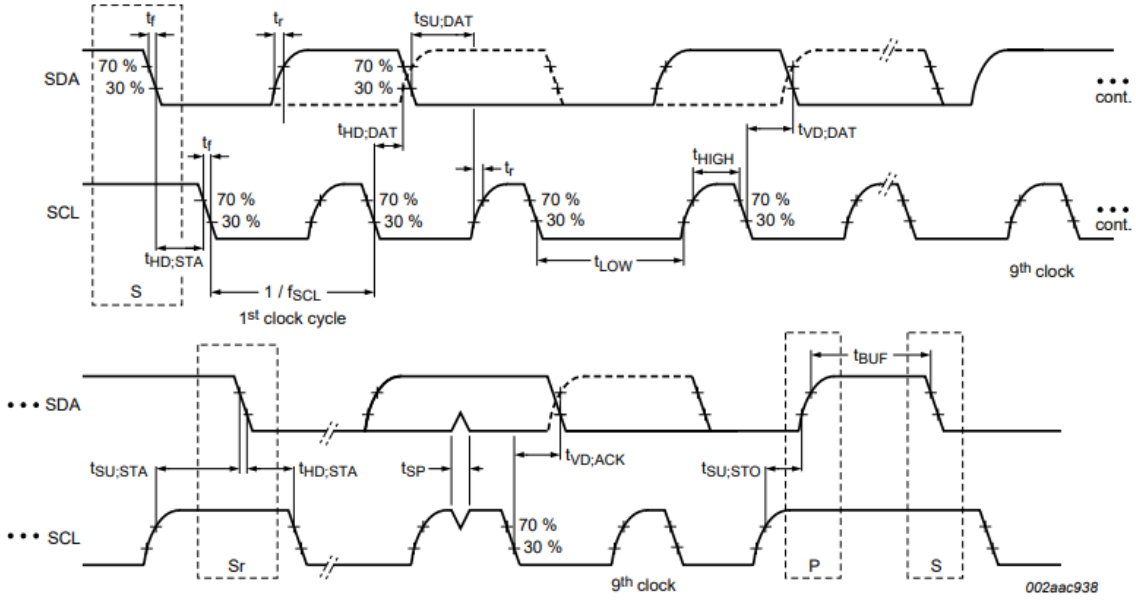


Figure 31: I²C Timing Diagram

5.5.2.6 UART

Table 31: UART AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UART_DBG	Debug UART frequency				115200	KHz
RIF_UART	Host UART frequency				2	MHz
UART_TA	UART T/A frequency				2	MHz

5.5.2.7 JTAG

Table 32: JTAG AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tcyc	CLK cycles		100			ns
CLK D.C.	Clock Duty cycle		40	50	60	%
Ttdo_cq	clock-to-Q from falling edge of TCK		0		13.5	ns
Ttms/tdi-su	Data setup to rising edge of TCK		8			ns
Ttms/tdi-ho	Data HOLD from rising edge of TCK		5			ns

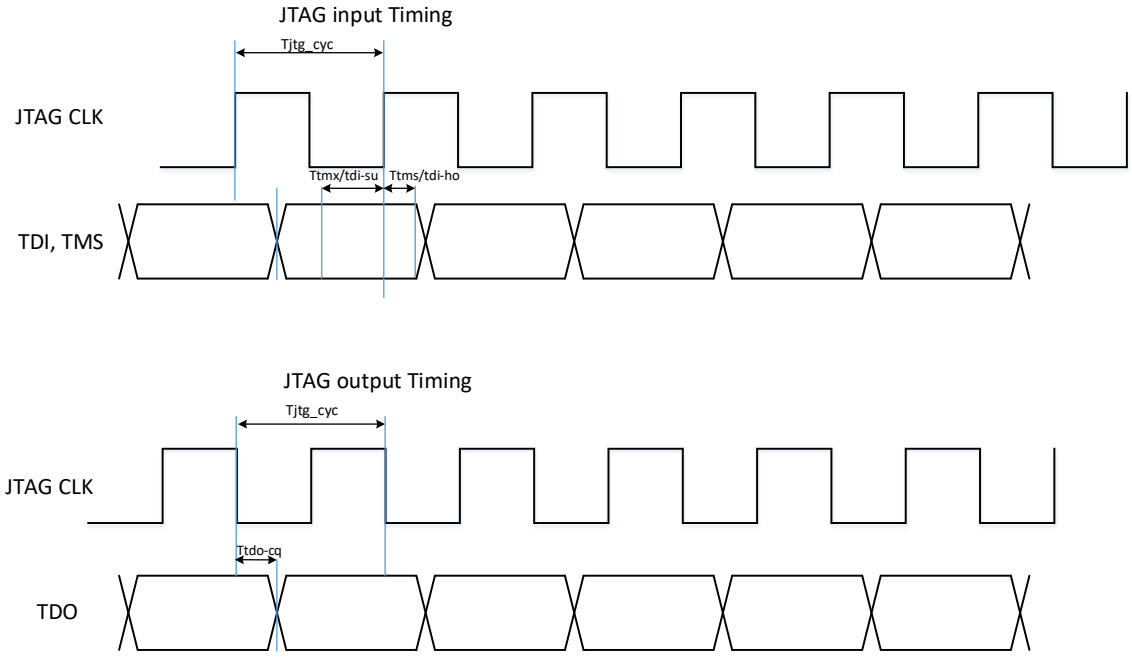


Figure 32: JTAG Timing Diagram

5.5.2.8 I²S

Table 33: I²S AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ti2s_cyc	CLK IN period		40			ns
CLK D.C	CLK IN Duty Cycle		45		55	%
Ti2s_cq	clock-to-Q from falling edge of CLK		0		12	ns
Ti2s-su	Data setup to rising edge of CLK		5			ns
Ti2s-h	Data HOLD from rising edge of CLK		5			ns

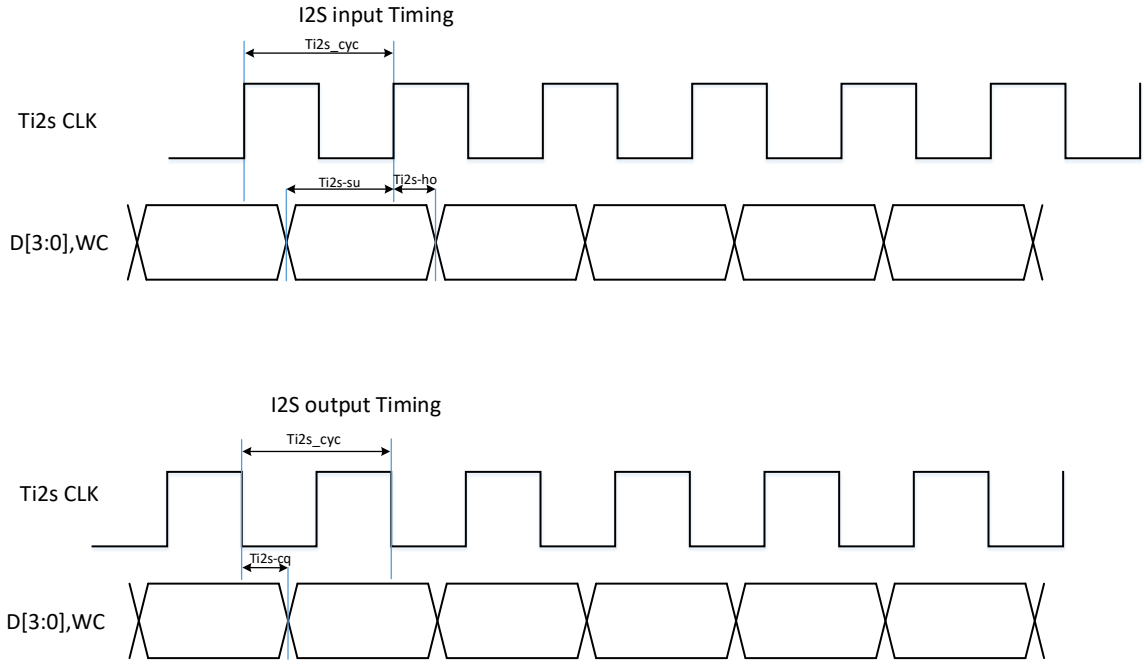


Figure 33: I²S Timing Diagram

5.5.2.9 DHDI (DHDI Mode)

Table 34: DHDI AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FCLK	Clock lane frequency			250		MHz
Data rate	Data rate	Data lane		2500		Mbps
Tintra_skew_tx	Output intra pair skew		-15		+15	ps
Tinter_skew_tx	Output inter pair skew between every two pairs		-50		+50	ps
Tintra_skew_rx	input intra pair skew tolerance		-25		+25	Ps
Tinter_skew_rx	input inter pair skew tolerance between every two pairs		-100		+100	ps

5.5.2.10 TMDS

Table 35: TMDS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Data rate	Maximum serial data rate				6	Gbps
FTMDSCLK	TMDSCLK frequency	On TMDSCLKP/N outputs If the attached Sink supports < 340MHz	25		340	MHz
		On TMDSCLKP/N outputs If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	85		150	MHz
PTMDSCLK	TMDSCLK period	RL=50Ω ±10% If the attached Sink supports < 340MHz	2.97		40	ns
		RL=50Ω ±10% If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	6.66		11.76	ns
tCDC	TMDSCLK duty cycle	tCDC = tCPH / PTMDSCLK RL=50Ω ±10%	40	50	60	%
tCPH	TMDSCLK high time	RL=50Ω ±10%	4	5	6	UI
tCPL	TMDSCLK low time	RL=50Ω ±10%	4	5	6	UI
	TMDSCLK jitter 1	RL=50Ω ±10%			0.25	UI
tSK(P)	Intra-Pair (Pulse) skew. (between a pair lanes)	RL=50Ω ±10%			0.15	UI
tSK(PP)	Inter-Pair (Pulse) skew (between different pairs).	RL=50Ω ±10%			1	UI
tr	Differential output signal rise time	20% to 80%, RL = 50 Ω ±10% If the attached Sink supports < 340MHz	75			ps

tr_data		20% to 80%, RL = 50Ω ±10% If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	42.5			ps
tr_clock		20% to 80%, RL = 50 Ω ±10% If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	75			ps
tf	Differential output signal fall time	20% to 80%, RL = 50 Ω ±10% If the attached Sink supports < 340MHz	75			ps
tf_data		20% to 80%, RL = 50 Ω ±10% If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	42.5			Ps
tf_clock		20% to 80%, RL = 50 Ω ±10%If the attached Sink supports only ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz	75			ps
TMDS Receivers specification						
Data rate	Maximum serial data rate				3.4	Gbps
FPCLK	TMDS Input clock frequency	On HDMI_RX_TMDSCLKP/N	25		340	MHz
Intra-pair skew tolerance		FPCLK ≤ 225MHz			0.4	UI
		FPCLK > 225MHz			0.15UI + 112ps	mixed
Inter per skew					2UI + 1.78ns	mixed

	Input Clock Jitter Tolerance	Relative to Ideal Recovered Clock as defined in HDMI 2.0 specification			0.30	UI

5.6 ESD Ratings

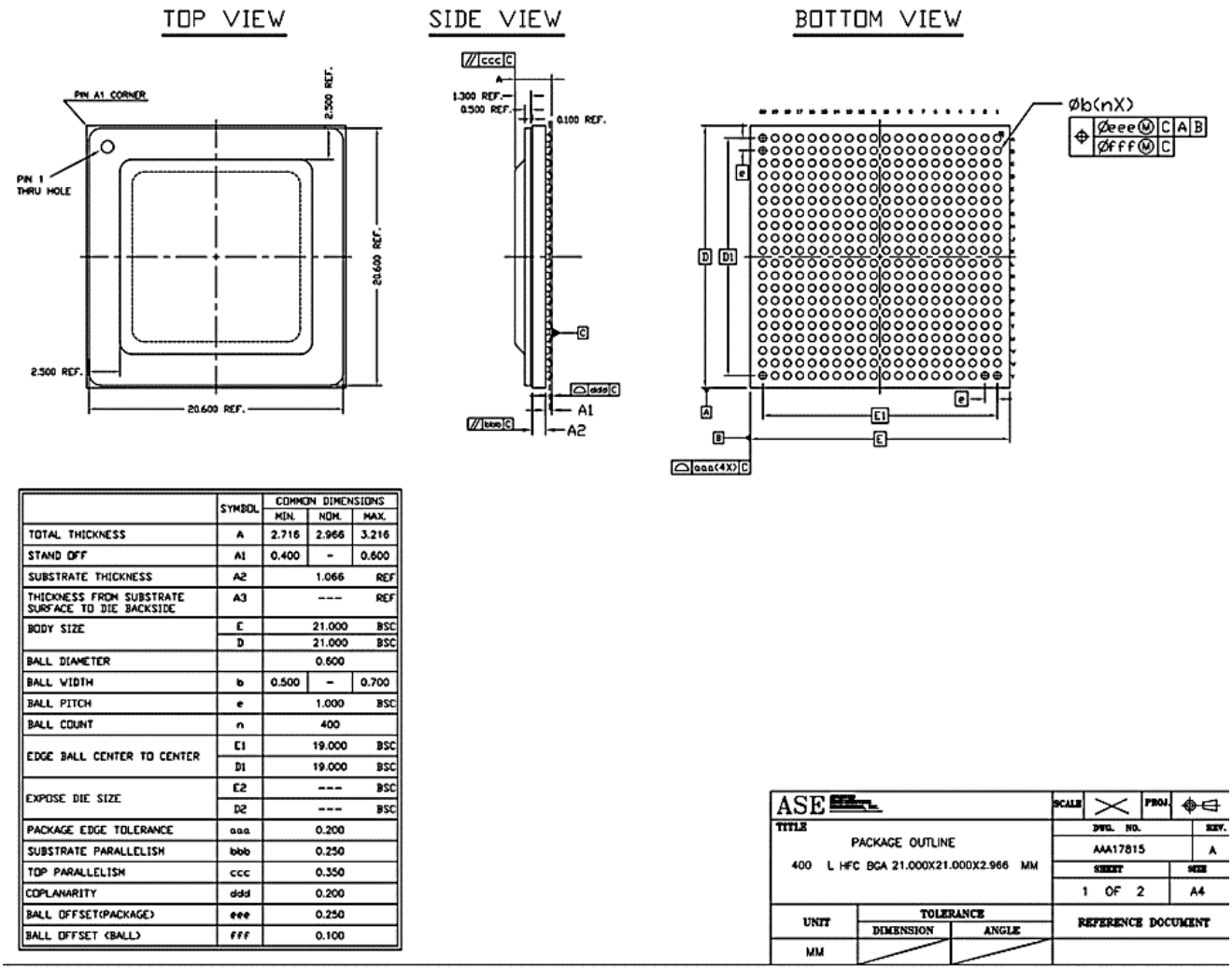
Not Final: The information in this section is preliminary and subject to change.

Table 36: ESD Ratings

Test	Value	Unit
HBM (per JEDEC JS-001)	± 2000	V
CDM (per JEDEC JESD22-C101)	± 500	
Latch Up (per JEDEC JESD78)	± 100	mA
	Over-voltage: 1.5x supply at 85°C	

6 Package Mechanical Data

6.1 VS3000 Package Mechanical Data



	SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
TOTAL THICKNESS	A	2.716	2.966	3.216
STAND OFF	A1	0.400	-	0.600
SUBSTRATE THICKNESS	A2		1.066	REF
THICKNESS FROM SUBSTRATE SURFACE TO DIE BACKSIDE	A3		---	REF
BODY SIZE	E		21.000	BSC
	D		21.000	BSC
BALL DIAMETER			0.600	
BALL WIDTH	b	0.500	-	0.700
BALL PITCH	e		1.000	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	E1		19.000	BSC
	D1		19.000	BSC
EXPOSE DIE SIZE	E2		---	BSC
	D2		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.200	
SUBSTRATE PARALLELISH	bbb		0.250	
TOP PARALLELISM	ccc		0.350	
COPLANARITY	ddd		0.200	
BALL OFFSET(PACKAGE)	eee		0.250	
BALL OFFSET (BALL)	fff		0.100	

ASE	SCALE: X	PROJ.	
TITLE: PACKAGE OUTLINE 400 L HFC BGA 21.000X21.000X2.966 MM	DWG. NO.: AAA17815	REV.: A	
	SHEET: 1 OF 2	SIZE: A4	
UNIT: MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	

Figure 34: VS3000 Mechanical Information (all dimensions in mm)

6.2 VS3000 Marking Information

Not Final: The information in this section is preliminary and subject to change.

For the VS3000 markings depicted below, the following information applies:

Table 37: VS3000 Marking schema per example

Row	Step	Description	Definition
1	1	Logo	Valens
2	1	Product P/N	VS3xxxxxx
3	1	LOT number	V2xxxxxxx
4	1	Bar code	
4	2	Assembly year and week	YYWW
5	1	Assembly site code Country Of Origin per assembly location	ATWN

Figure 35: VS3000 Marking

6.3 Ordering Codes

Table 38: Ordering Codes

Ordering Code	Item Description
VS3000A0SESB	Valens HDBaseT VS3000 Transmitter/Receiver (engineering samples)
VS3000A0S	Valens HDBaseT VS3000 Transmitter/Receiver

7 Thermal Parameters

7.1 Terminology

- θ_{JA} - Junction-to-ambient thermal resistance (EIA/JESD51-2 and EIA/JESD51-6):

  $\theta_{JA} = (T_J - T_A) / P_H$
  where T_J = junction temperature
  T_A = ambient temperature
  P_H = power dissipation

  θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} means better overall thermal performance.

- Ψ_{JT} - Junction-to-top-center thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6):

  $\Psi_{JT} = (T_J - T_T) / P_H$
  Where T_T = temperature at the top-center of the package

  Ψ_{JT} is used for estimating the junction temperature by measuring T_T in an actual environment.

- θ_{JB} - Junction-to-board thermal resistance (EIA/JESD51-8):

  $\theta_{JB} = (T_J - T_B) / P_H$
  Where T_B = board temperature with ring cold plate fixture applied

  θ_{JB} represents the resistance to the heat flows from the chip to PCB. θ_{JB} is used in compact thermal models for system-level thermal simulation.

- θ_{JC} - Junction-to-case thermal resistance:

  $\theta_{JC} = (T_J - T_C) / P_H$
  Where T_C = case temperature attached with a cold plate

  θ_{JC} represents the resistance to the heat flows from the chip to package top case. θ_{JC} is important when external heat sink is attached on package top.

7.2 Simulation Conditions

Ambient temperature: 85^{o} C

Power Consumption: 9 W

Air flow

7.3 Results Summary

Table 39: Thermal Data

V AIR (m/s)	θJA (°C/W)	ΨJT (°C/W)	θJC (°C/W)	θJB (°C/W)
0	11.41	0.51	0.64	3.78
1	9.77	0.51		
2	8.98	0.5		
3	8.56	0.5		

Table 40: PCB Constructions

Construction	Dimensions
PCB type	2s2p
PCB Layers	4-layer
PCB dimensions	101.5 x 114.3 x 1.6 mm
Core thickness	0.60 mm
Power and ground layer thickness	0.375 mm
Top and bottom trace thickness	0.07 mm
Solder mask thickness	0.02 mm
Thermal Via Diameter	0.30 mm
Thermal Via plating thickness	0.018 mm
Thermal Via Pitch	1.0 mm
Number of Vias	48
L1 Top / L4 Bottom coverage (%)	20
L2/L3 Inner copper coverage (%)	90

8 Quality and Environmental Policy

Committed to Quality

Valens is 100% engaged in a culture of continuous improvement, while cultivating constructive partnerships with suppliers, customers and stakeholders.

The Valens Quality Management System is certified and regularly audited according to ISO 9001 requirements.

Committed to the Environment

Valens consistently monitors and strives to minimize the environmental impact of our activities by implementing sustainable business practices across our operations, infrastructure and products, while complying with all laws, regulations, and applicable environmental, health and safety requirements.

Valens products are designed to comply with up to date Restrictions of Hazardous Substances (ROHS) and to limit the impact of Substances of Very High Concern (SVHC) under REACH regulation. Valens has established a Conflict Minerals Sourcing Policy and EICC-based Code of Conduct, and encourages suppliers to establish green, eco-friendly supply chain management processes.

The Valens Environmental Management System is certified and regularly audited, according to ISO 14001 requirements.

ISO 9001

ISO 14001

RoHS – Restriction of Hazardous Substances

REACH SVHC – Substances of Very High Concern

Conflict Minerals Sourcing Policy

For further information, please refer to the Valens Quality and Environmental Policy detailed on our web page: http://valens.com/about/quality

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