Serially Interfaced, 8-Digit LED Display Drivers

FEATURES

- 10MHz Serial Interface
- Individual LED Segment Control
- Decode/No-Decode Digit Selection
- 150µA Low-Power Shutdown (Data Retained)
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Display

APPLICATIONS

- Bar-Graph Displays
- 7-Segment Displays
- Industrial Controllers
- Panel Meters
- LED Matrix Displays

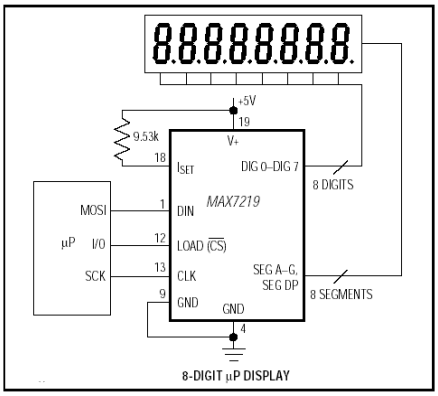
GENERAL DESCRIPTION

The MAX7219 are compact, serial input/output common-cathode display drivers that interface microprocessors (µPs) to 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. Only one external resistor is required to set the segment current for all LEDs.

A convenient 3-wire serial interface connects to all common µPs. Individual digits may be addressed and updated without rewriting the entire display. The MAX7219 also allow the user to select code-B decoding or no-decode for each digit.

The devices include a 150µA low-power shutdown mode, analog and digital brightness control, a scan-limit register that allows the user to display from 1 to 8 digits, and a test mode that forces all LEDs on.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)	Operating Temperature Ranges
V+ .....-0.3V to 6V	MAX7219C .....0°C to +70°C
DIN, CLK, LOAD.....-0.3V to 6V	MAX7219E .....-40°C to +85°C
All Other Pins.....-0.3V to (V+ + 0.3V)	Storage Range .....-65°C to +160°C
Current	Lead Temperature (soldering, 10sec) .....+300°C
DIG0–DIG7 Sink Current.....500mA	
SEGA–G, DP Source Current.....100mA	
Continuous Power Dissipation (TA = +85°C)	
Narrow Plastic DIP 0.87W	
Wide SO 0.76W	
Narrow CERDIP.....1.1W	

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V+ = 5V ±10%, R_{SET} = 9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

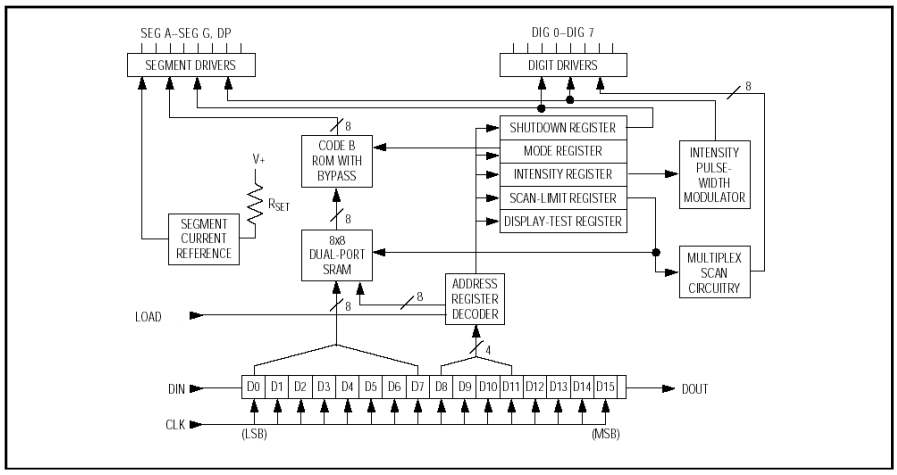
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V+		4.0		5.5	V
Shutdown Supply Current	I+	All digital inputs at V+ or GND, T_A = +25°C			150	µA
Operating Supply Current	I+	R_{SET} = open circuit			8	mA
		All segments and decimal point on, $I_{SEG\_}$ = -40mA		330		
Display Scan Rate	f_{OSC}	8 digits scanned	500	800	1300	Hz
Digit Drive Sink Current	I_{DIGIT}	V+ = 5V, V_{OUT} = 0.65V	200			mA
Segment Drive Source Current	I_{SEG}	T_A = +25°C, V+ = 5V, V_{OUT} = (V+ - 1V)	-26	-35	-45	mA
Segment Drive Current Matching	ΔI_{SEG}			3.0		%
Digit Drive Source Current	I_{DIGIT}	Digit off, V_{DIGIT} = (V+ - 0.3V)	-2			mA
Segment Drive Sink Current	I_{SEG}	Segment off, V_{SEG} = 0.3V	5			mA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V ±10%, R_{SET} =9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOGIC INPUTS						
Input Current DIN, CLK, LOAD	I_{IH}, I_{IL}	V_{IN} = 0V or V+	-1		1	μA
Logic High Input Voltage	V_{IN}		3.5			V
Logic Low Input Voltage	V_{IL}				0.8	V
Output High Voltage	V_{ON}	DOUT, I_{SOURCE} = -1mA	V+-1			V
Output Low Voltage	V_{OL}	DOUT, I_{SINK} = 1.6mA			0.4	V
Hysteresis Voltage	ΔV_I	DIN, CLK, LOAD		1		V
TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
CLK Rise to LOAD Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF			25	ns
Load-Rising Edge to Next Clock	t_{LDCK}		50			ns
Minimum LOAD Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

FUNCTIONAL DIAGRAM



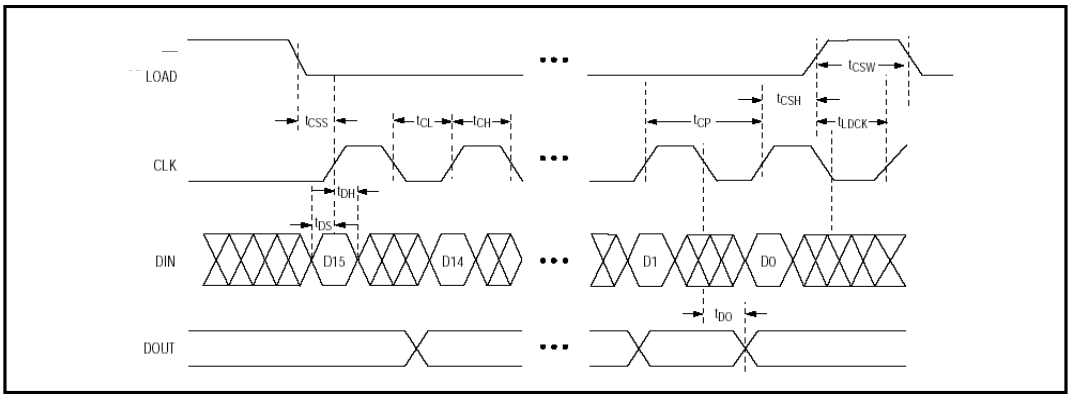
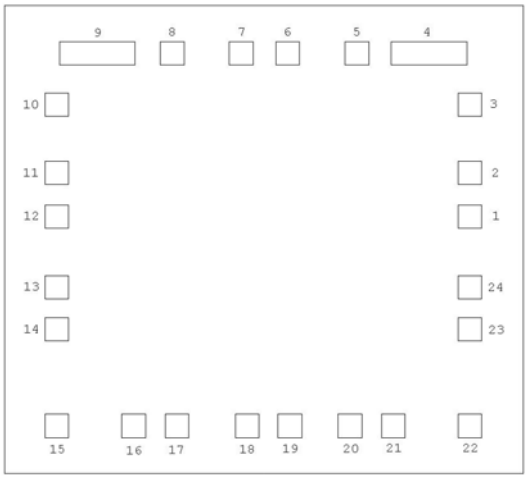


Figure 1. Timing Diagram

TABLE 1. SERIAL-DATA FORMAT (16 BITS)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB			DATA				LSB

PAD LOCATION AND COORDINATES

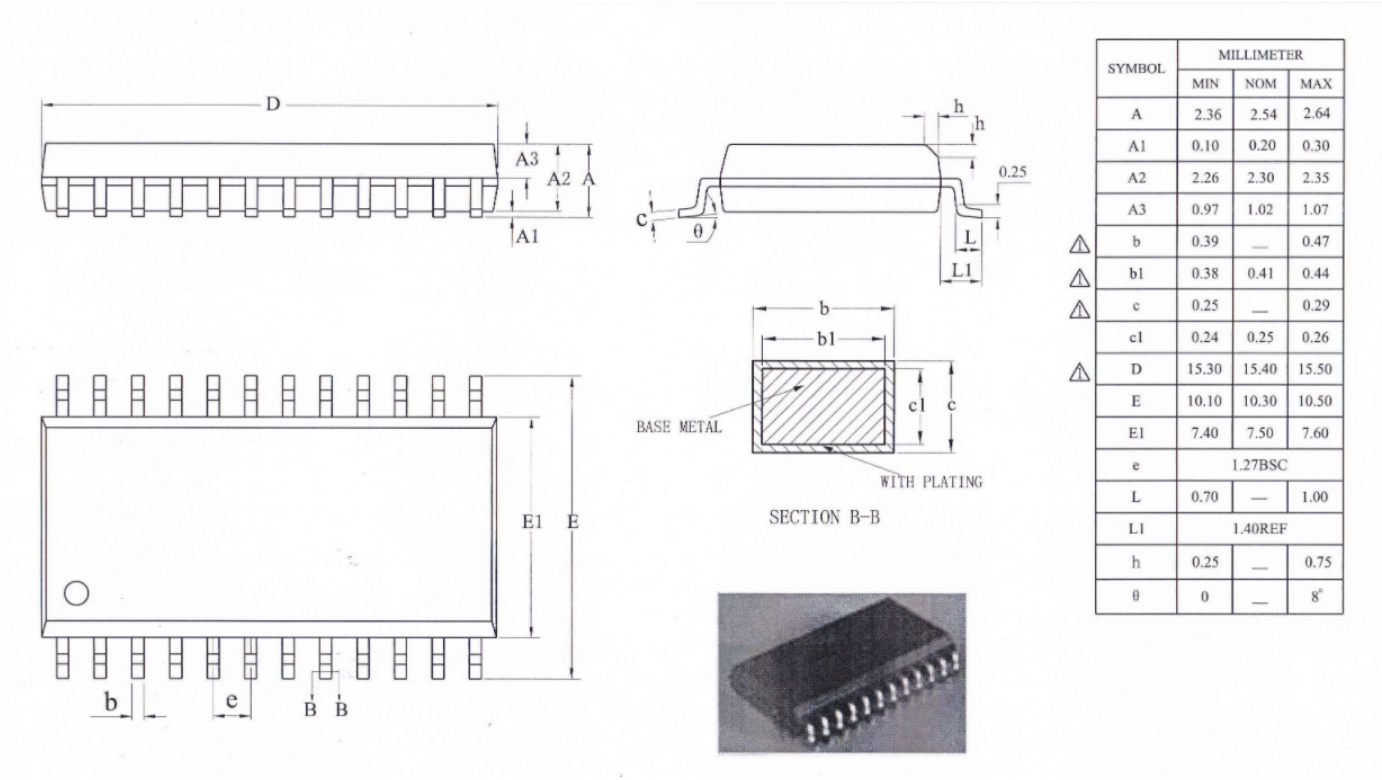


Chip Size: 2.0 x 2.2 mm^2

PIN DESCRIPTION

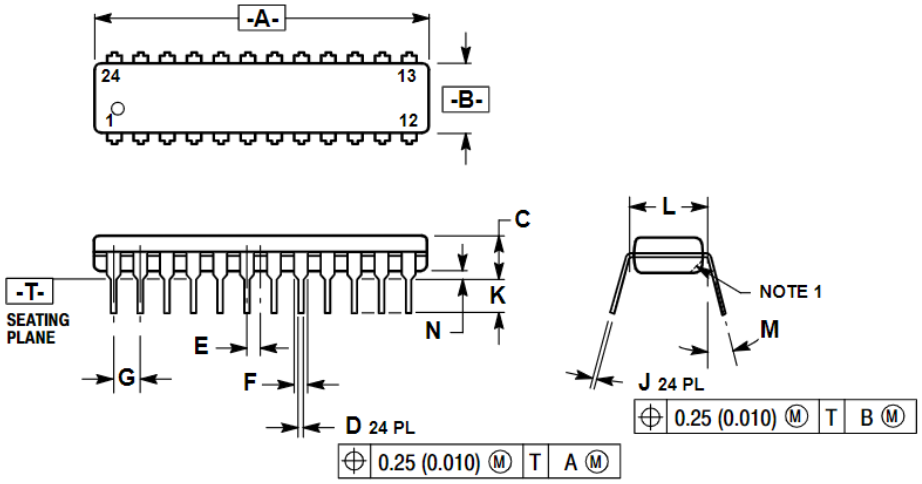
PIN	NAME	FUNCTION
1	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
2, 3, 5-8, 10, 11	DIG 0–DIG 7	Eight-Digit Drive Lines that sink current from the display common cathode. The MAX7219 pulls the digit outputs to V+ when turned off.
4, 9	GND	Ground (both GND pins must be connected)
12	LOAD	Load-Data Input. The last 16 bits of serial data are latched on LOAD's rising edge.
13	CLK	Serial-Clock Input. 10MHz maximum rate. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT.
14-17, 20-23	SEG A–SEG G, DP	Seven Segment Drives and Decimal Point Drive that source current to the display. On the MAX7219, when a segment driver is turned off it is pulled to GND.
18	ISET	Connect to VDD through a resistor (RSET) to set the peak segment current (Refer to Selecting RSET Resistor section).
19	V+	Positive Supply Voltage. Connect to +5V.
24	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later.

Pad N	Pad Name	Coordinates μm		Pad N	Pad Name	Coordinates μm	
		X	Y			X	Y
1	DIN	1970	1095	13	CLK	220	795
2	DIG 0	1970	1285	14	SEG A	220	615
3	DIG 4	1970	1575	15	SEG F	220	200
4	GND	1800	1795	16	SEG B	550	200
5	DIG 6	1495	1795	17	SEG G	730	200
6	DIG 2	1200	1795	18	ISET	1030	200
7	DIG 3	1005	1795	19	V+	1210	200
8	DIG 7	710	1795	20	SEG C	1465	200
9	GND	390	1795	21	SEG E	1650	200
10	DIG 5	220	1575	22	SEG DP	1970	200
11	DIG 1	220	1285	23	SEG D	1970	615
12	LOAD	220	1095	24	DOUT	1970	795



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
A2	2.26	2.30	2.35
A3	0.97	1.02	1.07
⚠ b	0.39	—	0.47
⚠ b1	0.38	0.41	0.44
⚠ c	0.25	—	0.29
c1	0.24	0.25	0.26
⚠ D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	—	1.00
L1	1.40REF		
h	0.25	—	0.75
θ	0	—	8°

PDIP-24
CASE 724-03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01