Datasheet

MM32SPIN05x

32-Bit Microcontroller Based on Arm® Cortex®-M0

Version: 1.23_q

Content

List of Figures

List of Tables

1 General Introduction

General Introduction

1.1 Introduction

This product incorporates a high performance 32bit microcontroller with the core of Arm® Cortex®-M0. The highest operating frequency is up to 72MHz, with built-in high-speed memory, a rich set of I/O ports and peripherals connected to the external bus. This product contains one 12bit ADC, one comparator, one 16-bit general-purpose timer, one 32-bit general-purpose timer, three 16-bit basic timers, one 16-bit advanced timer, and standard communication interfaces, including one I2C, two SPI and two UART interfaces.

The device works between 2.0V to 5.5V range. The regular temperature for the device is -40°C to +85°C and -40°C to +105°C extended temperature range are also available. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 5 different packages: LQFP48, LQFP32, QFN32, QFN20 and TSSOP20.

The abundant peripherals make this microcontroller suitable for a variety of applications:

- Motor drive and application control
- Medical and handhled devices
- PC gaming peripherals and GPS platform
- Industrial applications: programmable controllers (PLCs), inverters, printers and scanners
- Alarm system, video intercom, heating, ventilation and air conditioning

1.2 Product Characteristics

- Core and system
  - 32-bit Arm® Cortex®-M0 processor as the core
  - Maximum operating frequency is up to 72MHz
  - Single cycle 32-bit hardware multiplier
  - Hardware divider(32bit)
- Memory
  - 32K bytes of Flash memory
  - 4K bytes of SRAM
  - Boot loader supports Chip Flash and ISP (In-System Programming)
- Clock, reset and power management

  - 2.0V to 5.5V power supply
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - External 4 ~ 24MHz high speed crystal oscillator
  - Embedded factory-tuned 48/72MHz high speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- One 12-bit ADC and 1μS of conversion time (up to 13 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- One comparator
- One 5-channel DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI and ADC
- Up to 39 fast I/Os:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports are capable of inputting and outputting 5V signals
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - One 16-bit 4-channel advanced-control timer with 4-channel PWM output, dead-time generation and emergency stop
  - One 16-bit timer and one 32-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - Two 16-bit timer, with one IC/OC, one OCN, deadtime generation and emergency stop and modulator gate for IR control
  - One 16-bit timer, with one IC/OC
  - Two watchdog timers (independent and window type)
  - One SysTick timer: 24-bit downcounter
- Up to 5 Communication interfaces
  - Two UARTs
  - One I2C
  - Two SPIs
- 96-bit unique ID (UID)
- Packages LQFP48, LQFP32, QFN32, QFN20 and TSSOP20

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex®-M0, please refer to Cortex®-M0 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. MM32SPIN05x device features and peripheral counts

Peripheral \ Device		MM32SPIN05PF	MM32SPIN05PT	MM32SPIN05NT	MM32SPIN05NW/TW
Flash memory -K Bytes		32	32	32	32
SRAM -K Bytes		4	4	4	4
Timers	General purpose (16 bit)	4	4	4	4
	General purpose (32 bit)	1	1	1	1
	Advanced control	1	1	1	1
Common interfaces	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	1	1	1
GPIOs		39	25	27	16
12-bit ADC	Number	1	1	1	1
	Channel	13	13	13	9
Comparators		1			
CPU frequency		72 MHz			
Operating voltage		2.0V ~ 5.5V			
Packages		LQFP48	LQFP32	QFN32	QFN20/TSSOP20

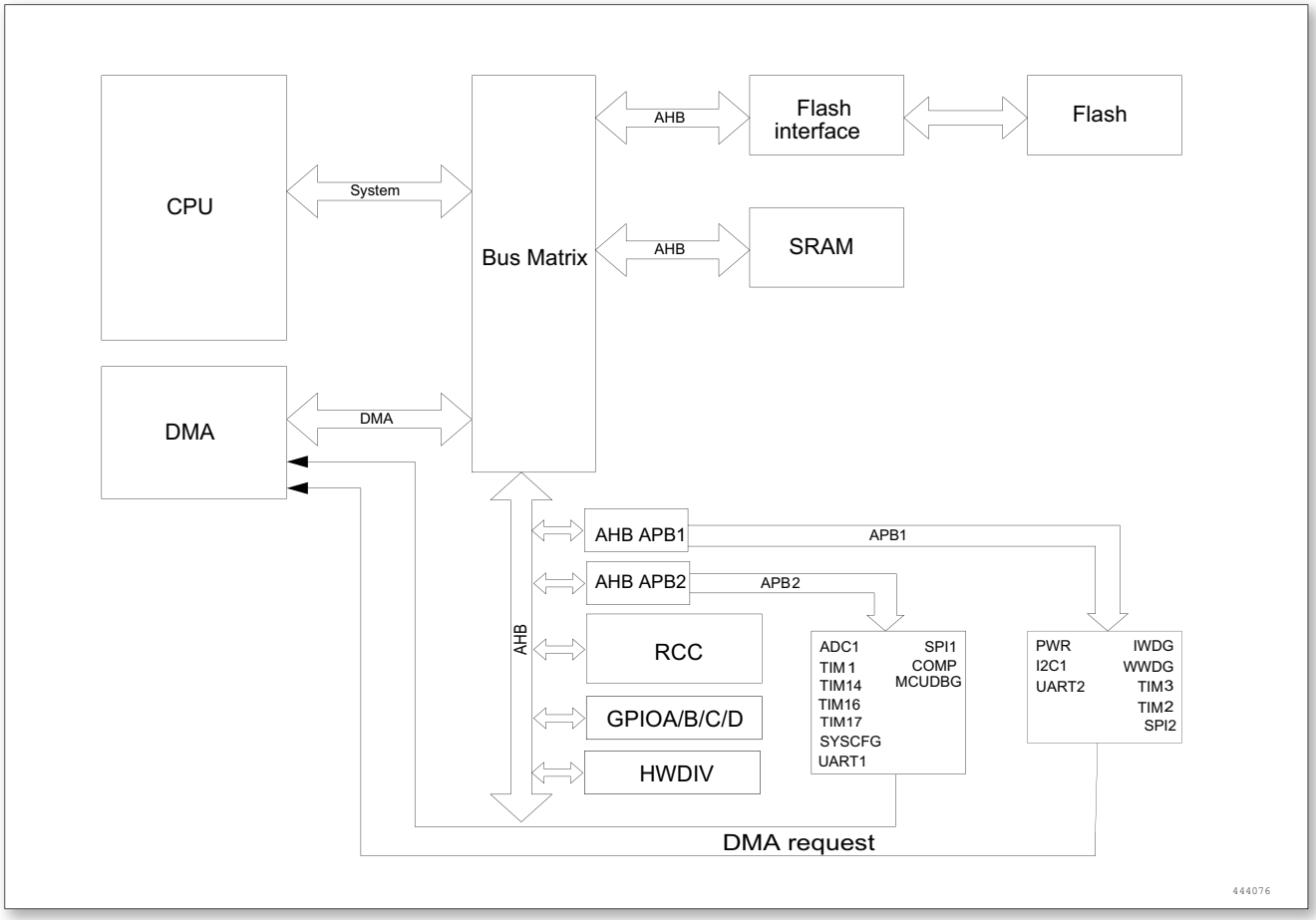

Figure 1. Block diagram

2.2 Summary

2.2.1 Arm® Cortex®-M0 with embedded flash memory and SRAM

The Arm® Cortex®-M0 processor is configurable and has multilevel pipeline 32bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Embedded flash memory

The embedded flash memory is up to 32K bytes, usable for storing programs and data.

2.2.3 Embedded SRAM

4K Bytes of embedded SRAM.

2.2.4 Nested vectored interrupt controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex®-M0 interrupt lines) with 16 pro-

grammable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the core
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher priority interrupts that arrive late
- Support tail-chaining of interrupts
- Automatically saves the processor state
- Offer automatic recovery when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.2.5 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors used to generate interrupt/event requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge or both) and can be masked independently. A pending register maintains the status of all interrupt requests. The EXTI can detect a signal with a pulse width shorter than the internal AHB clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.6 Clocks and startup

System clock selection is performed on startup, however the internal 48 MHz oscillator is selected as default CPU clock on reset. Then an external 2~24 MHz clock with failure monitoring function can be selected. If an external clock failure is detected, the clock will be isolated. The system automatically switches back to the internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure AHB frequency and high-speed APB (APB2 and APB1) domain. The maximum frequency of AHB and high-speed APB is 72MHz. Please refer to the clock drive diagram in figure 2.

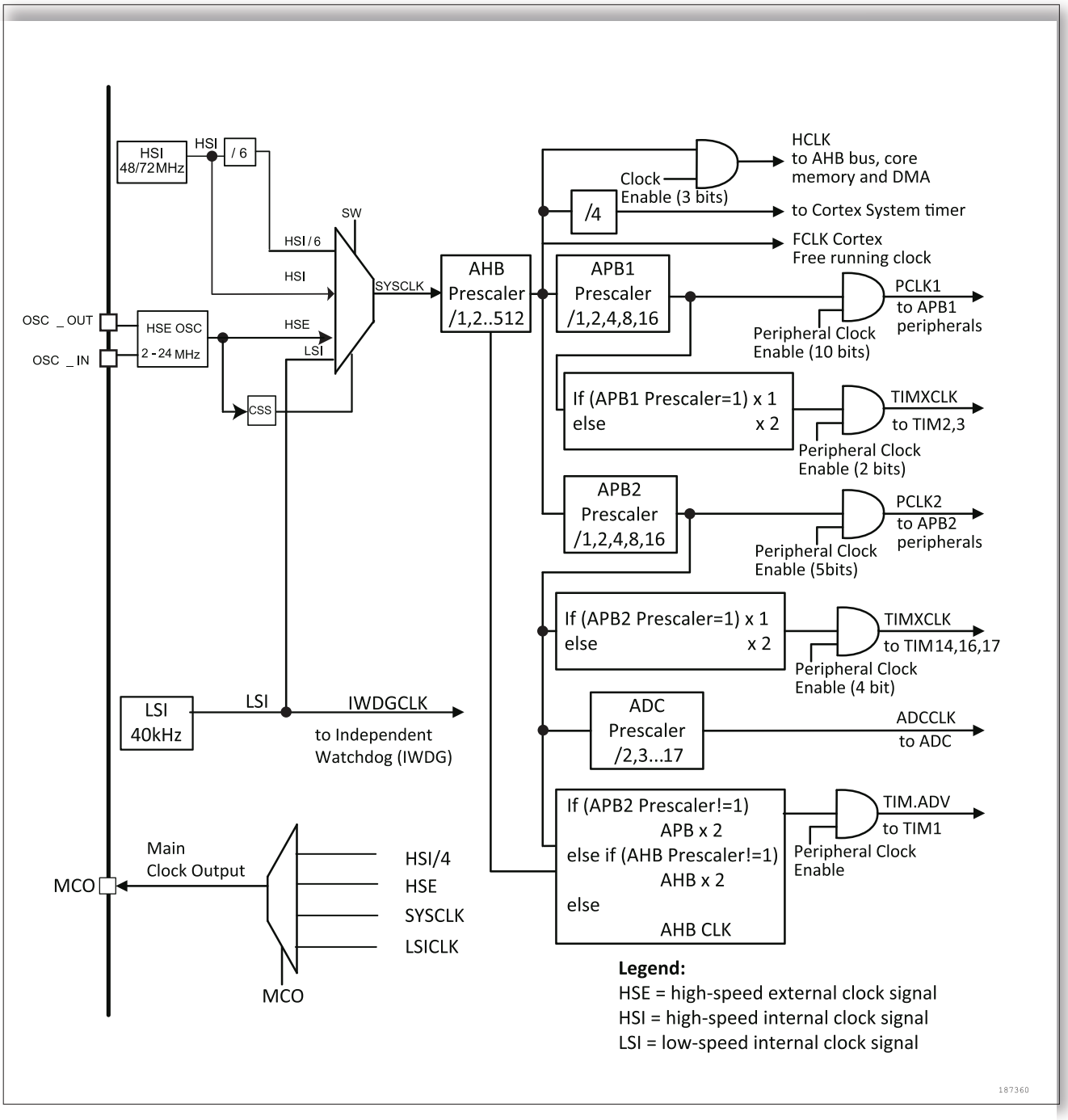

Figure 2. Clock tree

2.2.7 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is stored in the system memory, and can reprogram the flash by UART1

2.2.8 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{SSA}, V_{DDA}= 2.0V ~ 5.5V：external power supply for reset modules and oscillators. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.9 Power supply supervisors

This product has integrated power-on reset (POR)/power-down reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When V_{DD} is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.10 Voltage regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.11 Low-power modes

The product support lowpower mode to achieve the best compromise between low power consumption, short startup time and multiple wakeup events.

Table 2. Low power mode list

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
SLEEP NOW or SLEEP ON EXIT	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up event			
Stop	PDDS bit SLEEPDEEP bit WFI or WFE	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	HSI and HSE oscillator off	On
Standby	PDDS bit SLEEPDEEP bit WFI or WFE	WKUP pin rising edge, NRST pin external reset, IWDG reset			Off

Sleep mode

In the Sleep mode, only the CPU stops working. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers. The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the EXTI signals. The EXTI signal can be a wakeup signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. The entire 1.5V power supply domain is disconnected. HSI and HSE oscillators are also turned off. They can be woken up by the rising edge of WKUP pin, external reset of NRST pin and IWDG reset. They also can be woken up by the watchdog timer without reset. The contents of SRAM and registers will be lost.

2.2.12 Direct memory access controller (DMA)

The flexible 5 way universal DMA can manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC and general-purpose, basic, advanced control timer TIMx.

2.2.13 Timers and watchdogs

The product includes one advanced timer, two general-purpose timers, three basic timers, two watchdog timers and one SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
Basic	TIM14	16-bit	Up	integer from 1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	Yes

Advanced-control timer (TIM1)

The advanced control timer is composed of one 16-bit counter, four capture/compare channels and one three-phase complementary PWM generator. It has complementary PWM outputs with dead time insertion and can be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center alignment mode)
- Single pulse output

If configured as a 16-bit general-purpose timer, it has the same features as a TIM2 timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of generalpurpose TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

Two synchronizable general-purpose timers (TIM2, TIM3) are built into the product. The

general-purpose timer has one 16/32bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

General-purpose timers 32-bit

The general-purpose timer has one 32-bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

General-purpose timers 16-bit

The general-purpose timer has one 16-bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

The general-purpose timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. Their counters can be frozen in the debug mode. Any of the general-purpose timer can be used to produce PWM outputs. Each timer has independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1～4 Hall sensors. Each timer can produce PWM outputs, or be seen as a simple time reference.

Basic timer

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or onepulse mode output. Its counter can be frozen in debug mode.

TIM16/TIM17

Every timer is based on a 16-bit auto-reload up-counter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or one-pulse mode output. TIM16 and TIM17 have a complementary output with dead time generation and independent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit down-counter. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.14 Universal asynchronous receiver/transmitter (UART)

UART provides hardware management of the CTS, RTS.

Compatible with ISO7816 smart card mode. The UART interface supports output data lengths of 5 bits, 6 bits, 7 bits, 8 bits, and 9 bits.

All UART interface can be served by the DMA controller.

2.2.15 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode,and Fast Mode.

It supports 7-bit or 10-bit addressing modes.

2.2.16 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1 ~ 32 bits per frame. The maximum rate is 24M for master mode and 12M for slave mode.

All SPI interfaces can be served by the DMA controller.

2.2.17 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or alternate peripheral function. Most GPIO pins are shared with digital or analog alternate peripherals.

If required, the peripheral function of the I/O pins can be locked following a specific sequence in order to avoid spurious writing to the I/O registers.

2.2.18 Analog-to-digital converter (ADC)

The product is embedded with one 12-bit analog-to-digital converter (ADC) which has up to 13 external channels and is available for single-shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

All ADC can be served by the DMA controller.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timers (TIMx) and the advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

2.2.19 Hardware Dvision

The hardware division unit consists of four 32-bit data registers, which are dividend, divisor, quotient and remainder, and can be done with signed or unsigned 32-bit division. The hardware division control register USIGN can choose whether to have signed division or unsigned division.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the reader register, remainder register, or status register is read before the end, the read operation is suspended until the end of the operation.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.20 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.21 Serial wire debug port (SWDP)

Two-wire serial debug port (SW-DP) is embedded in the Arm.

An Arm SW-DP allows to be connected to a single-chip microcomputer through serial wire debugging tools.

2.2.22 Comparator (COMP)

The product has one built-in comparator which can be used independently (suitable for I/Os on all terminals) or in combination with the timer. It can also be used for a variety of functions, including:

- Trigger wakeup events in the low-power mode by analog signals
- Adjust the analog signal
- Combine with PWM outputs from timers to form a cycle-by-cycle current control loop
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Alternate I/O pins
  - The internal comparison voltage CRV can be AVDD or the partial voltage value of the internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminals to trigger the following events:
  - Capture event
  - OCref_clr event (cycle-by-cycle current control)
  - Brake event to shut off PWM rapidly

3 Pin definition

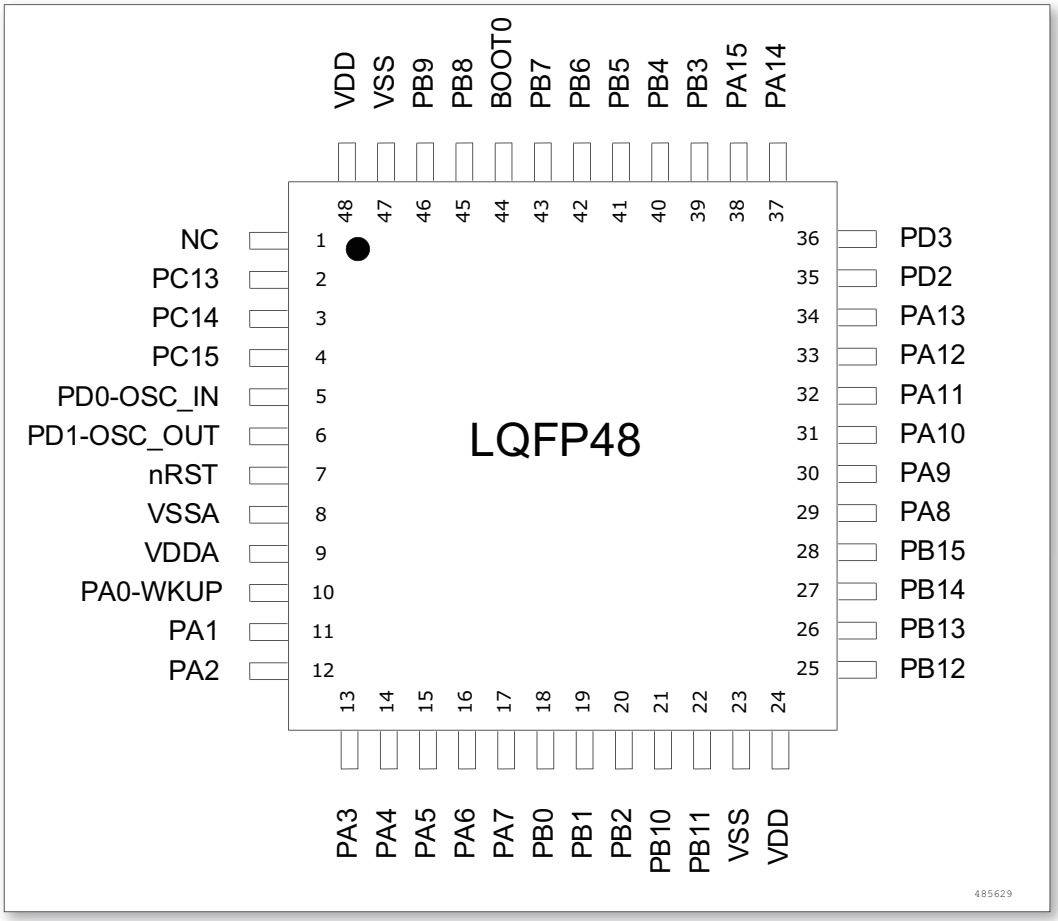

Figure 3. LQFP48 packet pinout

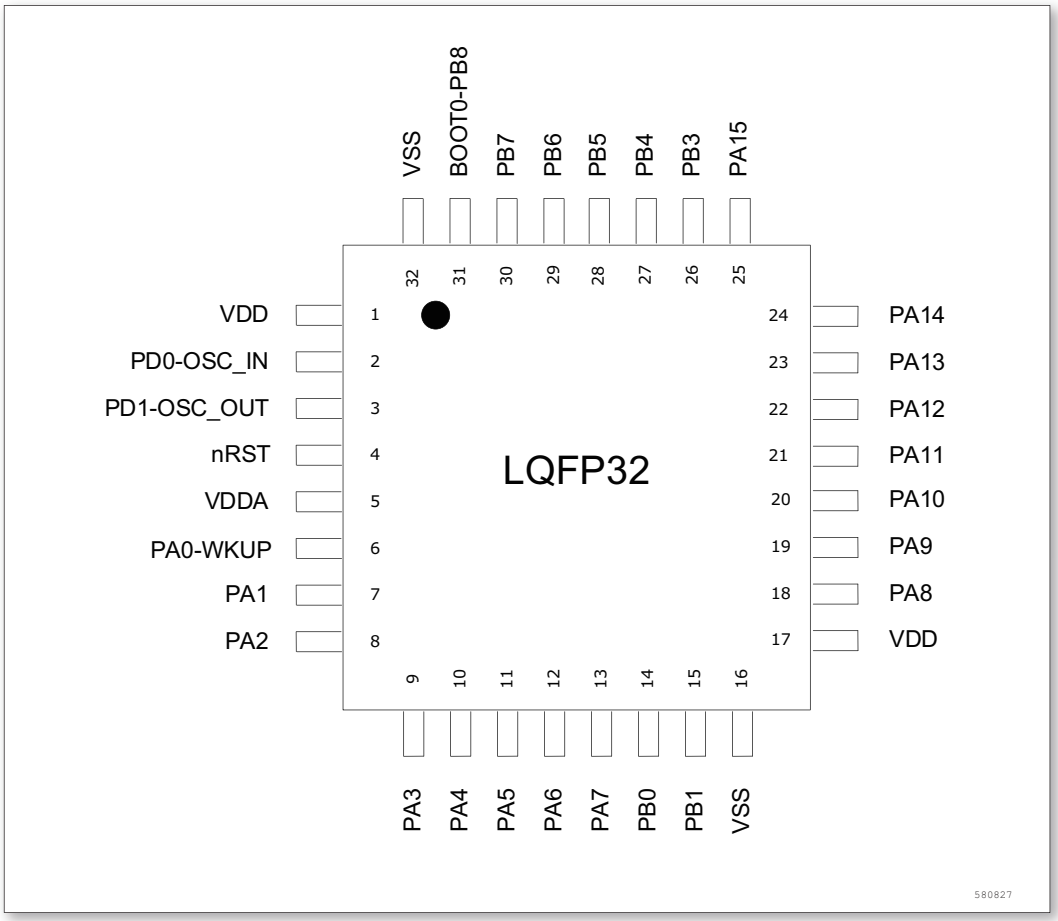

Figure 4. LQFP32 packet pinout

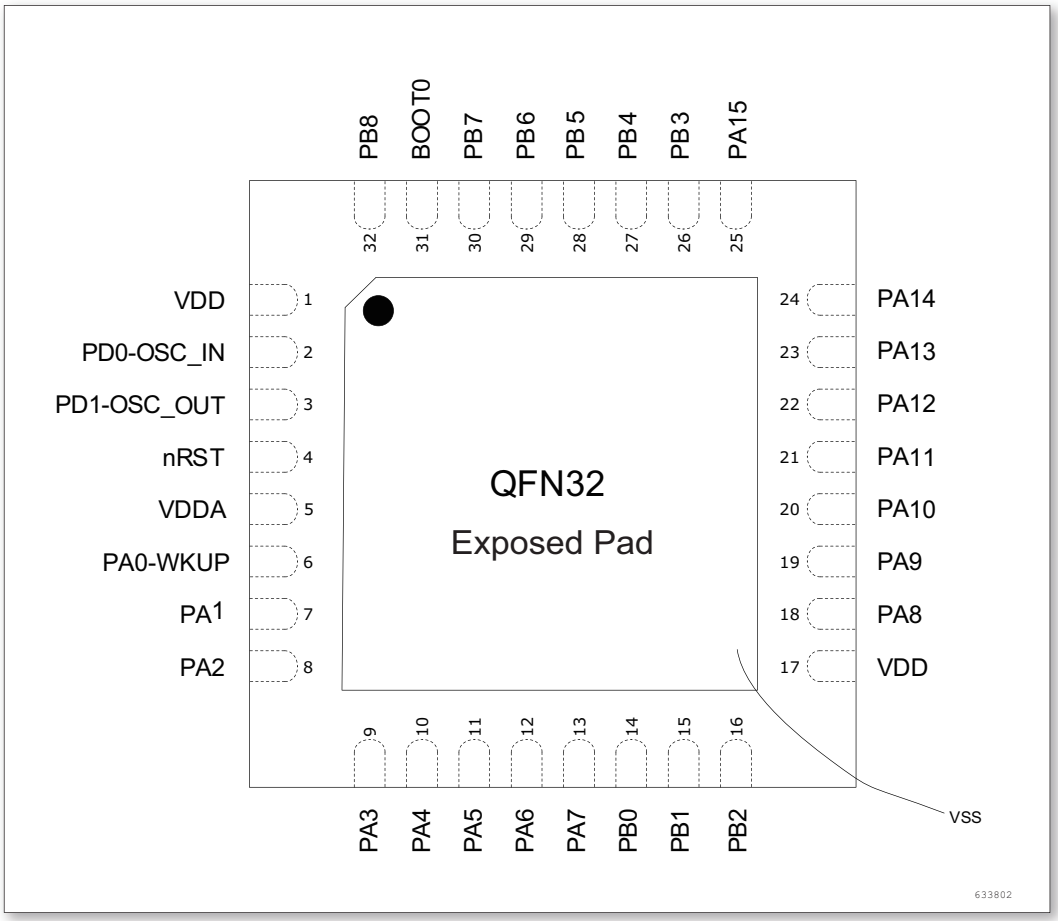

Figure 5. QFN32 packet pinout

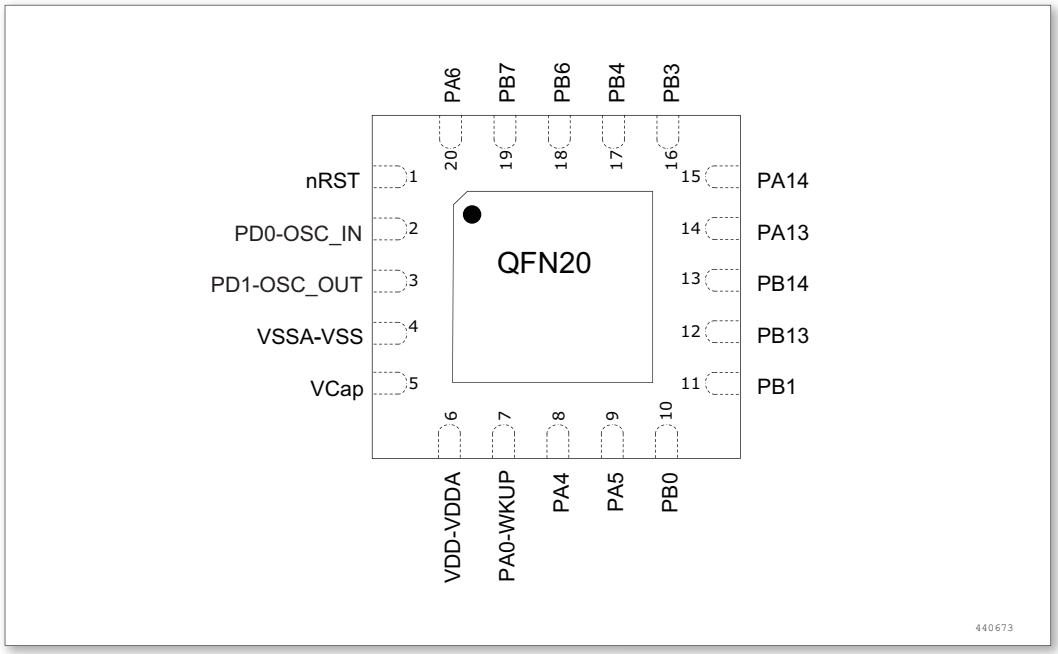

Figure 6. QFN20 packet pinout

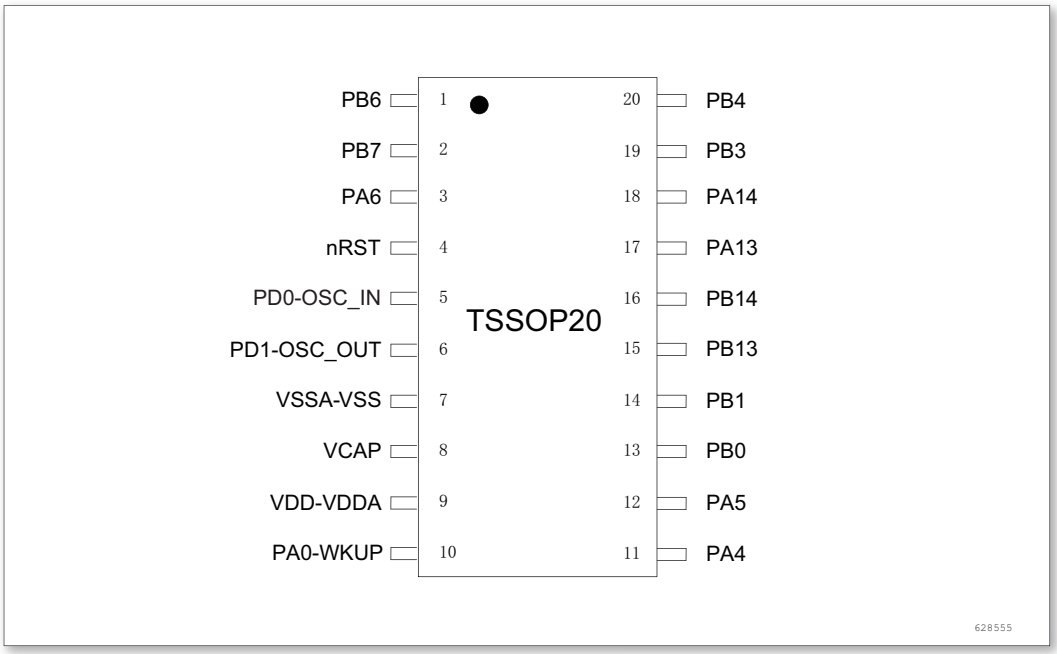

Figure 7. TSSOP20 packet pinout

Annotate: VCap should be setted to float or connect to ground with 0.1uF-0.01uF capacitor.

Table 4. Pin definitions

Pin number					Pin name	Type(1)	I/O level(2)	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
1	-	-	-	-	NC	S	-	NC	-	-
2	-	-	-	-	PC13	I/O	FT	PC13	TIM2_CH1	-
3	-	-	-	-	PC14	I/O	FT	PC14	TIM2_CH2	-
4	-	-	-	-	PC15	I/O	FT	PC15	TIM2_CH3	-
5	2	2	5	2	PD0 OSC_IN	I/O	FT	PD0	I2C1_SDA	-
6	3	3	6	3	PD1 OSC_OUT	I/O	FT	PD1	I2C1_SCL	-
7	4	4	4	1	nRST	I/O	FT	nRST	-	-
8	-	0	-	4	VSSA	S	-	VSSA	-	-
9	5	5	9	6	VDDA VDD(3)	S	-	VDDA	-	-
10	6	6	10	7	PA0 WKUP	I/O	TC	PA0	UART2_CTS/ TIM2_CH1_ETR/ SPI2_NSS/ TIM2_CH3/ COMP1_OUT	ADC1_VIN[0]

Pin number					Pin name	Type[1]	I/O level[2]	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
11	7	7	-	-	PA1	I/O	TC	PA1	UART2_RTS/ TIM2_CH2	ADC1_VIN[1]/ COMP1_INP[0]
12	8	8	-	-	PA2	I/O	TC	PA2	UART2_TX/ TIM2_CH3/ SPI2_NSS	ADC1_VIN[2]/ COMP1_INP[1]
13	9	9	-	-	PA3	I/O	TC	PA3	UART2_RX/ TIM2_CH4	ADC1_VIN[3]/ COMP1_INP[2]
14	10	10	11	8	PA4	I/O	TC	PA4	SPI1_NSS/ TIM1_BKIN/ TIM14_CH1/ I2C1_SDA	ADC1_VIN[4]/ COMP1_INP[3]
15	11	11	12	9	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR/ TIM1_ETR/ I2C1_SCL/ TIM1_CH3N	ADC1_VIN[5]/ COMP1_INM[0]
16	12	12	3	20	PA6	I/O	TC	PA6	SPI1_MISO/ TIM3_CH1/ TIM1_BKIN/ UART2_RX/ TIM1_ETR/ TIM16_CH1/ TIM1_CH3/ COMP1_OUT	ADC1_VIN[6]/ COMP1_INM[1]
17	13	13	-	-	PA7	I/O	TC	PA7	SPI1_MOSI/ TIM3_CH2/ TIM1_CH1N/ TIM14_CH1/ TIM17_CH1/ TIM1_CH2N/ TIM1_CH3N	ADC1_VIN[7]/ COMP1_INM[2]
18	14	14	13	10	PB0	I/O	TC	PB0	TIM3_CH3/ TIM1_CH2N/ TIM1_CH1N/ TIM1_CH3	ADC1_VIN[8]

Pin number					Pin name	Type[1]	I/O level[2]	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
19	15	15	14	11	PB1	I/O	TC	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ TIM1_CH4/ TIM1_CH2N/ MCO/ TIM1_CH2/ TIM1_CH1N	ADC1_VIN[9]
20	-	16	-	-	PB2	I/O	FT	PB2	-	-
21	-	-	-	-	PB10	I/O	FT	PB10	I2C1_SCL/ TIM2_CH3/ SPI2_SCK	-
22	-	-	-	-	PB11	I/O	FT	PB11	I2C1_SDA/ TIM2_CH4	-
23	16	0	7	4	VSS	S	-	VSS	-	-
24	17	17	9	6	VDD	S	-	VDD	-	-
25	-	-	-	-	PB12	I/O	FT	PB12	SPI2_NSS/ SPI2_SCK/ TIM1_BKIN/ SPI2_MOSI/ SPI2_MISO	-
26	-	-	15	12	PB13	I/O	FT	PB13	SPI2_SCK/ SPI2_MISO/ TIM1_CH1N/ SPI2_NSS/ SPI2_MOSI/ I2C1_SCL/ TIM1_CH3N/ TIM2_CH1	-
27	-	-	16	13	PB14	I/O	FT	PB14	SPI2_MISO/ SPI2_MOSI/ TIM1_CH2N/ SPI2_SCK/ SPI2_NSS/ I2C1_SDA/ TIM1_CH3/ TIM1_CH1	-

Pin number					Pin name	Type[1]	I/O level[2]	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
28	-	-	-	-	PB15	I/O	FT	PB15	SPI2_MOSI/ SPI2_NSS/ TIM1_CH3N/ SPI2_MISO/ SPI2_SCK/ TIM1_CH2N/ TIM1_CH2	-
29	18	18	-	-	PA8	I/O	FT	PA8	MCO/ TIM1_CH1/ TIM1_CH2/ TIM1_CH3	-
30	19	19	-	-	PA9	I/O	FT	PA9	UART1_TX/ TIM1_CH2/ UART1_RX/ I2C1_SCL/ MCO/ TIM1_CH1N/ TIM1_CH4	-
31	20	20	-	-	PA10	I/O	FT	PA10	TIM17_BKIN/ UART1_RX/ TIM1_CH3/ UART1_TX/ I2C1_SDA/ TIM1_CH1/ SPI2_SCK	-
32	21	21	-	-	PA11	I/O	FT	PA11	UART1_CTS/ SPI2_MOSI/ TIM1_CH4/ I2C1_SCL/ COMP1_OUT	-
33	22	22	-	-	PA12	I/O	FT	PA12	UART1_RTS/ TIM1_ETR/ SPI2_MISO/ I2C1_SDA/ TIM1_CH2	-

Pin number					Pin name	Type(1)	I/O level(2)	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
34	23	23	17	14	PA13	I/O	FT	PA13	SWDIO/ SPI2_MISO/ MCO/ TIM1_CH2/ TIM1_BKIN	-
35	-	-	-	-	PD2	I/O	FT	PD2	-	-
36	-	-	-	-	PD3	I/O	FT	PD3	-	-
37	24	24	18	15	PA14	I/O	FT	PA14	SWDCLK/ UART2_TX/ SPI1_NSS	-
38	25	25	-	-	PA15	I/O	FT	PA15	SPI1_NSS/ UART2_RX/ TIM2_CH1_ETR	-
39	26	26	19	16	PB3	I/O	TC	PB3	SPI1_SCK/ TIM2_CH2/ UART1_TX/ TIM2_CH3/ TIM1_CH1/ TIM2_CH1	ADC1_VIN[10]
40	27	27	20	17	PB4	I/O	TC	PB4	SPI1_MISO/ TIM3_CH1/ UART1_RX/ TIM17_BKIN/ TIM1_CH2/ TIM2_CH2	ADC1_VIN[11]
41	28	28	-	-	PB5	I/O	FT	PB5	SPI1_MOSI/ TIM3_CH2/ TIM16_BKIN/ MCO/ TIM1_CH3/ TIM2_CH3	-
42	29	29	1	18	PB6	I/O	FT	PB6	UART1_TX/ I2C1_SCL/ TIM16_CH1N/ TIM2_CH1	-

Pin number					Pin name	Type[1]	I/O level[2]	Main function	Alternate functions	Additional functions
LQFP 48	LQFP 32	QFN 32	TSSOP 20	QFN 20						
43	30	30	2	19	PB7	I/O	TC	PB7	UART1_RX/ I2C1_SDA/ TIM17_CH1N/ UART2_TX	ADC1_VIN[12]
44	31	31	-	-	BOOT0	I	FT	BOOT0	-	-
45	31	32	-	-	PB8	I/O	FT	PB8	I2C1_SCL/ TIM16_CH1/ UART2_RX	-
46	-	-	-	-	PB9	I/O	FT	PB9	I2C1_SDA/ TIM17_CH1/ TIM1_CH4/ SPI2_NSS	-
47	32	0	-	4	VSS	S	-	VSS	-	-
48	1	1	-	6	VDD	S	-	VDD	-	-
-	-	-	8	5	VCap	S	-	1.5V regulator capacitor	-	-

1. I = input, O = output, S = power supply, HiZ = high resistance.
2. FT: 5V tolerant. Input signal should be between VDD and 5V.
   TC: Standard I/O. Input signal does not exceed VDD.
3. Only exist in QFN20 and TSSOP package types.

Table 5. Alternate functions for PA port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 _ETR	SPI2_NSS	TIM2_CH3	-	-	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	SPI2_NSS	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS	-	-	TIM1_BKIN	TIM14_CH1	I2C1_SDA	-	-
PA5	SPI1_SCK	-	TIM2_CH1 _ETR	TIM1_ETR	-	I2C1_SCL	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	TIM1_CH4
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	TIM1_CH1	SPI2_SCK

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA11	-	UART1_CTS	TIM1_CH4	-	SPI2_MOSI	I2C1_SCL	-	COMP1_OUT
PA12	-	UART1_RTS	TIM1_ETR	-	SPI2_MISO	I2C1_SDA	-	TIM1_CH2
PA13	SWDIO	-	-	-	SPI2_MISO	MCO	TIM1_CH2	TIM1_BKIN
PA14	SWDCLK	UART2_TX	-	SPI1_NSS	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1_ETR	-	-	-	-	-

Table 6. Alternate functions for PB port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N
PB3	SPI1_SCK	-	TIM2_CH2	UART1_TX	TIM2_CH3	-	TIM1_CH1	TIM2_CH1
PB4	SPI1_MISO	TIM3_CH1	-	UART1_RX	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	MCO	-	-	TIM1_CH3	TIM2_CH3
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	UART2_TX	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	UART2_RX	-	-	-
PB9	-	I2C1_SDA	TIM17_CH1	-	TIM1_CH4	SPI2_NSS	-	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM1_CH3N	TIM2_CH1
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	TIM1_CH2N	TIM1_CH2

Table 7. Alternate functions for PC port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	-	-	-	-	-	-	TIM2_CH1	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 8. Alternate functions for PD port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	-	-	-	-	-	-
PD1	-	I2C1_SCL	-	-	-	-	-	-

4 Memory mapping

Memory mapping

Table 9. Memory mapping

Bus	Boundary address	Size	Peripheral	Notes
Flash	0x0000 0000 - 0x0000 7FFF	32 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT	
	0x0000 8000 - 0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 - 0x0800 7FFF	32 KB	Main Flash memory	
	0x0800 8000 - 0x1FFD FFFF	~ 256 MB	Reserved	
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 - 0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 - 0x1FFF FFFF	~ 2 KB	Reserved	
SRAM	0x2000 0000 - 0x2000 0FFF	4 KB	SRAM	
	0x2000 1000 - 0x2FFF FFFF	~ 512 MB	Reserved	
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	
	0x4000 0800 - 0x4000 27FF	8 KB	Reserved	
	0x4000 2800 - 0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved	
	0x4000 4400 - 0x4000 47FF	1 KB	UART2	
	0x4000 4800 - 0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved	
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved	
	0x4000 6400 - 0x4000 67FF	1 KB	Reserved	
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved	

Bus	Boundaryaddress	Size	Peripheral	Notes
APB1	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved	
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	
	0x4000 7400 - 0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved	
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1	
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1	
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 - 0x4001 3BFF	1 KB	Reserved	
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP	
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14	
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 - 0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA	
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 - 0x4002 13FF	1 KB	RCC	
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 - 0x4002 23FF	1 KB	Flash interface	
	0x4002 2400 - 0x4002 5FFF	15 KB	Reserved	
	0x4002 6000 - 0x4002 63FF	1 KB	Reserved	
	0x4002 6400 - 0x4002 FFFF	39 KB	Reserved	
	0x4003 0000 - 0x4003 03FF	1 KB	HDIV	
	0x4003 0400 - 0x47FF FFFF	~ 128 MB	Reserved	
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 - 0x5FFF FFFF	~ 384 MB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.2 Typical curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.3 Load capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

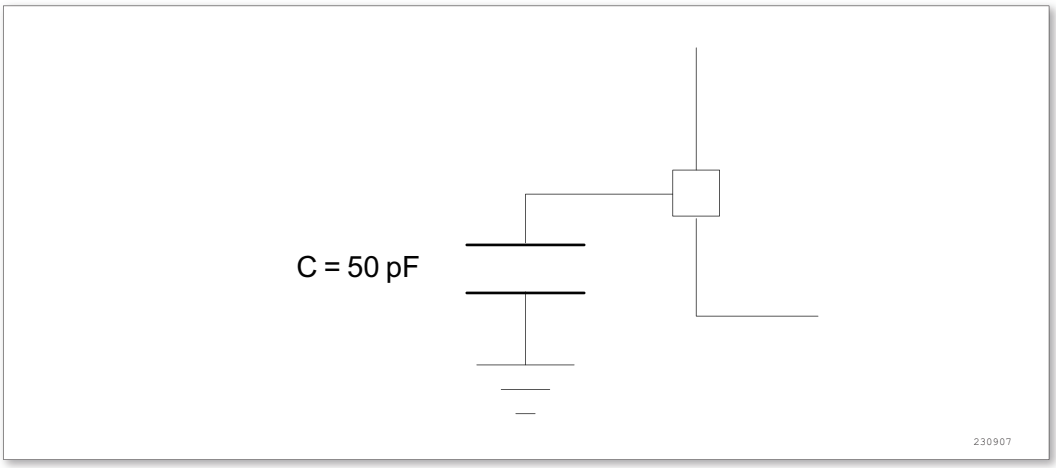

Figure 8. Load condition of the pin

5.1.4 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

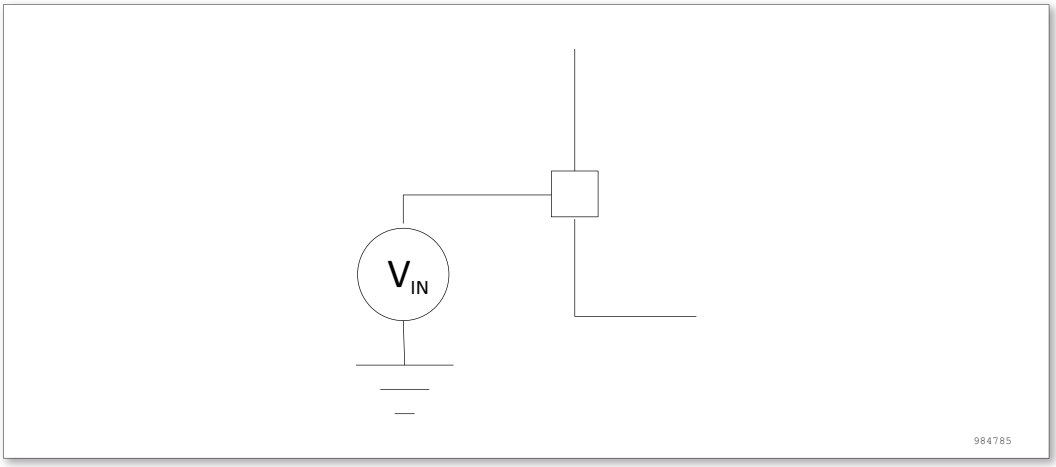

Figure 9. Pin input voltage

5.1.5 Power scheme

The power supply design scheme is shown in the figure below.

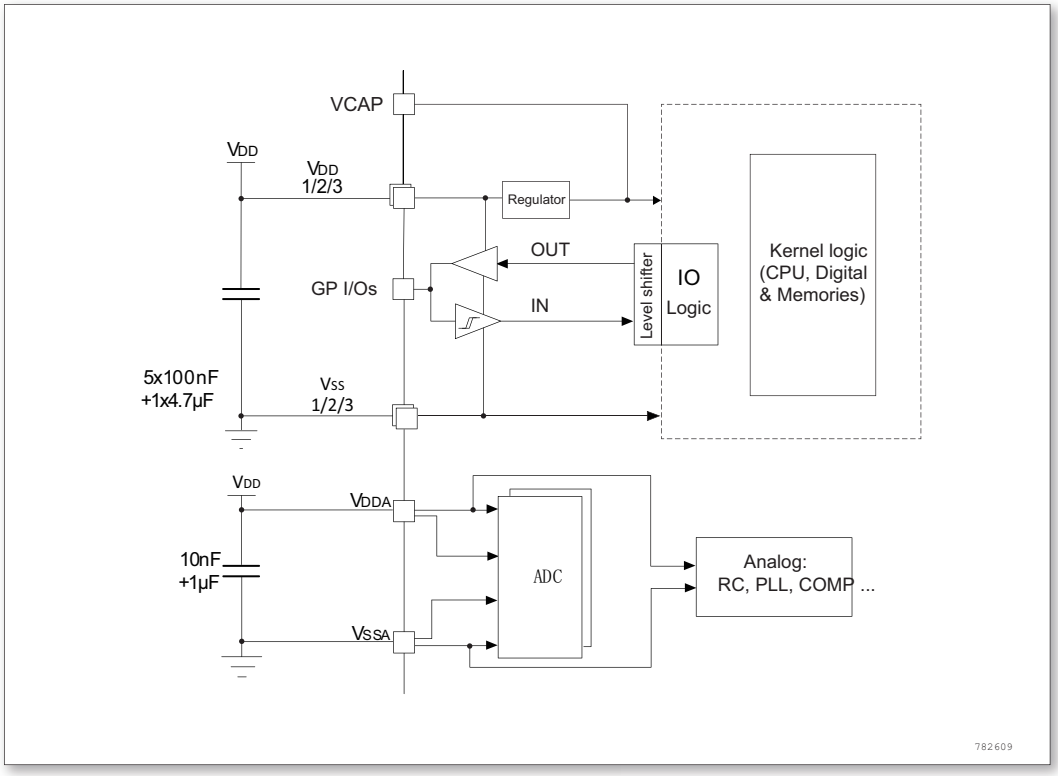

Figure 10. Power scheme

5.1.6 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

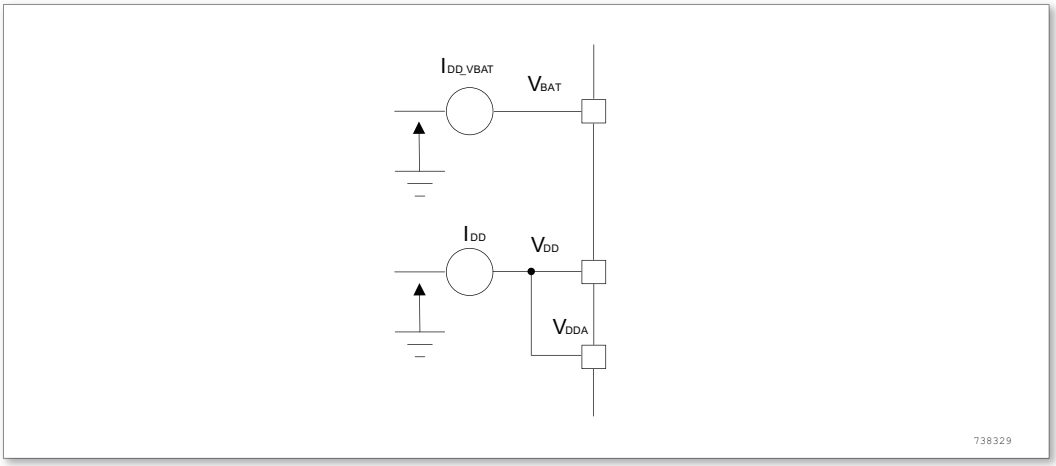

Figure 11. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 10, Table 11), it may result in that the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 10. Voltage characteristics

Symbol	Description	min	max	units
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	- 0.3	5.8	V
V_{IN}	Input voltage on the 5 Vtolerant pin (2)	V_{SS} - 0.3	5.8	
	Input voltage on other pins (2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage variations between different ground pins		50	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. V_{IN} maximum must always be respected. For information about the maximum allowed injected current values, please see the table below.

Table 11. Current characteristics

Symbol	Description	Maximum	Units
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (supply current) (1)	120	mA

Symbol	Description	Maximum	Units
I_{VSS}	Total current out of V_{SS} wire (outflow current) (1)	120	
I_{IO}	Output sink current on any I/O and control pins	20	
	Output current on any I/O and control pins	-18	
$I_{INJ(PIN)}$ (2)(3)	Injection current on NRST pin	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injection current on OSC_IN pin of HSE and OSC_IN pin LSE	±5	mA
$I_{INJ(PIN)}$ (2)(3)	injection current on other pins (4)	±5	mA
$\Sigma I_{INJ(PIN)}$ (4)	Total injection current on all I/O and control pins (4)	±25	mA

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. TThis current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/pulled between two consecutive power pins that refer to LQFP package with dense pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. A positive injection current is induced by $V_{IN} > V_{DDA}$ while a negative injection current is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3 Operating conditions

5.3.1 General operating conditions

Table 12. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	MHz
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	MHz
V_{DD}	Standard operating voltage		2.0	5.5	V
P_D	T_A=85°C(industrial) or T_A=105°C (extended industrial) power dissipation	QFN20		266	mW
		TSSOP			
V_{DDA} (1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}	2.0	5.5	V
	Analog operating voltage (ADC used)		2.5	5.5	
T_A		Maximum power dissipation	-40	105	°C
T_J	Junction temperature range		-40	125	°C

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum differ-

ence of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Thermal characteristics

The maximum junction temperature of the chip must not exceed the value given in the ”General operating conditions”.

The maximum junction temperature is calculated as follows:

$T_j max = T_A max + P_D max \times \theta_{JA}$

$T_A max$: Maximum ambient temperature

$P_D max$: Total chip power consumption, including the sum of internal and IO power consumption

Table 13. Package thermal characteristics

Symbol	Description	Value	Unit
θ_{JA}	QFN20 Thermal resistance from junction temperature to ambient temperature	75	°C/W
	TSSOP20 Thermal resistance from junction temperature to ambient temperature		

5.3.3 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 14. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD} (1)	V_{DD} rise time rate	T_A = 25°C	300	∞	μS/V
	V_{DD} fall time rate		300	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. All power-ups need to start at 0V, to ensure that the chip can be powered up reliably.

5.3.4 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 12.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.82		V
		PLS[3：0]=0000 (Falling edge)		1.71		V
		PLS[3：0]=0001 (Rising edge)		2.12		V
		PLS[3：0]=0001 (Falling edge)		2.00		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0010 (Rising edge)		2.41		V
		PLS[3：0]=0010 (Falling edge)		2.30		V
		PLS[3：0]=0011 (Rising edge)		2.71		V
		PLS[3：0]=0011 (Falling edge)		2.60		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0100 (Rising edge)		3.01		V
		PLS[3：0]=0100 (Falling edge)		2.90		V
		PLS[3：0]=0101 (Rising edge)		3.31		V
		PLS[3：0]=0101 (Falling edge)		3.19		V
		PLS[3：0]=0110 (Rising edge)		3.61		V
		PLS[3：0]=0110 (Falling edge)		3.49		V
		PLS[3：0]=0111 (Rising edge)		3.91		V
		PLS[3：0]=0111 (Falling edge)		3.79		V
		PLS[3：0]=1000 (Rising edge)		4.21		V
		PLS[3：0]=1000 (Falling edge)		4.09		V
		PLS[3：0]=1001 (Rising edge)		4.51		V
		PLS[3：0]=1001 (Falling edge)		4.39		V
		PLS[3：0]=1010 (Rising edge)		4.81		V
		PLS[3：0]=1010 (Falling edge)		4.69		V
V_{PDRhys} (2)	PDR hysteresis			110		mV
$V_{POR/PDR}$	Power on/down reset threshold			1.66		V
$T_{RSTTEMPO}$ (2)	Reset duration			0.61		ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting periods).
- The instruction prefetching function is on. When the peripherals are enabled：f_{HCLK} = f_{PCLK1}= f_{PCLK2}.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 16. Typical and maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Max(1)	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the stop mode after reset	6	μA
	Supply current in Standby mode	Enter the standby mode after reset	0.4	

1. Data based on characterization results, not tested in production.The IO state is an analog input.

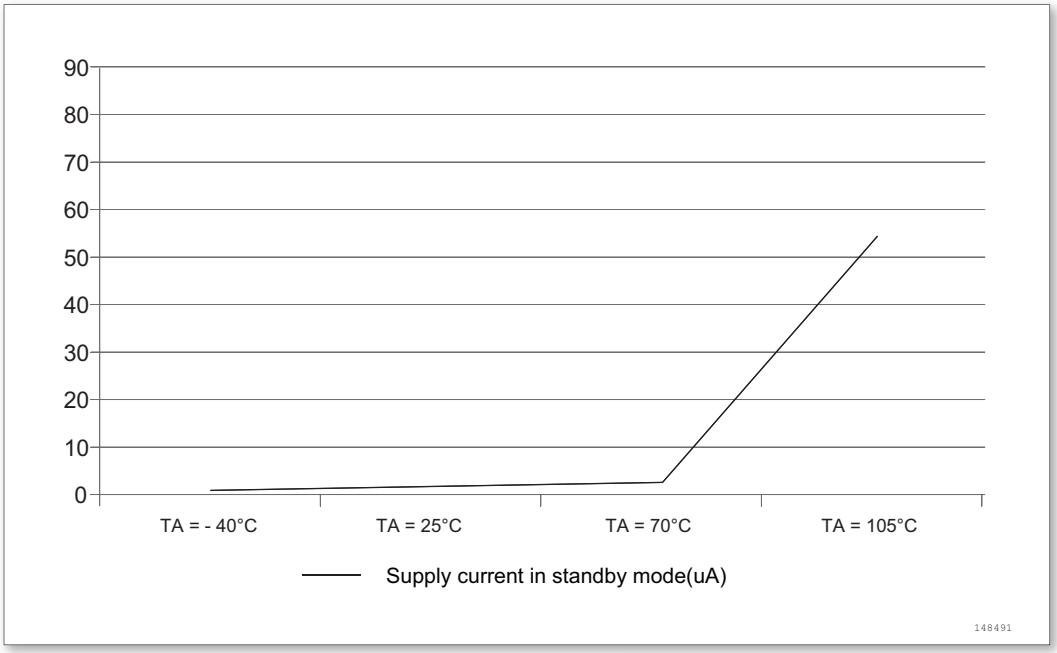

Figure 12. Typical current consumption in standby mode vs. temperature at V_{DD} = 3.3V

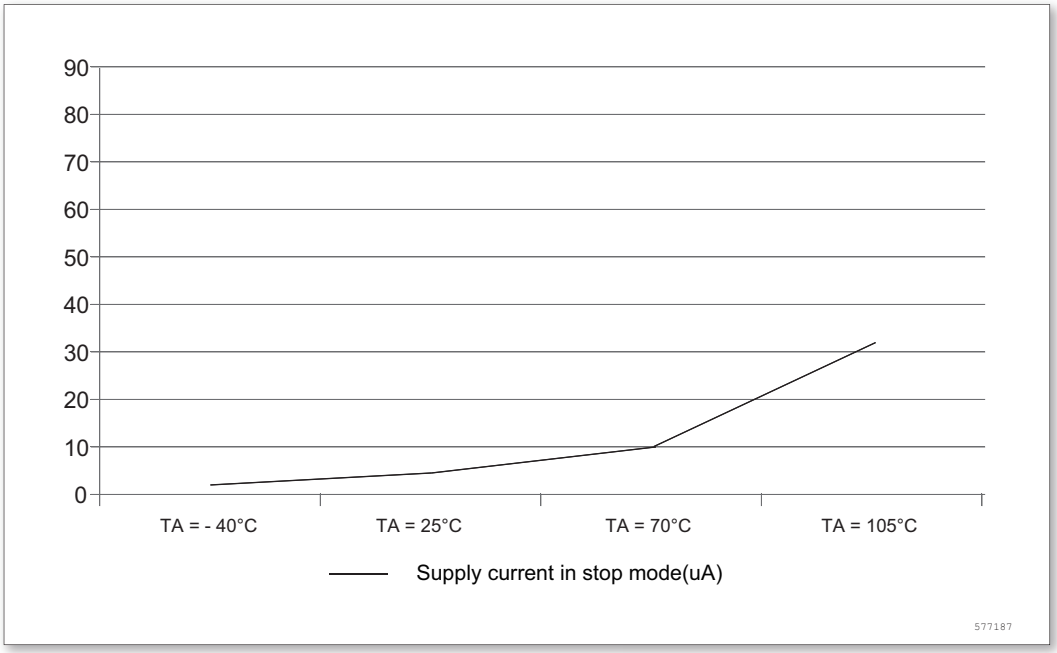

Figure 13. Typical current consumption in stop mode vs. temperature at V_{DD} = 3.3V

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration, and are connected to a static level —- V_{DD} or V_{SS} (no load).
- All the peripherals are closed, unless otherwise specified.
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting periods).
- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 12.
- The instruction prefetching function is on. When the peripherals are enabled：
  f_{HCLK} = f_{PCLK1}= f_{PCLK2}..

Note: The instruction prefetch function must be set before the clock is set and the bus is divided.

Table 17. Typical current consumption in Run mode, code executing from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in operating mode	Internal clock	72MHz	14.4	8.78	mA
			48MHz	9.57	6.25	
			8MHz	2.21	1.66	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.

Table 18. Typical current consumption in sleep mode, code executing from Flash

Symbol	Parameter	Conditions	f_{HCLK}(2)	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in sleep mode	Internal clock	72MHz	9.16	3.75	mA
			48MHz	6.44	2.71	
			8MHz	1.66	0.95	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. External clock is 8MHz, when f_{HCLK} > 8MHz choose HSI 48MHz or HSI 72MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 19. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 12.

Table 19. On-chip peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit	Peripheral		Typical consumption at 25 °C	Unit
AHB	HWDIV	2.17	μA/MHz	APB2	SPI	7.92	μA/MHz
	GPIOD	0.75			TIM1	17.04	
	GPIOC	0.58			ADC	1.54	
	GPIOB	0.71			SYSCFG	0.37	
	GPIOA	0.71			UART1	5.38	
	CRC	1.00		APB1	PWR	0.79	
	DMA	4.38			I2C	9.58	
APB2	PWM	1.75			WWDG	5.96	
	TIM17	3.29			TIM3	8.83	
	TIM16	3.17			TIM2	0.50	
	TIM14	3.17			UART2	5.96	
	COMP	0.58					

1. f_{HCLK} = 72MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each device is the default value.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of General operating conditions.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

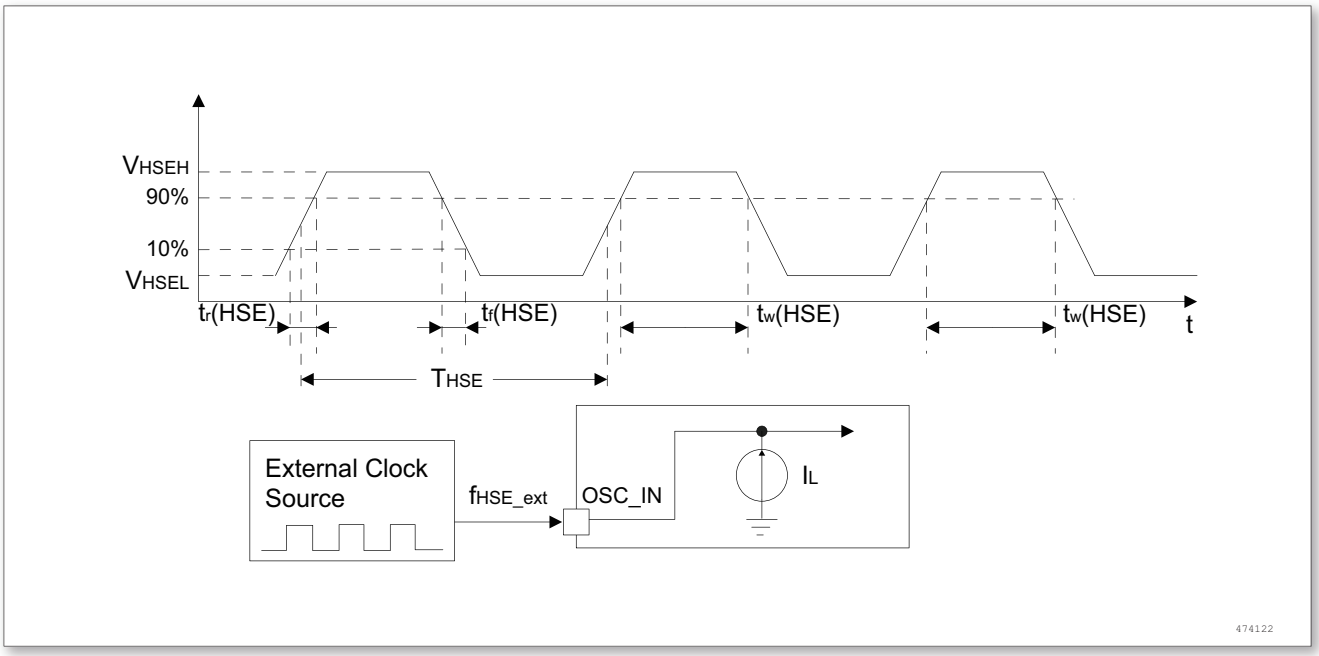

Figure 14. High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 21. HSE 8~ 24 oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	24	MHz
R_F	Feedback resistor			1000		kΩ
C_{L1} C_{L2}(3)	The proposed load capacitance corresponds to the crystal serial impedance (R_S) (4)	R_S = 30Ω		30		pF
I_2	HSE current consumption	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load			4.5	mA
g_m	Oscillator transconductance	Startup		8.5		mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		3		mS

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF (typical value) range, designed for high-frequency applications. A suitable crystal or resonator should also be carefully selected. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment the software enables HSE to a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

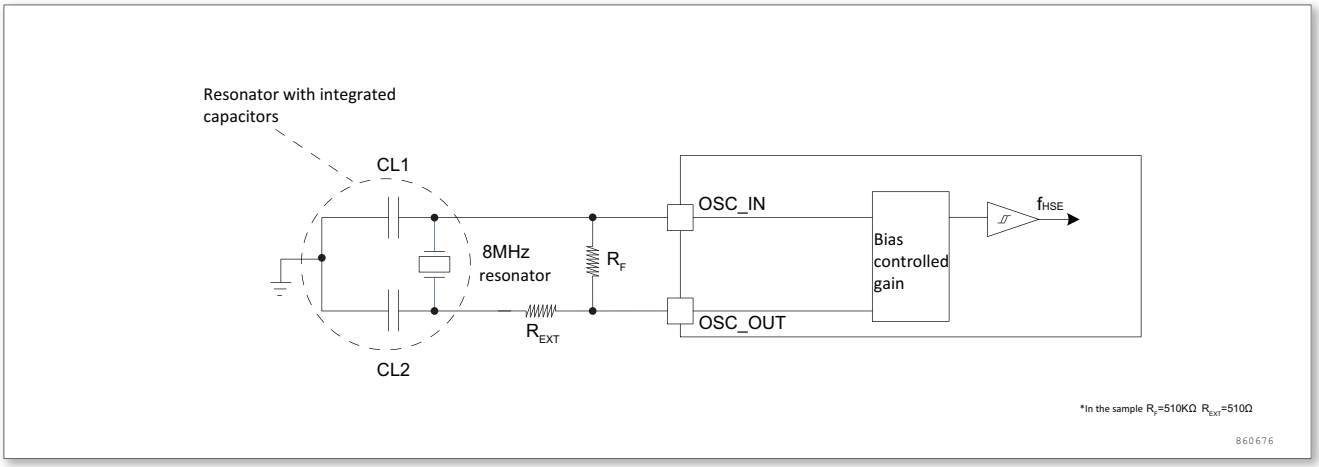

Figure 15. Typical application with an 8 MHz crystal

5.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 22. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48/72		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C ~ 105°C	-6		6	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -10°C ~ 105°C	-4		4	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time			10		μS
$I_{DD(HSI)}$	HSI oscillator power consumption			200		μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 85°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 23. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency			40		KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, Unless otherwise stated

2. Comprehensive assessment, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 24. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI clock wakeup	4.2	μS
t_{WUSTOP}(1)	Wakeup from Stop mode	HSI clock wakeup ＜ 2μS	12	μS
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI clock wakeup ＜ 2μS The regulator wakes up from the off mode ＜ 38μS	230	μS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.8 Memory characteristics

Flash memory

Table 25. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	16-bit programming time			28		μS
t_{ERASE}	Page (1024K bytes) erase time			8	10	mS
t_{ME}	Mass erase time			30	40	mS
I_{DD}	Supply current	Read mode		9		mA
		Write mode			7	mA
		Erase mode			2	mA

Table 26. Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (erase cycles)		20000			K cycle
t_{RET}	Data retention	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Guaranteed by design, not tested in production.

5.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- EFT：A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC61000-4-4standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table.

Table 27. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=+25°C, f_{HCLK}=48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that users apply EMC software optimization and conduct EMC-related prequalification tests.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and corrupted program counter) can be reproduced by manually forcing a low level on NRST or a onesecond low level on the crystal oscillator pins.

During ESD test, a voltage over the range of specification values can be directly applied to the chip. When unexpected behavior is detected, the software needs to be strengthened to prevent unrecoverable errors.

5.3.10 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JEDECJS-001-2017/JS-002-2018 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 28. MCU ESD characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, Conforming to JEDECJS-001-2017	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, Conforming to JEDECJS-002-2018	±500	
I_{LU}	Latch-up current	T_A = 25°C, Conforming to JESD78E	±100	mA

5.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 10 are derived from tests. All I/O ports are compatible with CMOS.

Table 29. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	2.5V< V_{DD} < 5.5V			0.3*V_{DD}	V
V_{IH}	Input high level voltage	2.5V< V_{DD} < 5.5V	0.7*V_{DD}			V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis(1)	2.5V< V_{DD} < 5.5V		0.1*V_{DD}		V
I_{lkg}	Input leakage current(2)	2.5V< V_{DD} < 5.5V	-1		1	μA
R_{PU}	Weak pull-up equivalent resistor(3)	2.5V< V_{DD} < 5.5V	10		50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	2.5V< V_{DD} < 5.5V	10		100	kΩ
C_{IO}	I/O pin capacitance	2.5V< V_{DD} < 5.5V			10	pF

1. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
2. Pull-up and pull-down resistors are MOS.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 5.2：

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the

ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 12. All I/O ports are CMOS compatible.

Table 30. Output voltage characteristics

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)(3)	Output high level voltage		2.80			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			0.80	V
	V_{OH} (2)(3)	Output high level voltage		2.20			V
10	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.60			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.00	V
	V_{OH} (2)(3)	Output high level voltage		1.80			V
01	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)	Output high level voltage		2.60			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.40			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.40	V
	V_{OH} (2)(3)	Output high level voltage					V

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 16 and Table 31, respectively.

Unless otherwise stated, the parameters listed in Table 31 are measured using the ambient temperature and supply voltage in accordance with the condition Table 10.

Table 31. I/O AC characteristics(1)

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	tf	Fall time from high level output to low level output	C_L=50pF, V_{DD}=3.3V		4.0		ns
	tr	Rise time from low level output to high level output			5.0		ns
10	tf	Fall time from high level output to low level output			5.0		ns
	tr	Rise time from low level output to high level output			6.2		ns
01	tf	Fall time from high level output to low level output			7.2		ns
	tr	Rise time from low level output to high level output			11.0		ns

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. The maximum frequency is defined in figure 16.

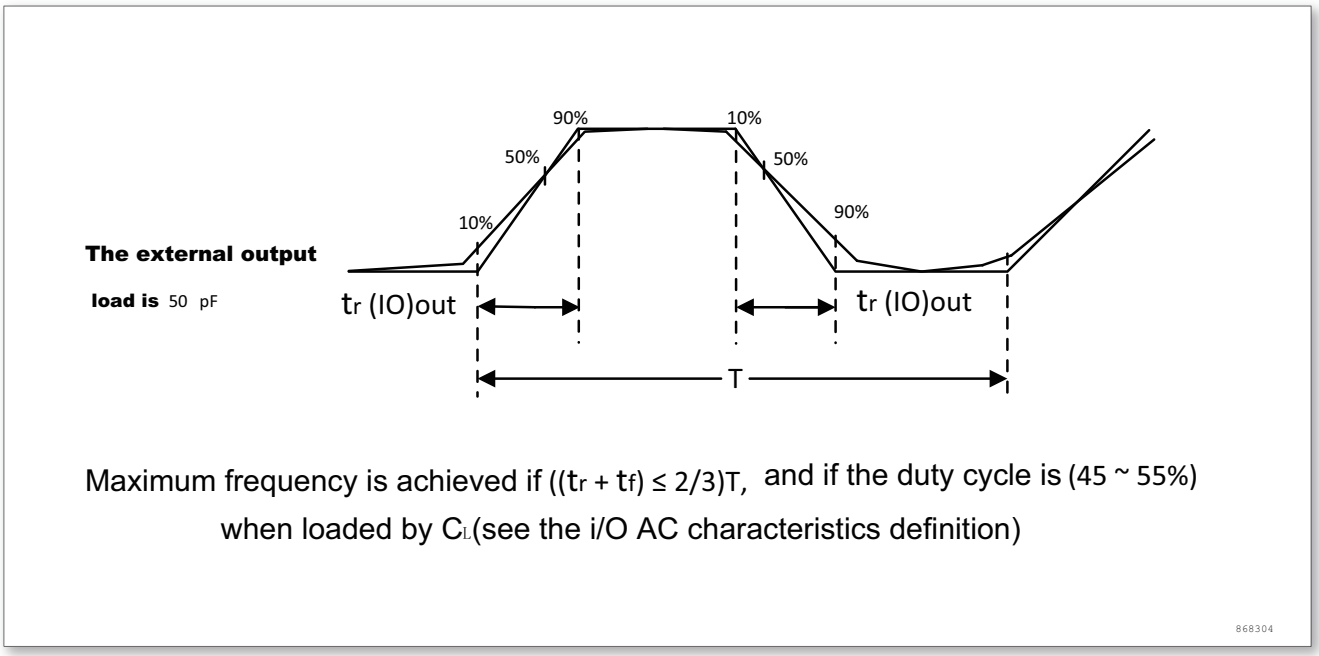

Figure 16. I/O AC characteristics

5.3.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}. Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 10.

Table 32. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.3		0.3*V_{DD}	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		0.7*V_{DD}		V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			0.1*V_{DD}		V
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN} = V_{SS}		50		kΩ
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

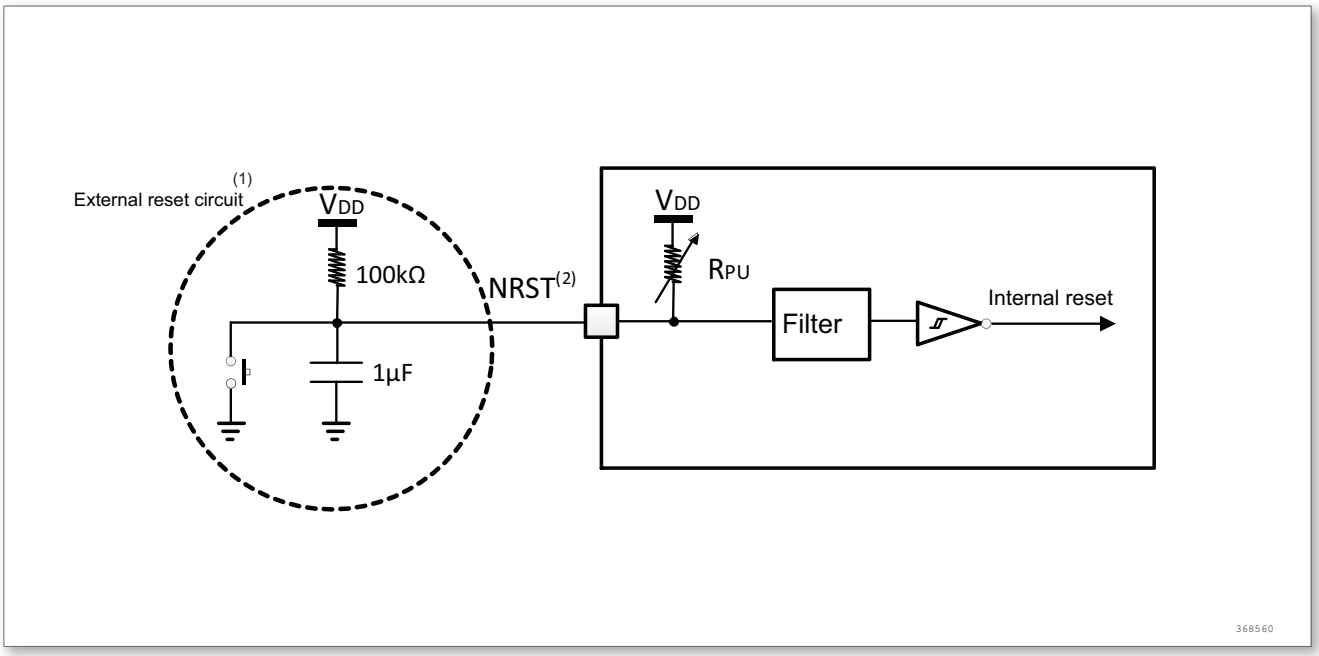

Figure 17. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 32, otherwise the MCU cannot be reset.

5.3.13 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.11.

Table 33. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24MHz	41.6		nS
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$ = 24MHz	0	24	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$24MHz	0.0417	2732	μS
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$24MHz		178.9	S

1. TIMx is a generic name.

5.3.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 34 are derived from tests performed under the ambient temperature, f_{PCLK1}frequency and supply voltage conditions summarized in Table 12.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 34, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.11.

Table 34. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

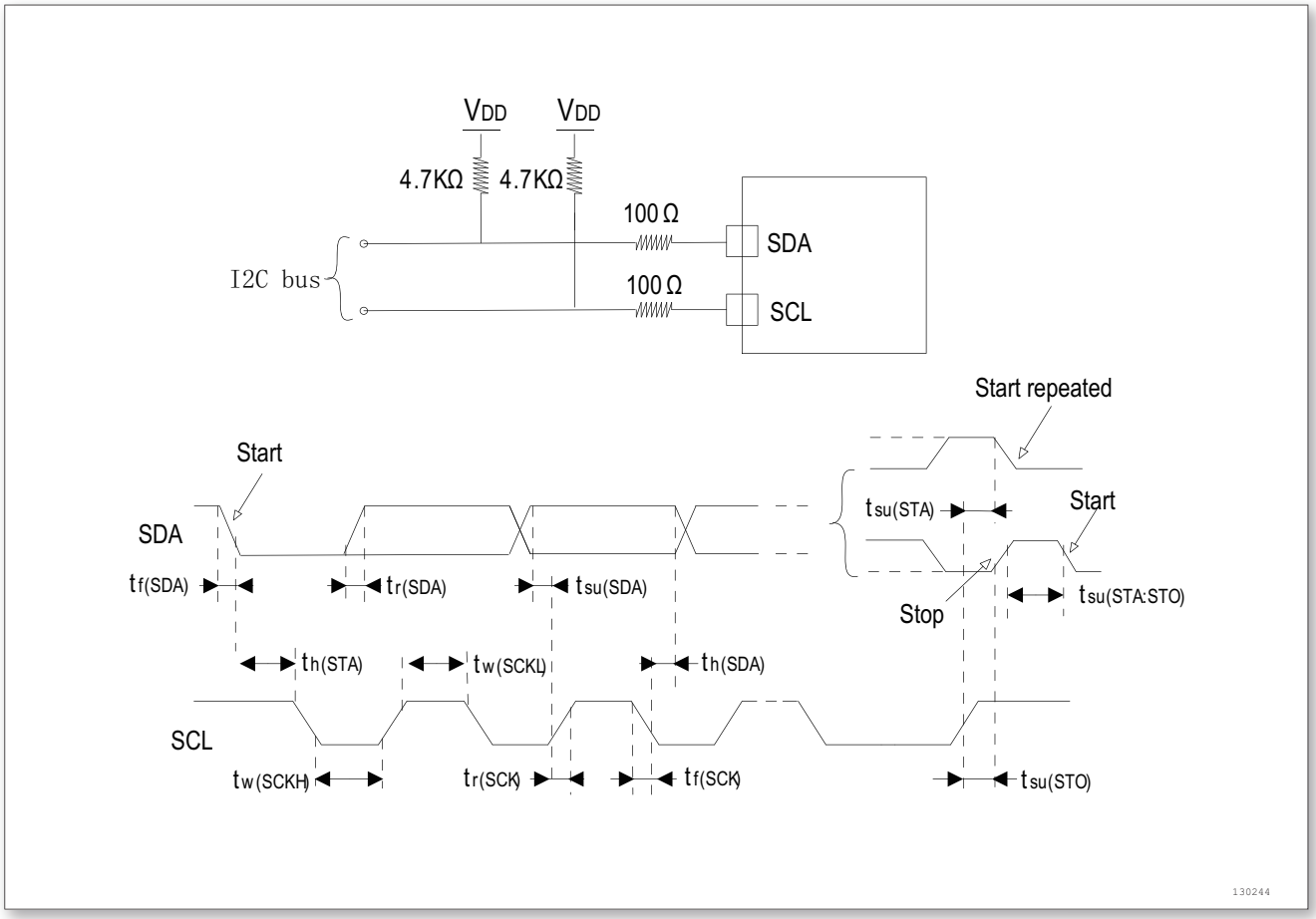

Figure 18. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 35 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 12.

Refer to subsubsec 5.3.11 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 35. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 30pF		8	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		ns
$t_{w(SCKH)}$ (2)	SCK high time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{w(SCKL)}$ (2)	SCK low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$ (2)	Data input setup time	Slave mode	1		ns
$t_{h(SI)}$ (2)	Data input hold time	Slave mode	3		ns
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$ (2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

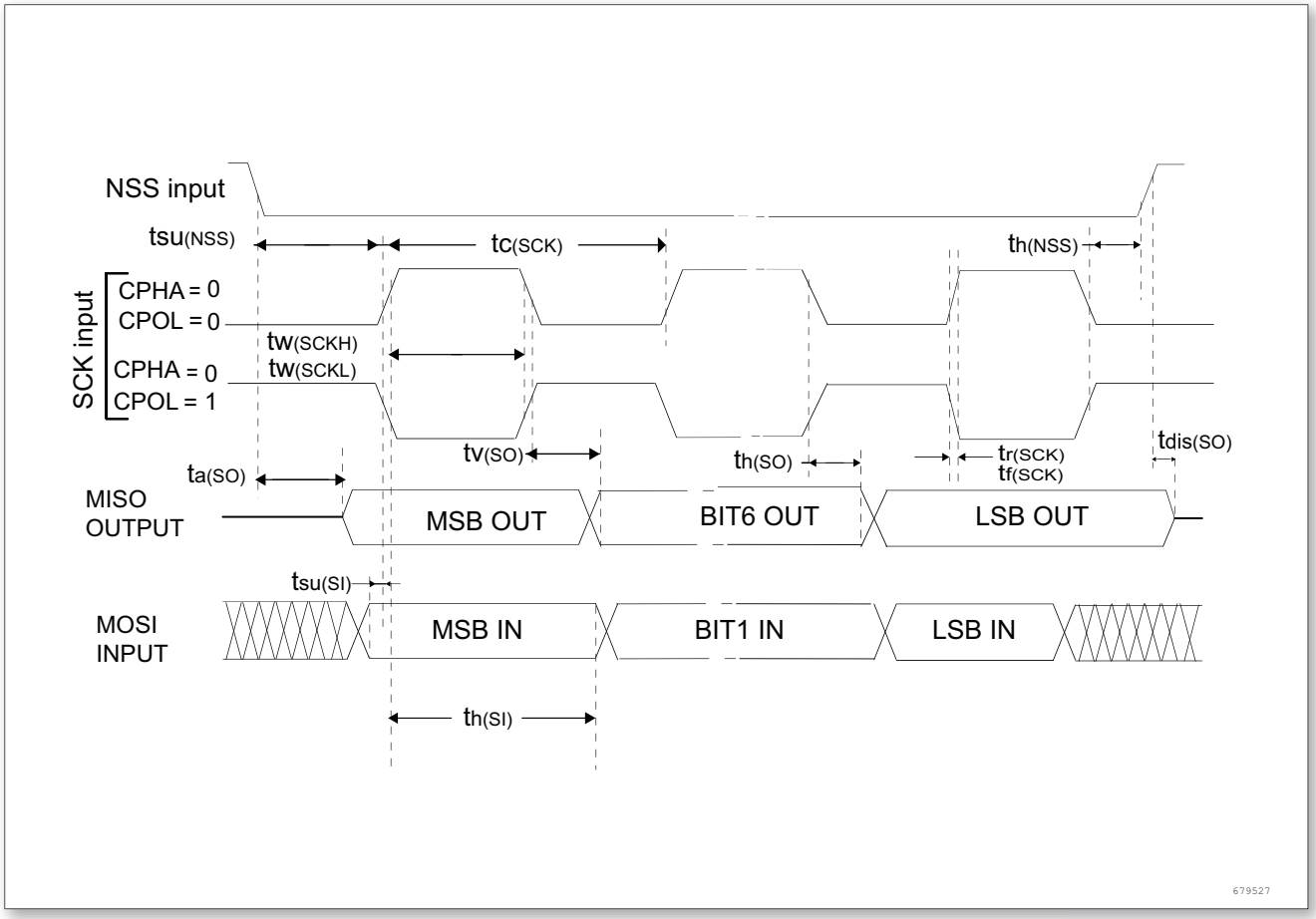

Figure 19. SPI timing diagram-slave mode and CPHA = 0

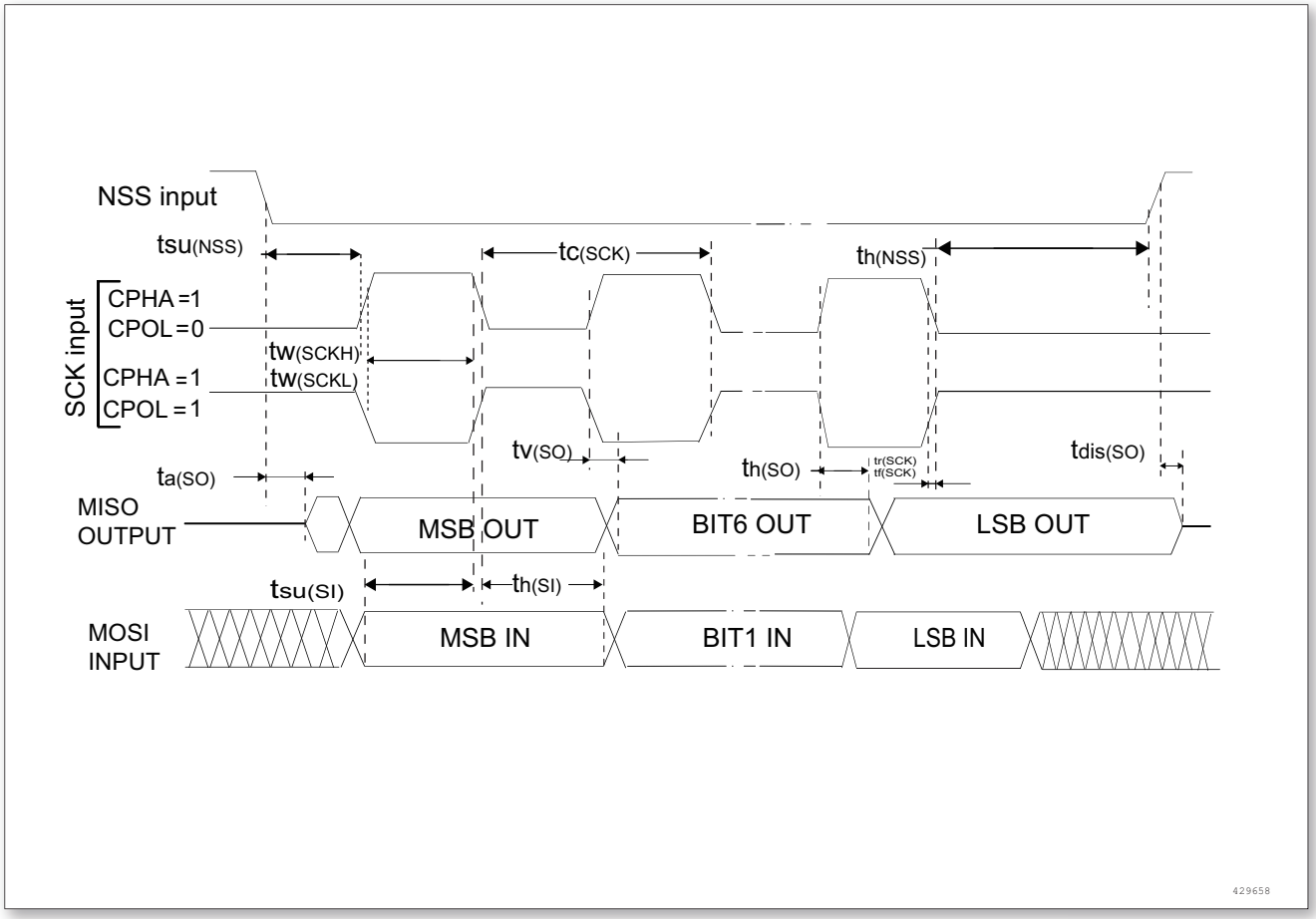

Figure 20. SPI timing diagram-slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

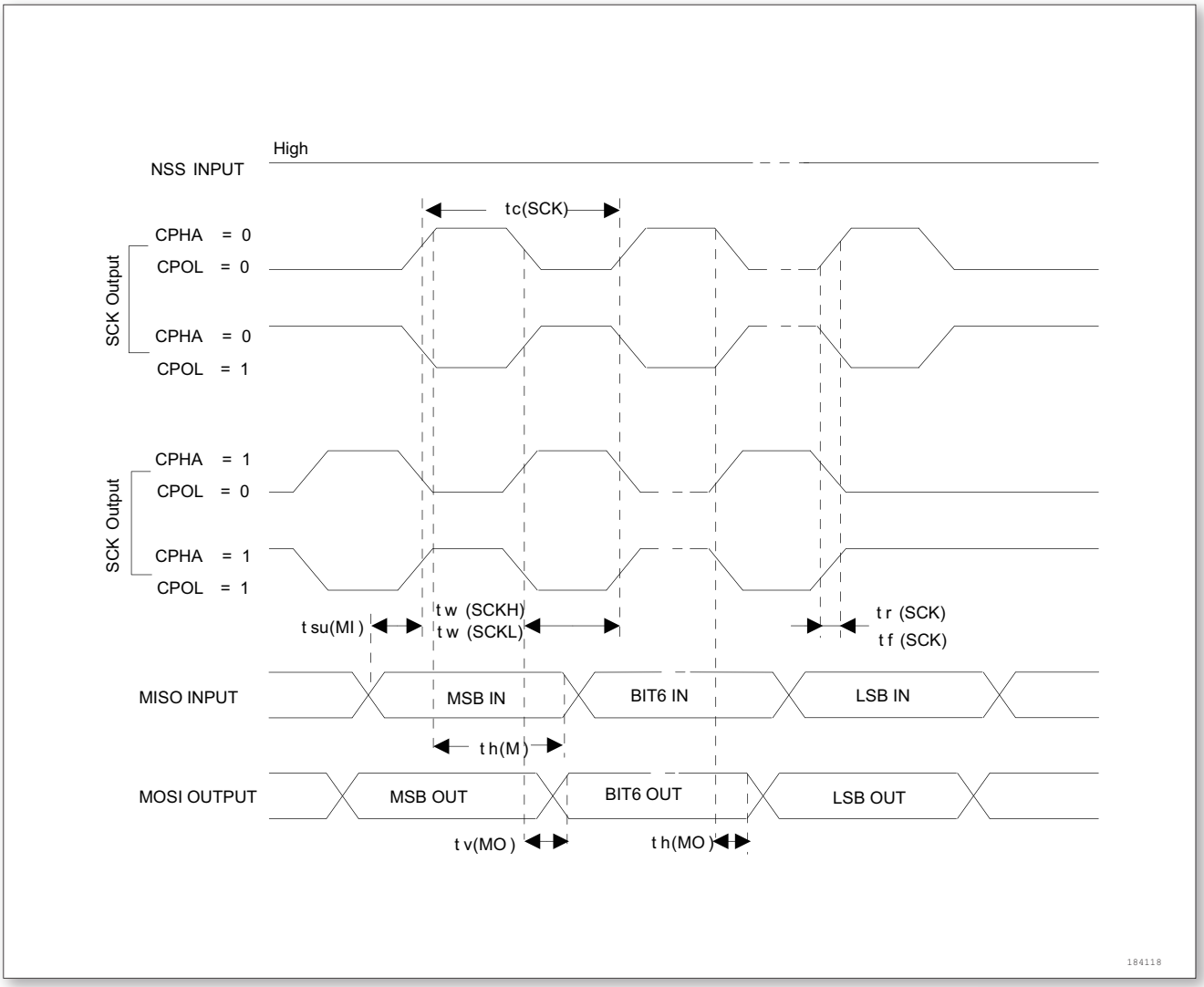

Figure 21. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.15 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 12.

Table 36. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.5	3	5.5	V
f_{ADC}	ADC clock frequency				15(1)	MHz
f_S(2)	Sampling rate				1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 15MHz			823	KHz
					1/17	$1/f_{ADC}$

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{AIN}(2)	Conversion voltage range(3)		V_{SSA}		V_{DDA}	V
R_{AIN}(2)	External sample and hold capactor		See Formulas 1 and Table 37			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor			10		pF
t_S(2)	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Stabilization time			1		μs
t_{conv}(2)	Total conversion time (including Sampling time)	f_{ADC} = 15MHz	1		16.9	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this series of products, V_{REF+} is internally connected to $_{DDA}$, V_{REF-} is internally connected to $_{SSA}$.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times (N+3) \times In(2)} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution) .

Table 37. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	0.1
7.5	0.5	4.0
13.5	0.9	7.8
28.5	1.9	17.5
41.5	2.76	25.9
55.5	3.7	34.9
71.5	4.77	45.2
239.5	16.0	153.4

1. Guaranteed by comprehensive evaluation, not tested in production.

Table 38. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz,f_{ADC} = 15MHz,R_{AIN} < 10KΩ,V_{DDA} = 3.3V，T_A = 25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. ADC Accuracy vs Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsubsec 5.3.12 does not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

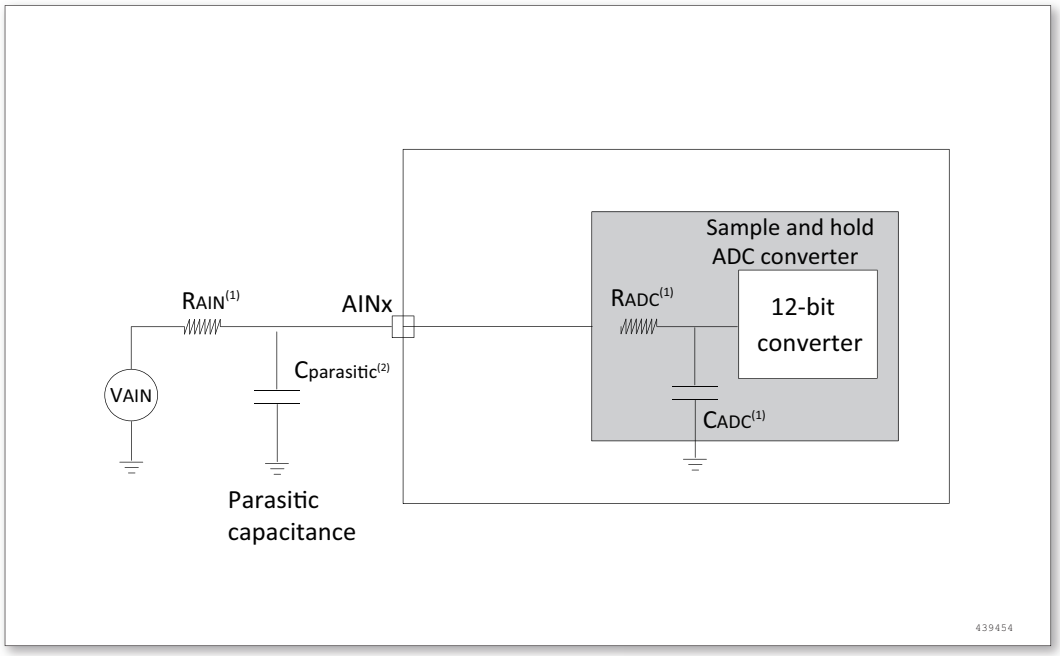

Figure 22. Typical connection diagram using the ADC

1. See Table 38 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10 nFcapacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

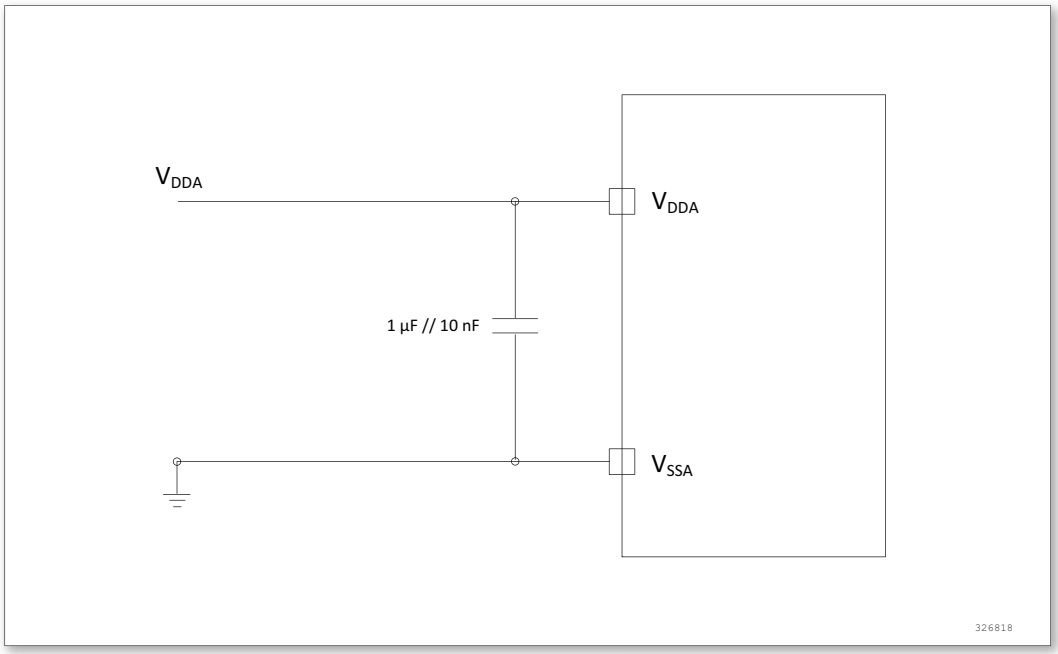

Figure 23. Power supply and reference power supply decoupling circuit

5.3.16 Temperature sensor characteristics

Table 39. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start} (2)	Setup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

5.3.17 Comparator characteristics

Table 40. Comparator characteristics

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	00		0		mV
HYST	Hysteresis	01		15		mV
HYST	Hysteresis	10		30		mV

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
OFFSET	Offset voltage	01	3.23	7.51	12.08	mV
OFFSET	Offset voltage	10	9.79	15	20.8	mV
OFFSET	Offset voltage	11	34.25	47.4	62.22	mV
DELAY(1)	Propagation delay	00		80		nS
DELAY(1)	Propagation delay	01		51		nS
DELAY(1)	Propagation delay	10		26		nS
DELAY(1)	Propagation delay	11		9		nS
I_q(2)	Operating current mean	00		4.5		uA
I_q(2)	Operating current mean	01		4.4		uA
I_q(2)	Operating current mean	10		4.4		uA
I_q(2)	Operating current mean	11		4.4		uA

1. The output flips 50% of the time and the time difference between the input and the flip.
2. Total current consumption, operating current.

6 Package information

Package information

6.1 Packaging LQFP48

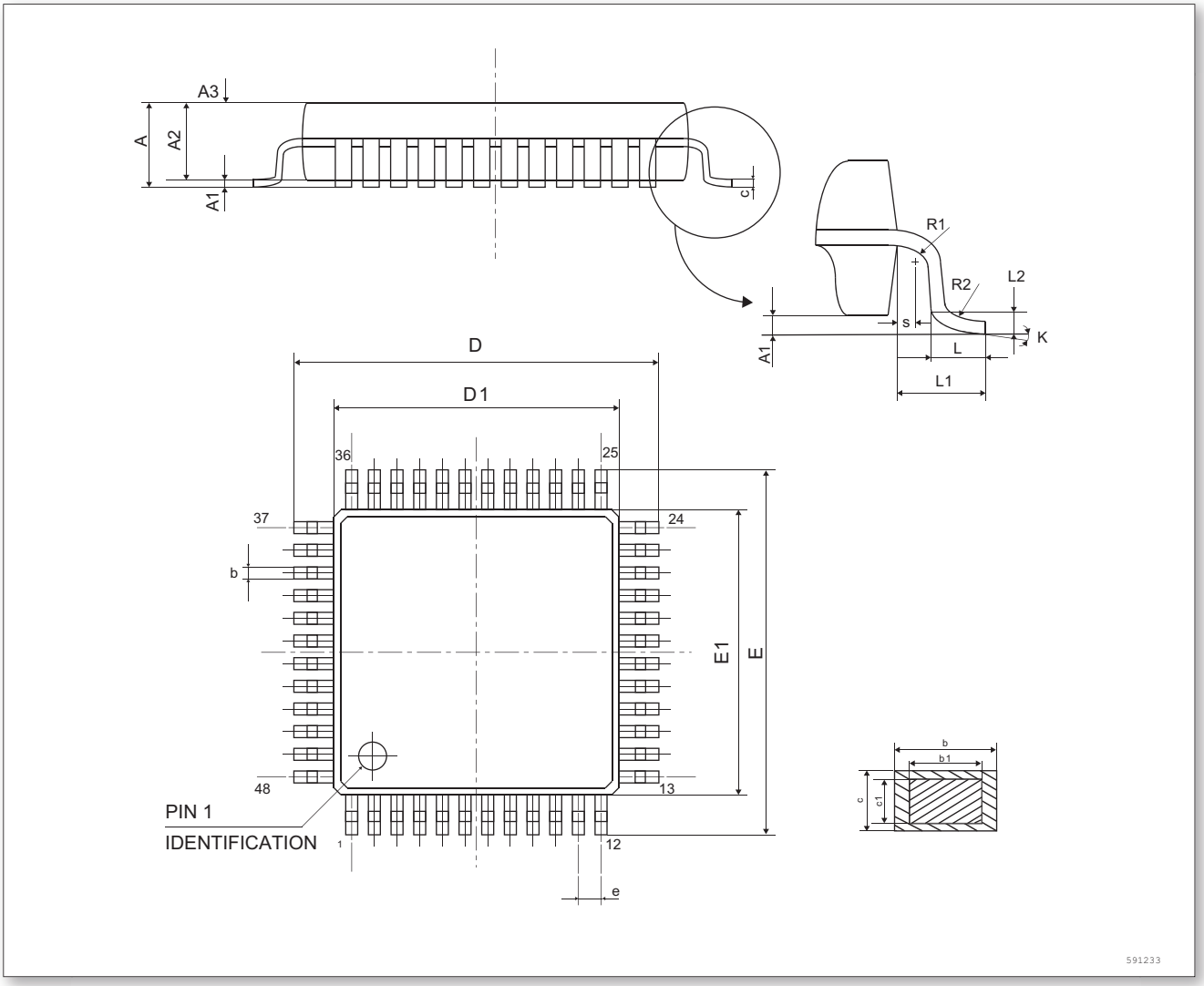

Figure 24. LQFP48 - 48-pin low-profile quad square flat package

1. The drawing is not drawn to scale.
2. Dimensions are in millimeters.

Table 41. LQFP48 size description

Label	MM		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.27
b1	0.17	0.20	0.23
c	0.13		0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50		0.70
L1	1.00REF		
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0°C	3.5°C	7°C
θ 1	11°C	12°C	13°C
θ 2	11°C	12°C	13°C

6.2 LQFP32 Package information

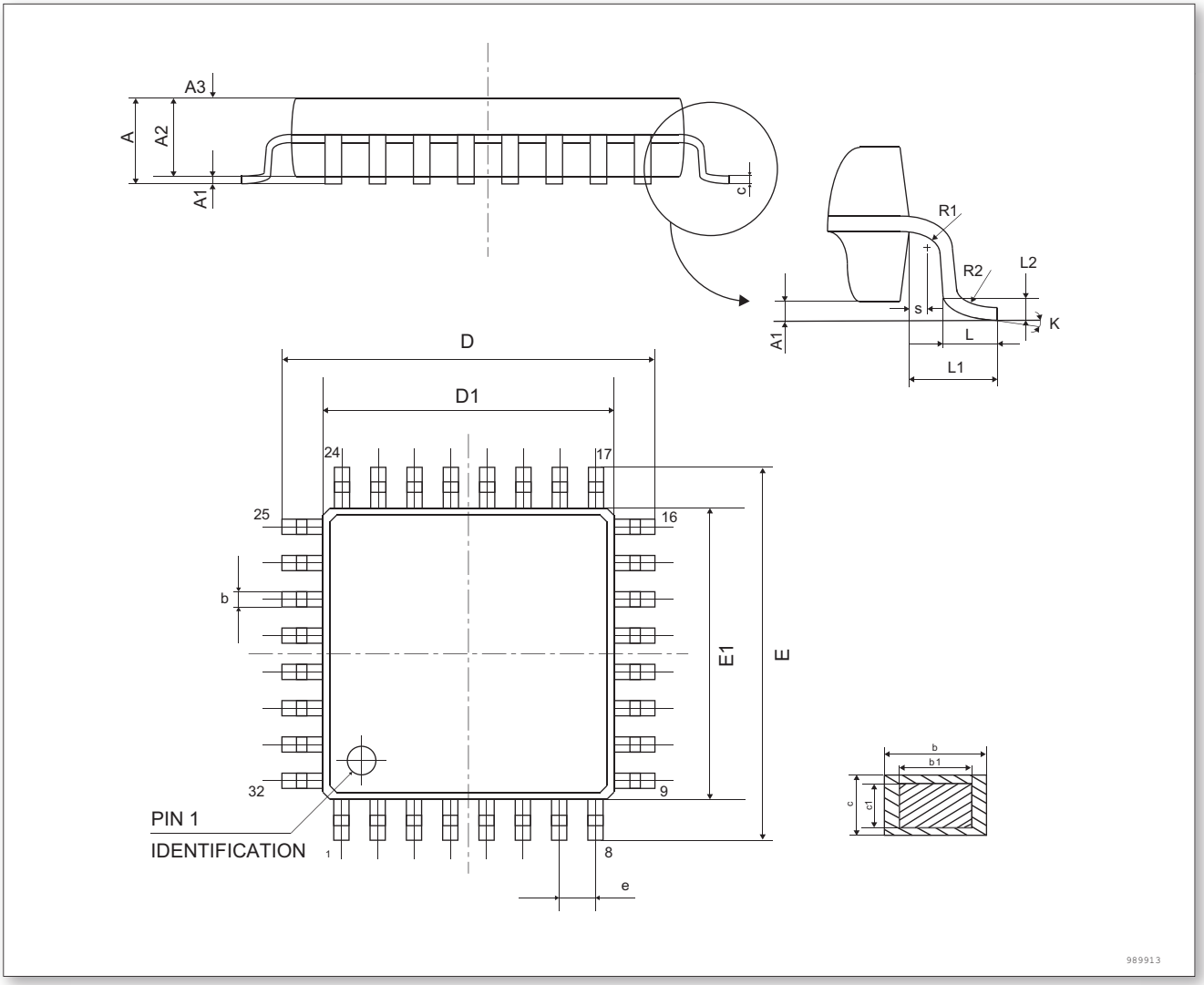

Figure 25. LQFP32 - 32-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 42. LQFP32 size description

Symbol	Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33		0.42
b1	0.32	0.35	0.38
c	0.13		0.18
c1	0.117	0.127	0.137

Symbol	Millimeters		
	Min	Typ	Max
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50		0.70
L1	1.00REF		
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0°C	3.5°C	7°C
θ 1	11°C	12°C	13°C
θ 2	11°C	12°C	13°C

6.3 Packaging QFN32

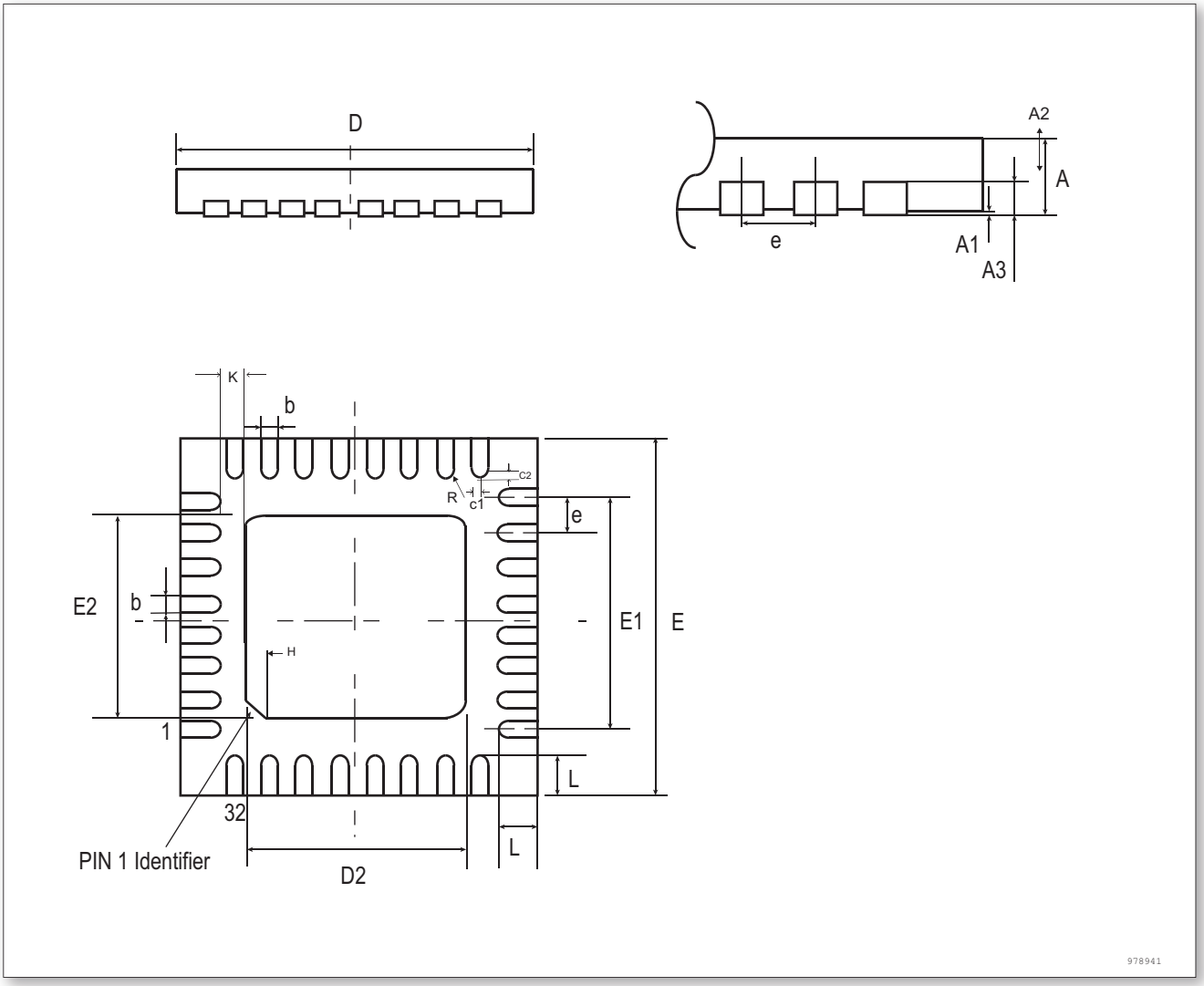

Figure 26. QFN32 - 32-pin quad flat no-leads package outline

1. The drawing is not drawn to scale.
2. Dimensions are in millimeters.

Table 43. QFN32 size description

Label	MM		
	Min	Typ	Max
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60

Label	MM		
	Min	Typ	Max
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09		
c1		0.08	
c2		0.08	
N		Number of pins = 32	

6.4 QFN20 Package information

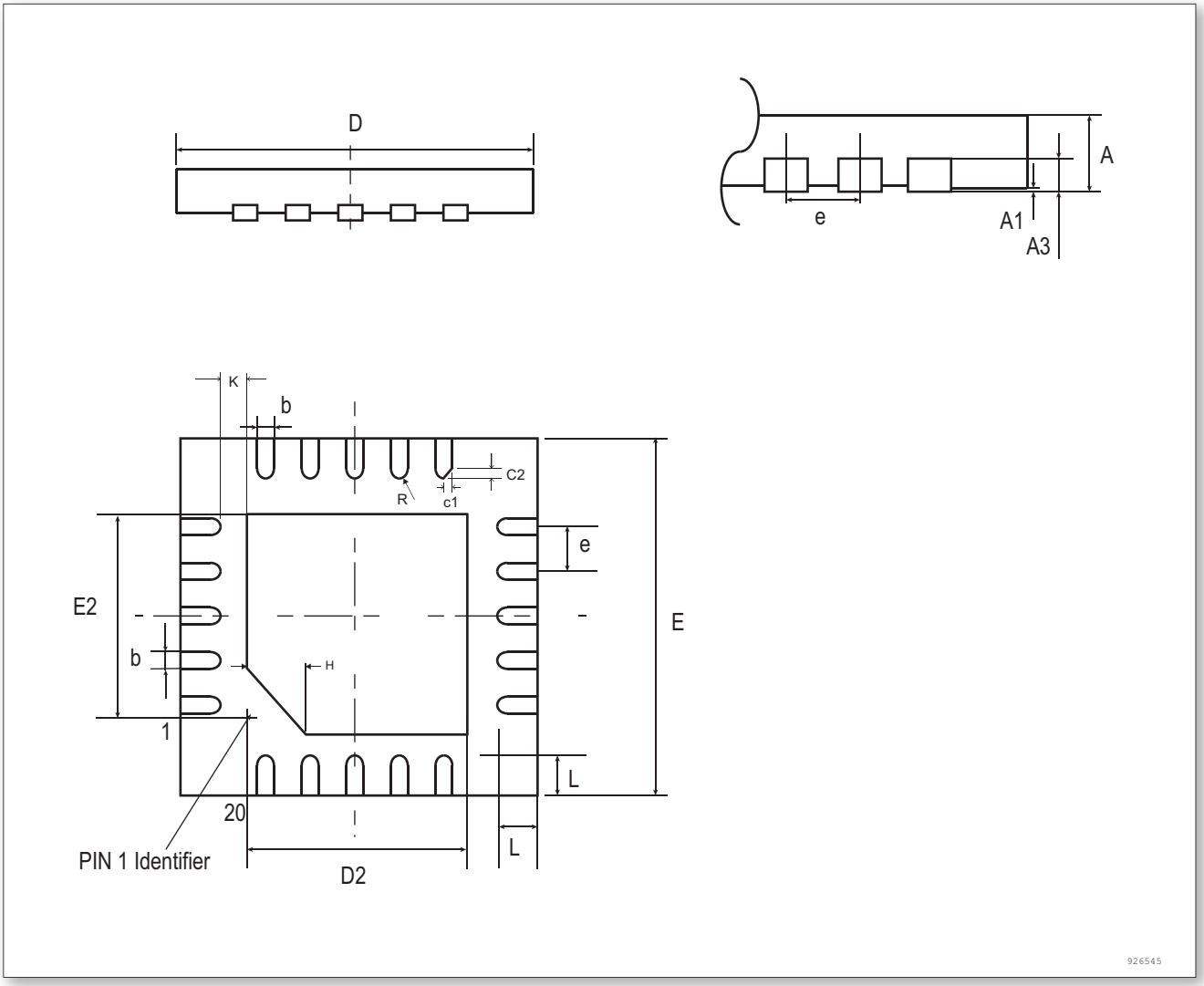

Figure 27. QFN20 - 20-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 44. QFN20 size description

Symbol	Millimeters		
	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60

Symbol	Millimeters		
	Min	Typ	Max
e	0.30	0.40	0.50
H		0.35REF	
K		0.40REF	
L	0.25	0.35	0.45
R	0.075		
N		Number of pins = 20	

6.5 TSSOP20 Package information

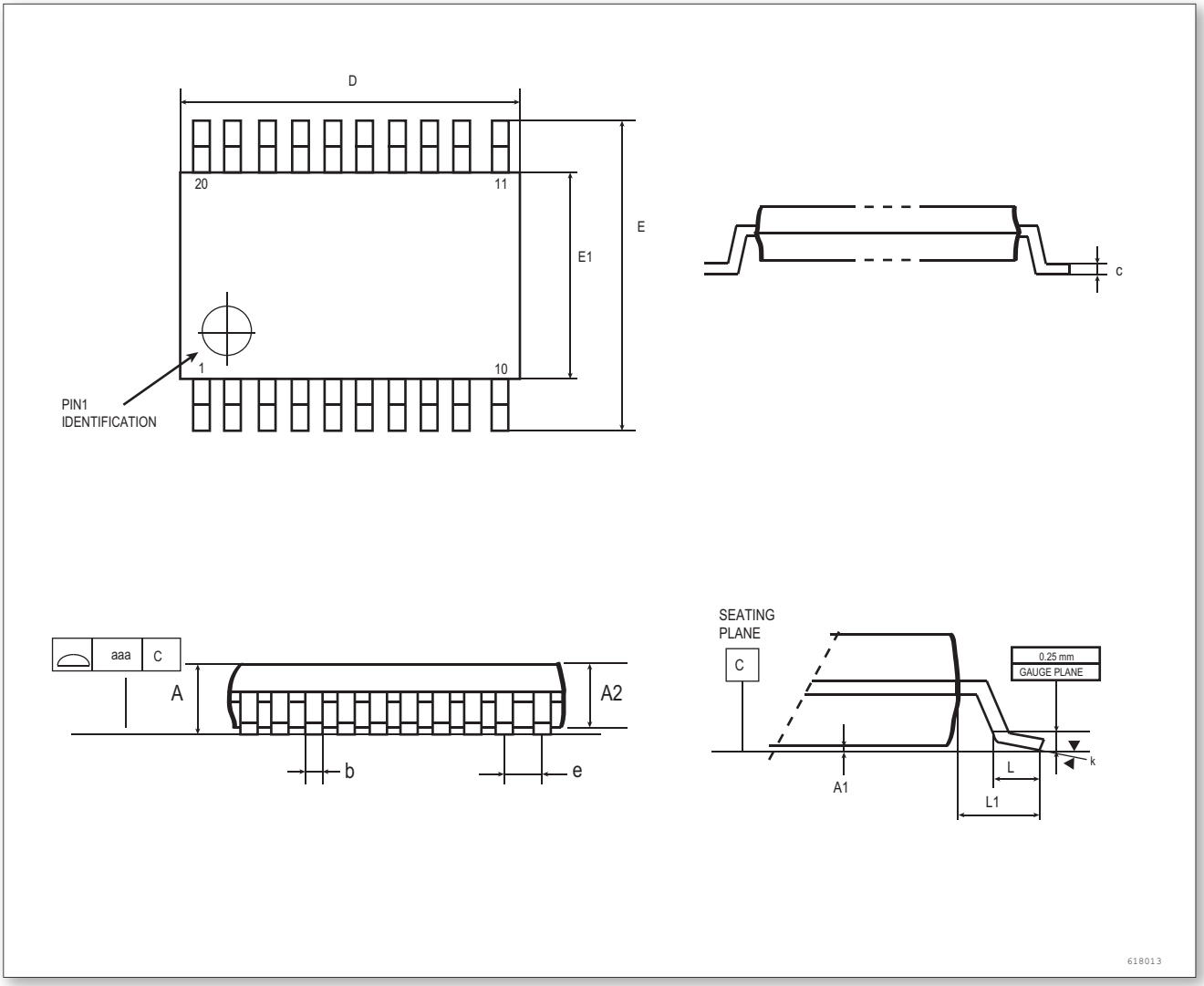

Figure 28. TSSOP20 - 20-lead thin shrink small outline package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 45. TSSOP20 size description

Symbol	Millimeters		
	Min	Typ	Max
A	1.0		1.10
A1	0.05		0.15
A2			0.95
A3	0.39		0.40
b	0.20	0.22	0.24
c	0.10		0.19
c1	0.10		0.15
D	6.40	6.45	6.50

Symbol	Millimeters		
	Min	Typ	Max
E	6.25	6.40	6.55
E1		4.35	4.40
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L2		0.25BSC	
L1		1.0REF	
R	0.09		
θ 1	0°C		8°C

7 Ordering information

Ordering information

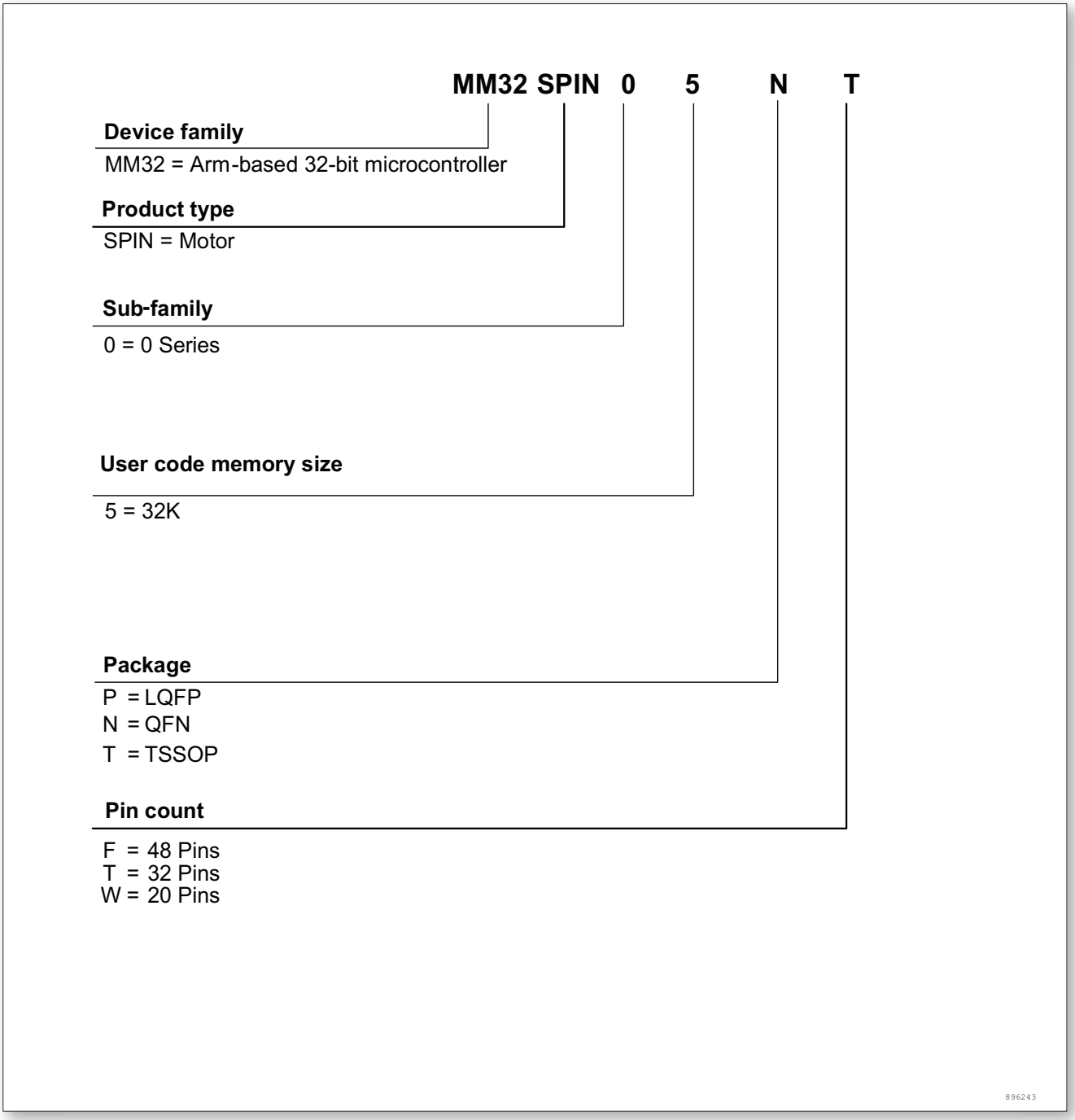

Figure 29. Ordering information scheme

8 Revision history

Revision history

Table 46. Revision history

Date	Version	Changes
2022/08/24	Rev1.23	Update the parameters of operating conditions at power-up/power-down.
2022/06/06	Rev1.22	Update IO parameters; add annoation 1 in table 14; change the NRST figure.
2022/01/21	Rev1.21	Modify the maximum value of the voltage characteristics.
2022/01/12	Rev1.20	Modify P_D and add thermal characteristics.
2021/11/10	Rev1.19	Modify high-speed internal oscillator parameters.
2021/11/10	Rev1.18	Modify temperature characteristics.
2021/09/08	Rev1.17	Modify IO static characteristics.
2020/08/27	Rev1.16	Modify AF parameters in the pin definition.
2020/05/10	Rev1.15	Modify electrical parameters.
2020/04/07	Rev1.14	Modify high-speed internal oscillator parameters.
2020/01/17	Rev1.13	Modify typical current consumption parameters.
2019/07/26	Rev1.12	Modify selection guide.
2019/07/08	Rev1.11	Modify ADC parameters in the selection guide.
2019/05/05	Rev1.10	Modify pin definition.
2019/03/11	Rev1.09	Modify the package parameters.
2019/03/06	Rev1.08	Modify the package parameters.
2019/01/10	Rev1.07	Add the QFN20 package.
2019/01/07	Rev1.06	Modify ADC voltage parameters.
2018/12/14	Rev1.05	Modify ADC descriptions.
2018/11/13	Rev1.04	Modify descriptions.
2018/11/12	Rev1.03	Modify descriptions.
2018/10/11	Rev1.02	Modify electrical parameters.
2018/08/26	Rev1.01	Modify pin definition.
2018/08/04	Rev1.00	Initial release.