



QPL9547

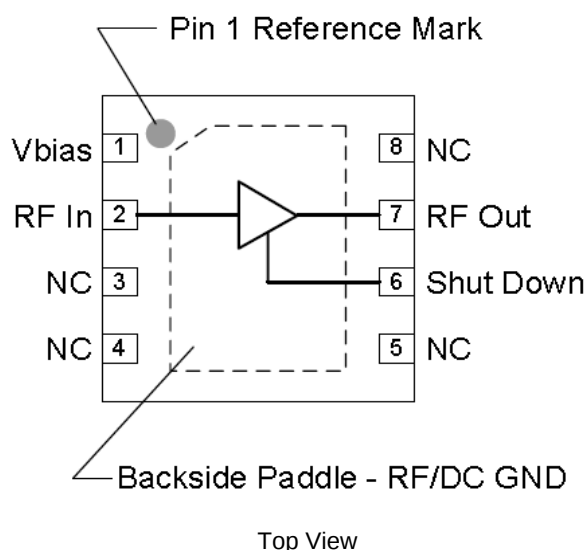
0.1 -6 GHz Ultra Low-Noise LNA

Product Overview

The QPL9547 is a high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 1.9 GHz, the amplifier typically provides 19.5 dB gain, +39 dBm OIP3 at a 65 mA bias setting, and 0.3 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The QPL9547 is bias adjustable and requires minimal external components to operate. It also has a power down control capability integrated into the die for TDD applications.

Functional Block Diagram



8 Pin 2X2 mm DFN Package

Key Features

- 0.1-6 GHz Operational Bandwidth
- Ultra low noise figure, 0.3 dB NF @ 1.9 GHz
- 39 dBm OIP3
- 19.5 dB small signal gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down mode pin with 1.8V logic
- Maintains OFF state with high Pin drive

Applications

- 5G m-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
QPL9547TR7	2500 pieces on a 7" reel
QPL9547EVB-01	0.6-4.2 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150°C
Supply Voltage (V_{DD})	7 V
RF Input Power, CW, 50Ω, T=25°C	22 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.15	+5	+5.25	V
T_{CASE}	-40		+105	°C
Tj for >10 ⁶ hours MTTF			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		100		6000	MHz
Test Frequency			1900		MHz
Gain		17.5	19.5		dB
Input Return Loss			12.2		dB
Output Return Loss			13.5		dB
Noise Figure ⁽²⁾			0.3	0.5	dB
Output P1dB		+21.0	+22.7		dBm
Output IP3	Pout=+2 dBm/tone, Δf=1 MHz	+35.0	+39.3		dBm
Power Shutdown Control (pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state		65	100	mA
	Off state (Power down)		4.3		mA
Shutdown pin current, I_{SD}	$V_{PD} = 1.8$ V		28		μA
Switching Time (LNA On)	50% DC to 0.5dB of settled power/gain		80		ns
Switching Time (LNA Off)	50% DC to -20dB from LNA On power/gain		80		ns
Thermal Resistance	Channel to case		38.6		°C/W

Notes:

1. Test conditions unless otherwise noted: $V_{DD} = +5.0$ V, Temp = +25 °C, 50 Ω system.
2. Input trace loss de-embedded from NF data.

S-Parameters

Test Conditions: $V_{DD}=+5$ V, $I_{DD}=65$ mA (typ.), $T=+25^{\circ}\text{C}$, unmatched 50 Ω system, calibrated to device leads

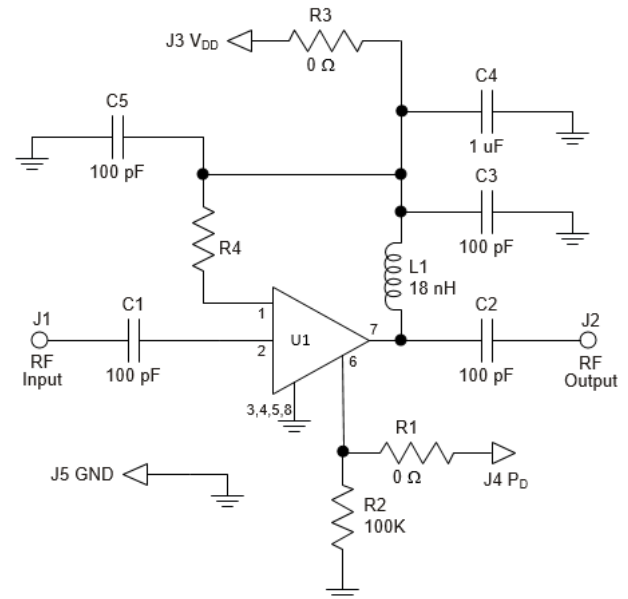
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.7	-7.9	-71	25.8	114	-33.4	32	-10.9	-14
0.9	-9.1	-84	24.5	103	-32.1	34	-10.9	-20
1.1	-10.2	-96	23.3	93	-31.0	35	-11.1	-25
1.3	-11.2	-107	22.2	85	-30.0	35	-11.3	-31
1.5	-12.0	-117	21.2	77	-29.1	34	-11.5	-37
1.7	-12.7	-128	20.3	70	-28.3	32	-11.8	-44
1.9	-13.2	-138	19.5	64	-27.6	30	-12.2	-51
2.1	-13.6	-148	18.8	57	-26.9	27	-12.4	-59
2.3	-13.8	-157	18.1	51	-26.4	25	-12.6	-68
2.5	-14.0	-166	17.5	44	-25.9	22	-12.8	-76
2.6	-14.0	-170	17.2	41	-25.7	20	-12.8	-81
2.7	-14.0	-174	16.9	38	-25.4	19	-12.8	-86
2.9	-13.7	-175	16.4	33	-25.0	16	-13.2	-96
3.1	-13.9	179	15.9	27	-24.6	13	-13.0	-104
3.3	-14.1	174	15.4	21	-24.3	9	-12.7	-112
3.5	-14.4	170	15.0	15	-24.0	6	-12.4	-120
3.7	-14.6	166	14.5	9	-23.7	3	-12.1	-128
3.9	-14.9	162	14.1	4	-23.4	-1	-11.7	-135
4.1	-15.2	158	13.8	-2	-23.2	-4	-11.4	-142
4.3	-15.4	154	13.4	-8	-23.0	-7	-11.1	-149
4.5	-15.6	150	13.0	-14	-22.8	-11	-10.8	-157
4.7	-15.7	146	12.7	-20	-22.6	-15	-10.5	-164
4.9	-15.8	143	12.3	-26	-22.5	-18	-10.2	-172
5.1	-15.8	139	12.0	-32	-22.3	-22	-9.9	179
5.3	-15.7	137	11.6	-38	-22.2	-26	-9.6	171
5.5	-15.6	135	11.2	-45	-22.2	-30	-9.2	163

Noise Parameters

Test Conditions: $V_{DD}=+5$ V, $I_{DD}=65$ mA (typ.), $T=+25^{\circ}\text{C}$, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	NF _{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	Rn (Ω)
0.6	0.16	0.20	12	2.09
0.7	0.15	0.21	17	1.91
0.8	0.17	0.25	27	1.99
0.9	0.23	0.21	23	2.06
1	0.23	0.18	32	2.01
1.1	0.22	0.17	39	1.93
1.2	0.21	0.15	36	1.97
1.3	0.20	0.15	38	2.06
1.4	0.17	0.15	59	2.05
1.6	0.17	0.13	62	1.83
1.7	0.16	0.13	79	1.71
1.8	0.15	0.11	78	1.79
1.9	0.13	0.14	96	1.65
2	0.11	0.13	103	1.70
2.1	0.15	0.11	109	1.66
2.2	0.17	0.12	127	1.58
2.3	0.18	0.13	141	1.50
2.4	0.21	0.10	143	1.67
2.5	0.23	0.13	160	1.65
2.6	0.25	0.15	159	1.51
2.7	0.27	0.14	165	1.59
2.8	0.28	0.18	173	1.42
2.9	0.27	0.18	178	1.50

Evaluation Board – QPL9547EVB-01



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size.
3. For TDD Applications: R1 = 0Ω & R2 = 100K
4. For FDD Applications: R2 = 100K 'OR' Pin 6 tied to ground. R1 = DNP/Omitted
5. A through line is included on the evaluation board to de-embed the board losses.
6. R4 sets the current draw. Can be changed for the desired bias point.

Bill of Material – QPL9547EVB-01

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise QPL9547 LNA	Qorvo	QPL9547
R4	3.32K	Resistor, Chip, 0402, 1%, 1/16W	various	
R2	100K	Resistor, chip, 0402, 1%, 1/10W	various	
R1, R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	18 nH	Inductor, coil, 0402, 2%	Coilcraft	0402CS-18NXGRW
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
C1, C2, C3, C5, C6, C7	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	

Typical Performance – QPL9547EVB-01

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 65\text{ mA}$ (typ.), Temp = $+25^\circ\text{C}$

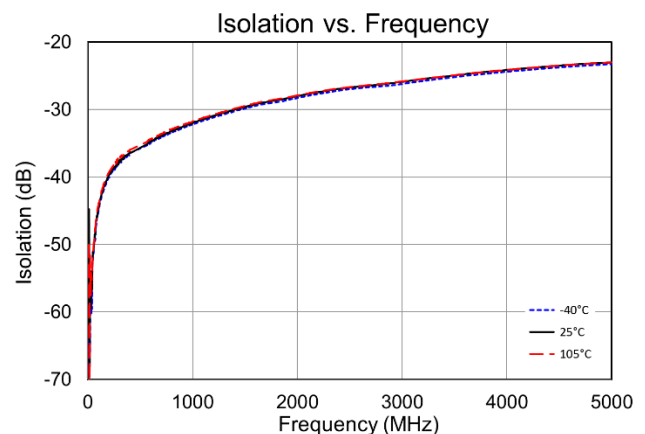
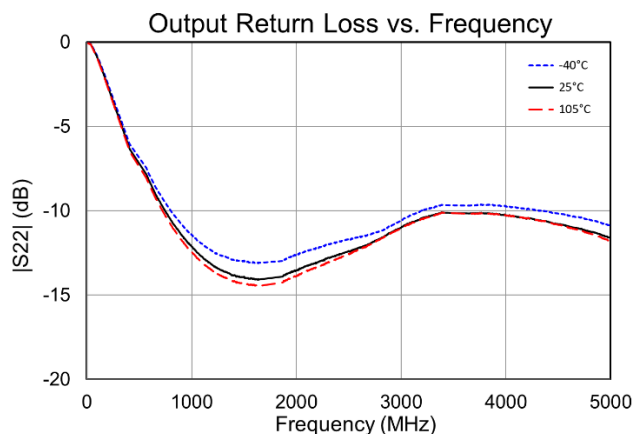
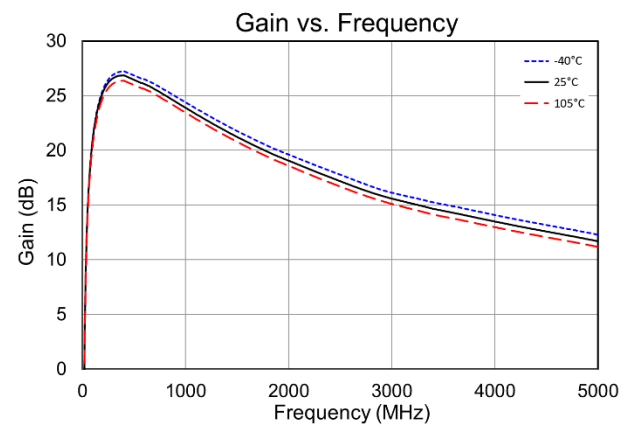
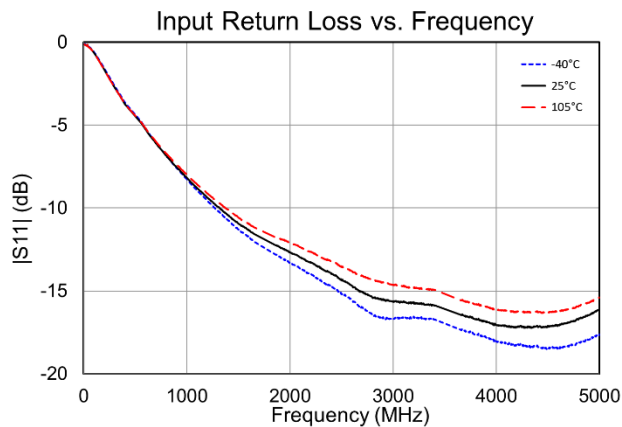
Parameter	Conditions	Typical Values			Units
Frequency		900	1900	2600	MHz
Gain		24.6	19.4	16.8	dB
Input Return Loss		7.3	12.4	14.4	dB
Output Return Loss		11.3	13.8	12.3	dB
Output P1dB		+22	+22.8	+23	dBm
OIP3	$P_{out}=+2\text{ dBm/ tone}$, $\Delta f=1\text{ MHz}$	+38.5	+39.2	+39.2	dBm
Noise figure ⁽¹⁾		0.38	0.30	0.45	dB

Notes:

1. Input trace loss de-embedded from NF data

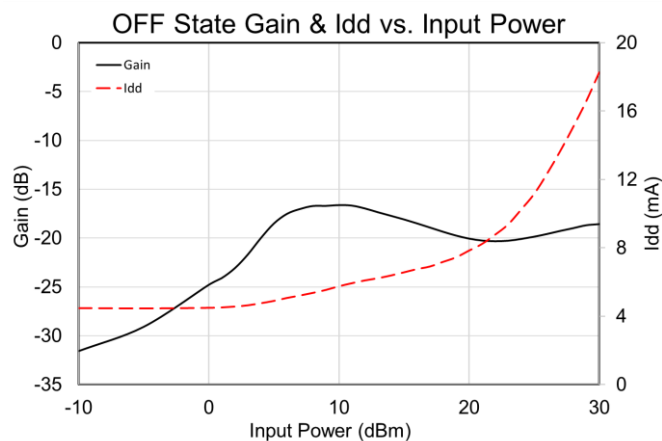
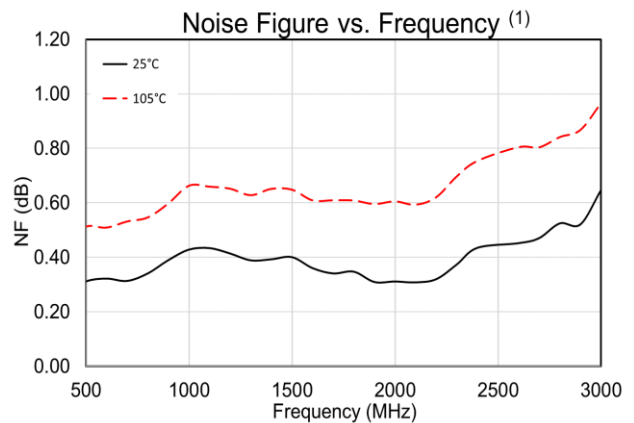
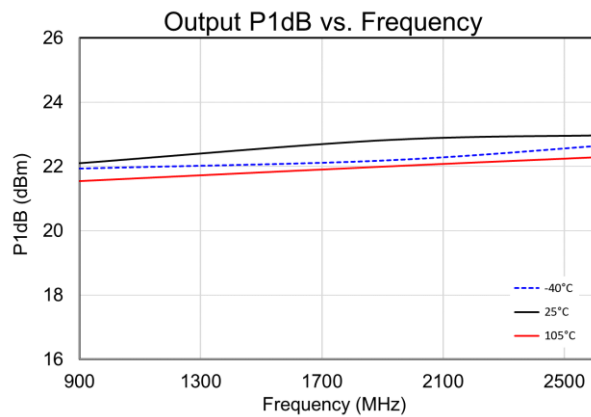
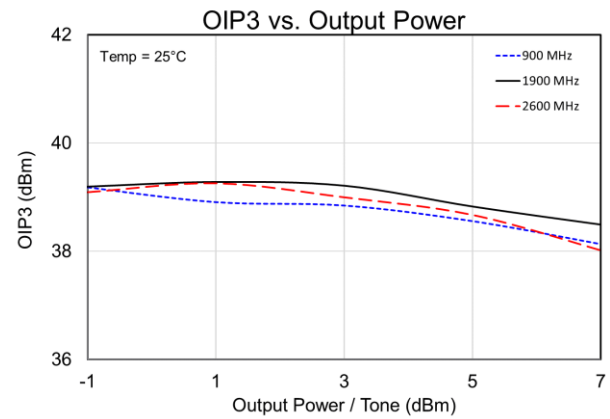
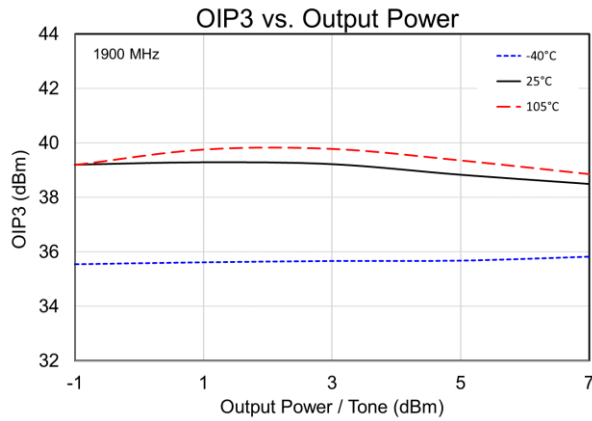
Performance Plots – QPL9547EVB-01

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 65\text{ mA}$.



Performance Plots – QPL9547EVB-01 Continued

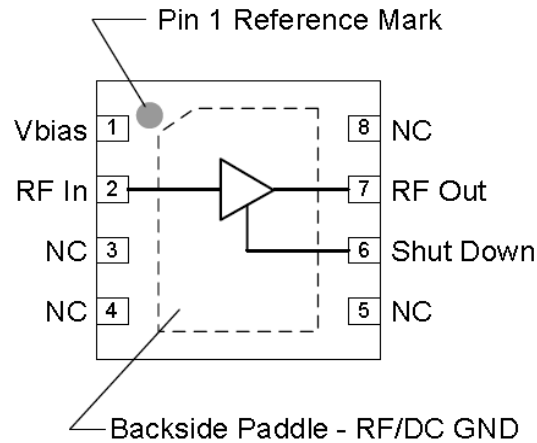
Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 65\text{ mA}$.



Notes:

1. Input trace loss de-embedded from NF. NF at cold temp is better than 0.3 dB causing measurement uncertainties. Therefore, not shown on plot.

Pad Configuration and Description

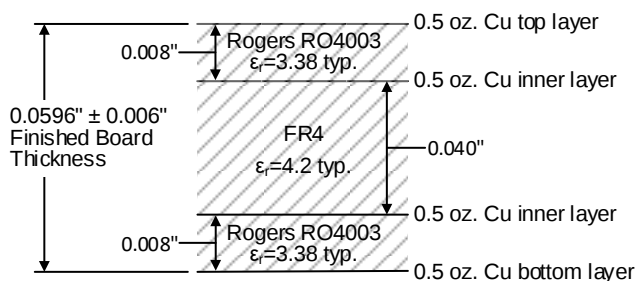


Top View

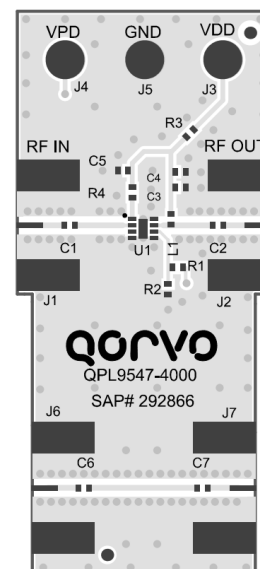
Pad No.	Label	Description
1	V _{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin, internally matched to 50 ohms. A DC block is required.
6	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, internally matched to 50 ohms. A DC block is required. V _{DD} supply pin.
3, 4, 5, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Evaluation Board PCB Information

Qorvo PCB Material and Stack-up



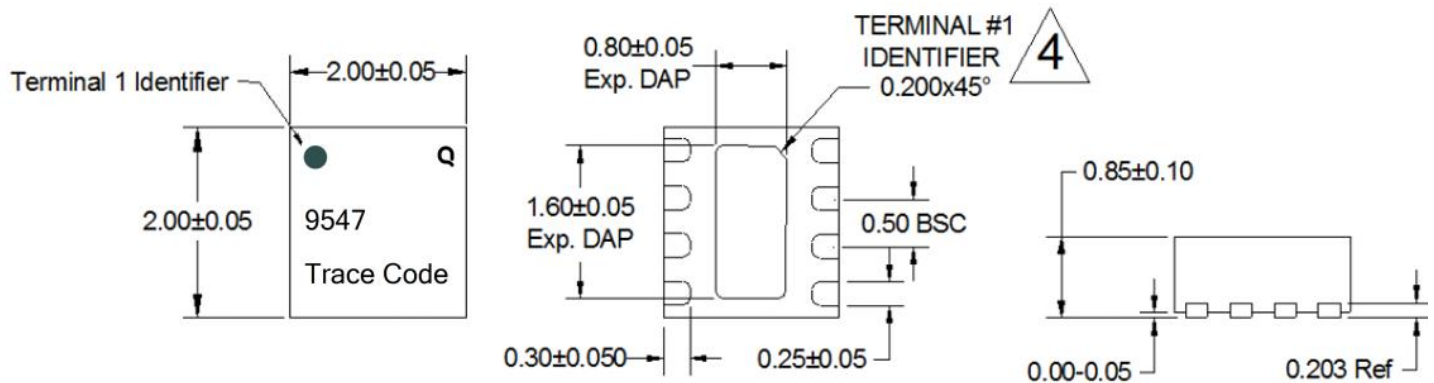
50 ohm line dimensions: width = 0.018", spacing = 0.020"
0.4 mil Solder mask at top and bottom layers



Package Marking and Dimensions

Marking: Part Number – 9547

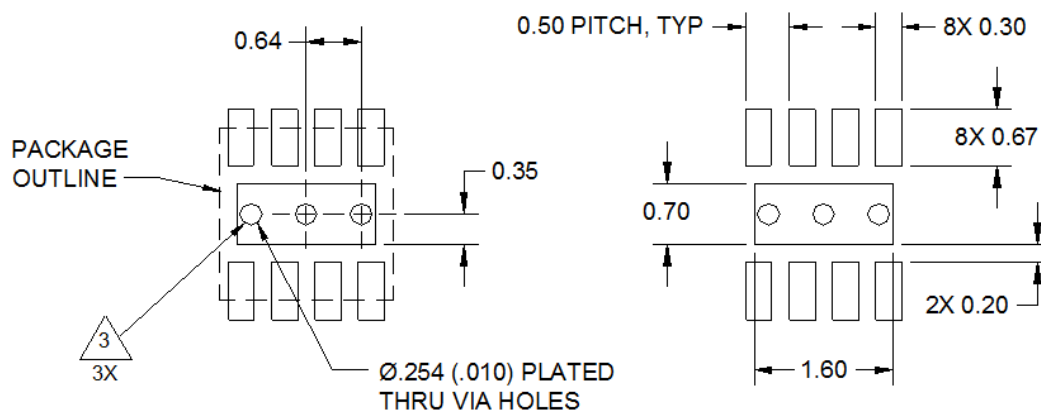
Trace Code – XXXX up to 4 Characters assigned by sub-contractor



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to SPE-000677.
3. Contact plating: NiPdAu

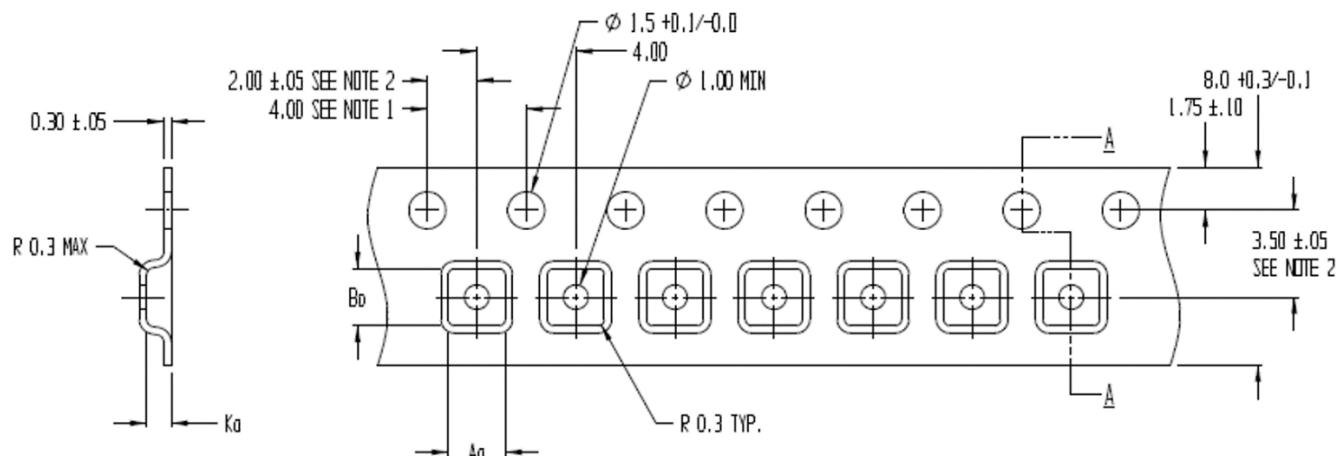
Recommended PCB Layout Pattern



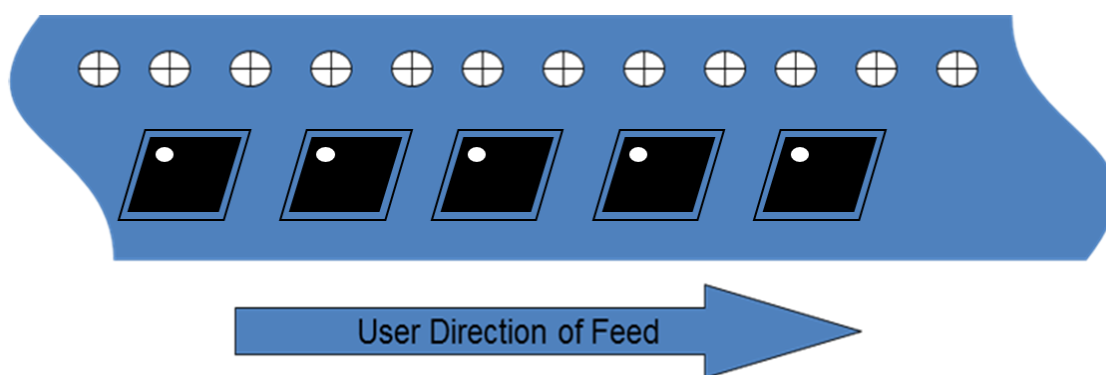
Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

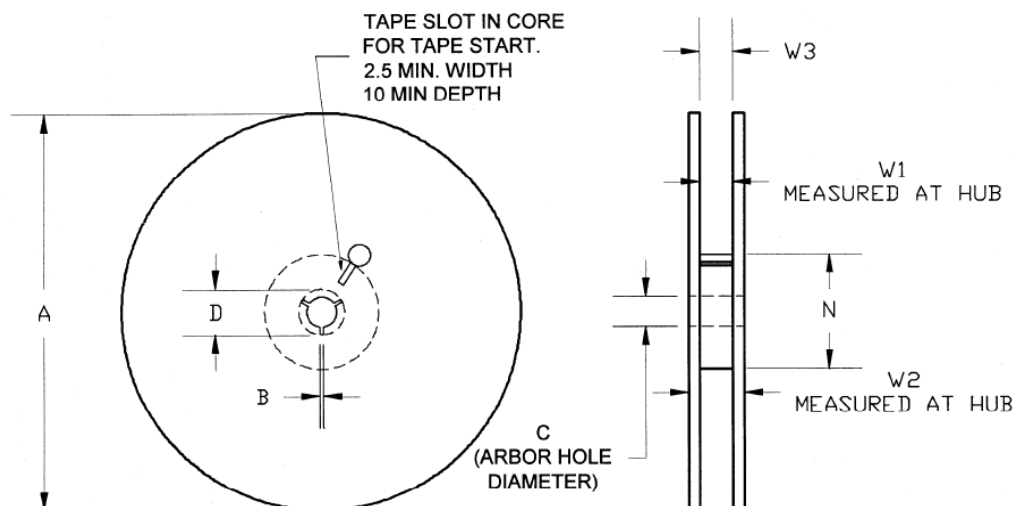


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



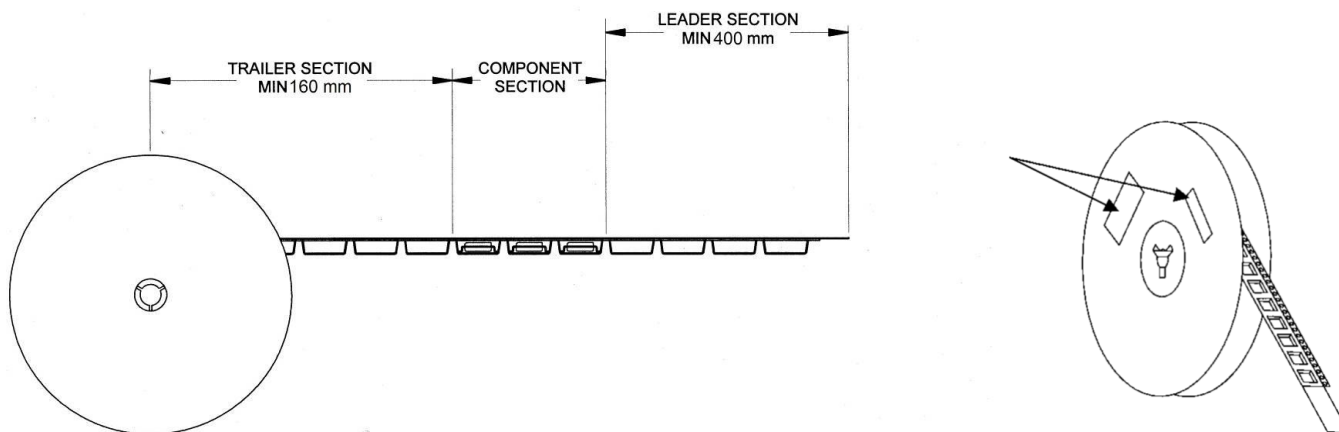
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020E



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Thickness: Ni 0.508 ~ 1.524 μm ; Pd 0.023 ~ 0.1016 μm ; Au 0.00254 ~ 0.01016 μm*)

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($\text{C}_{15}\text{H}_{12}\text{Br}_4\text{O}_2$) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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