WNMD2055

Dual N-Channel, 20V, 18A, Power MOSFET

Http://www.sh-willsemi.com

V_{DS} (V)	Max $R_{DS(on)}$ (mΩ)
20	8.2 @ VGS=4.5V
	8.5 @ VGS=3.7V
	10.0 @ VGS=3.1V
	12.0 @ VGS=2.5V
ESD Rating：2000V HBM	

Descriptions

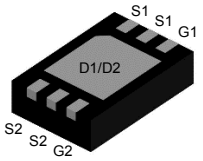
The WNMD2055 is Dual N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNMD2055 is Pb-free.

Features

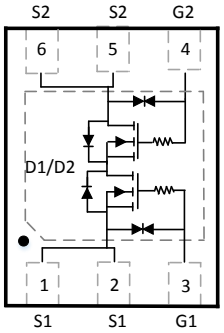
- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Small package DFN2X3-6L

Applications

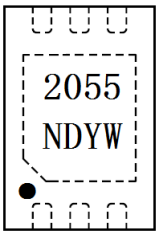
- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device



DFN2X3-6L



Pin configuration (Top view)



2055 = Device Code
ND = Special Code
Y = Year
W = Week (A~Z)

Marking

Order information

Device	Package	Shipping
WNMD2055-6/TR	DFN2X3-6L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current [d]	T_C=25°C	I_D	18	A
	T_C=100°C		18	A
Pulsed Drain Current [c]		I_{DM}	72	A
Continuous Drain Current	T_A=25°C	I_{DSM}	17	A
	T_A=70°C		14	
Avalanche Energy L=0.3mH		E_{AS}	60	mJ
Power Dissipation [b]	T_C=25°C	P_D	20	W
	T_C=100°C		8	
Power Dissipation [a]	T_A=25°C	P_{DSM}	3.7	W
	T_A=70°C		2.4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	27	34	°C/W
	Steady State		54	68	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	5.0	6.1	

Note:

a The value of $R_{\theta JA}$ is measured with the device mounted on 1-inch^2 (6.45cm^2) with 2oz.(0.071mm thick) Copper pad on a 1.5*1.5 inch^2, 0.06-inch thick FR4 PCB, in a still air environment with T_A =25°C. The power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value in any given application is determined by the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

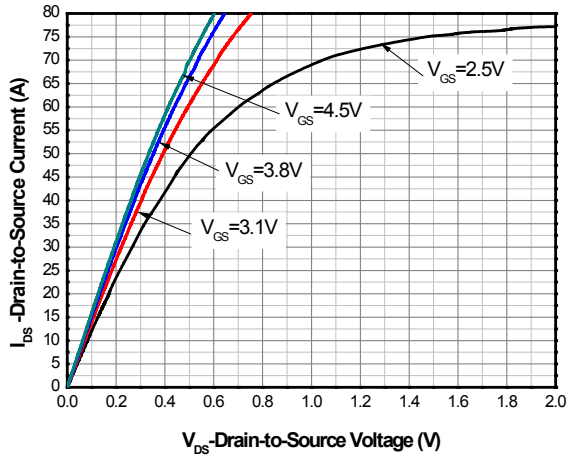
d The maximum current rating by source bonding technology.

e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

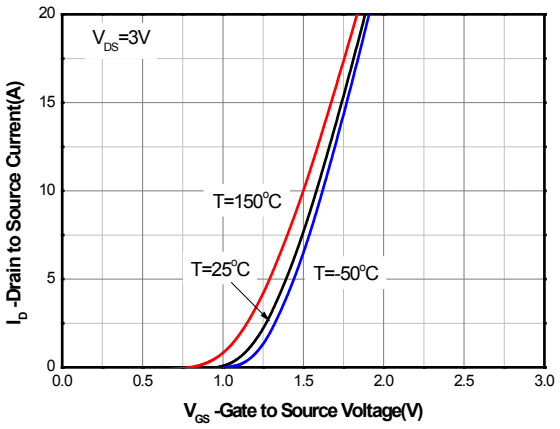
Electronics Characteristics (Ta=25ºC, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =16V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12V			±10	uA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	0.45	0.7	1.0	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 10A	5.0	6.4	8.2	mΩ
		V_{GS} = 3.7V, I_D = 7A	5.5	6.8	8.5	
		V_{GS} = 3.1V, I_D = 5A	6.0	7.3	10.0	
		V_{GS} = 2.5V, I_D = 4A	6.5	8.3	12.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0KHz, V_{DS} = 10 V		1600		pF
Output Capacitance	C_{OSS}			226		
Reverse Transfer Capacitance	C_{RSS}			211		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D =10 A		18.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	Q_{GS}			2.7		
Gate-to-Drain Charge	Q_{GD}			5.6		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D =10 A, R_G=2Ω		0.9		us
Rise Time	tr			3.1		
Turn-Off Delay Time	td(OFF)			7.8		
Fall Time	tf			6.5		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.75	1	V

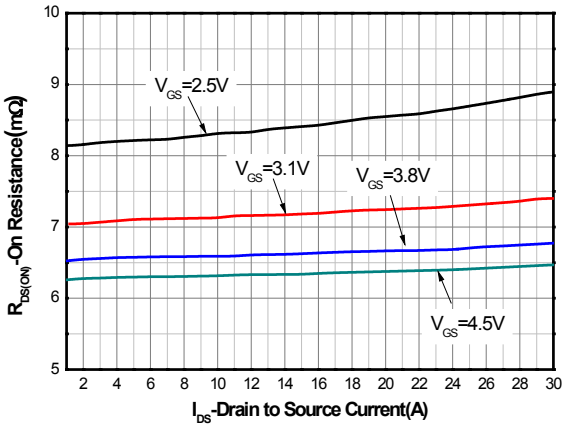
Typical Characteristics (Ta=25°C, unless otherwise noted)



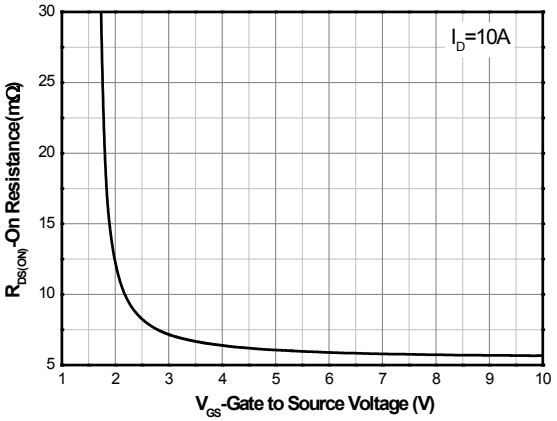
Output Characteristics [e]



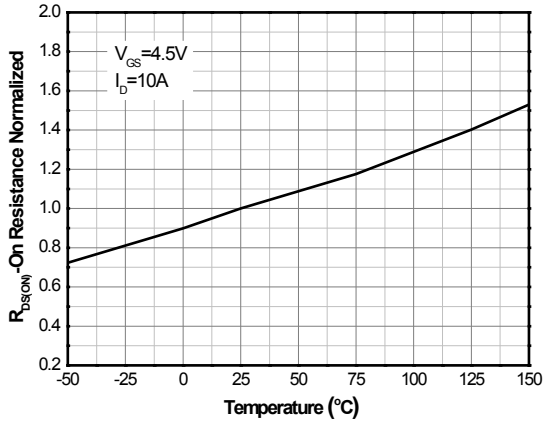
Transfer Characteristics [e]



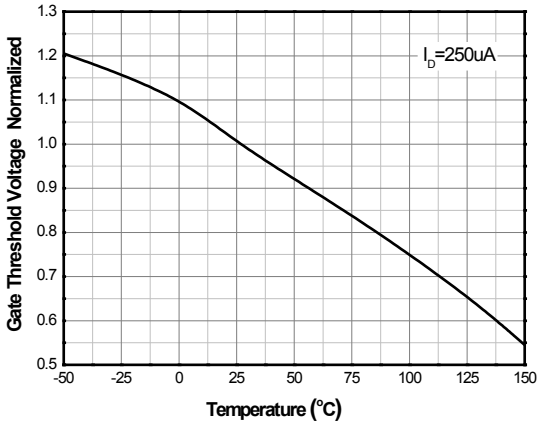
On-Resistance vs. Drain Current [e]



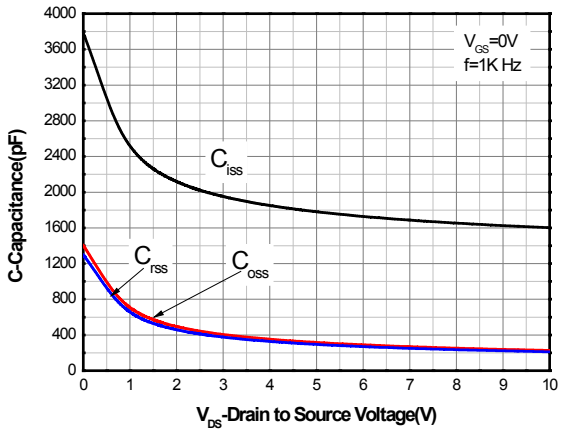
On-Resistance vs. Gate-to-Source Voltage [e]



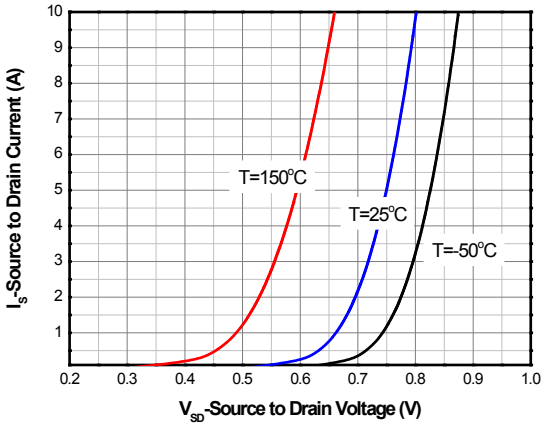
On-Resistance vs. Junction Temperature [e]



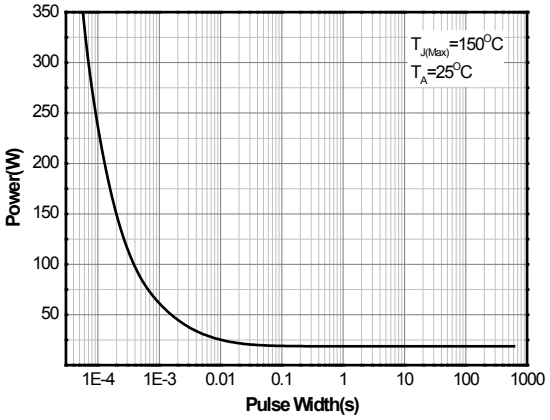
Threshold Voltage vs. Temperature



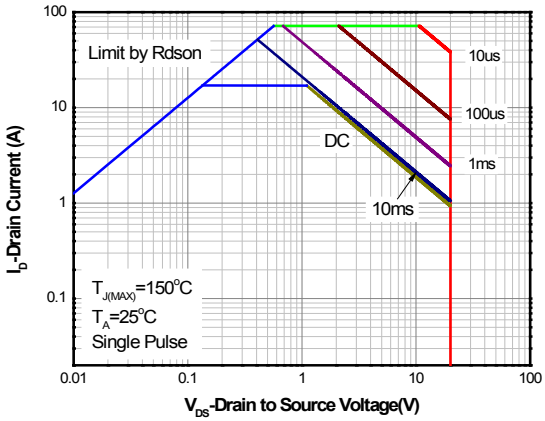
Capacitance



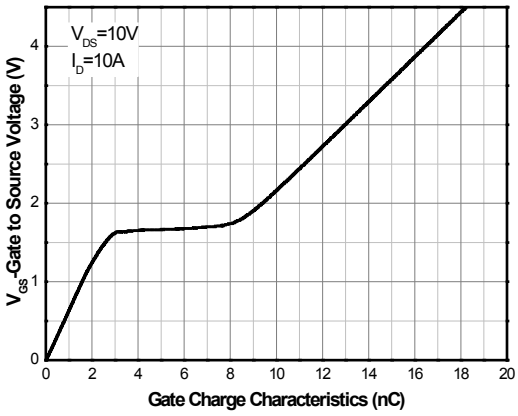
Body Diode Forward Voltage [e]



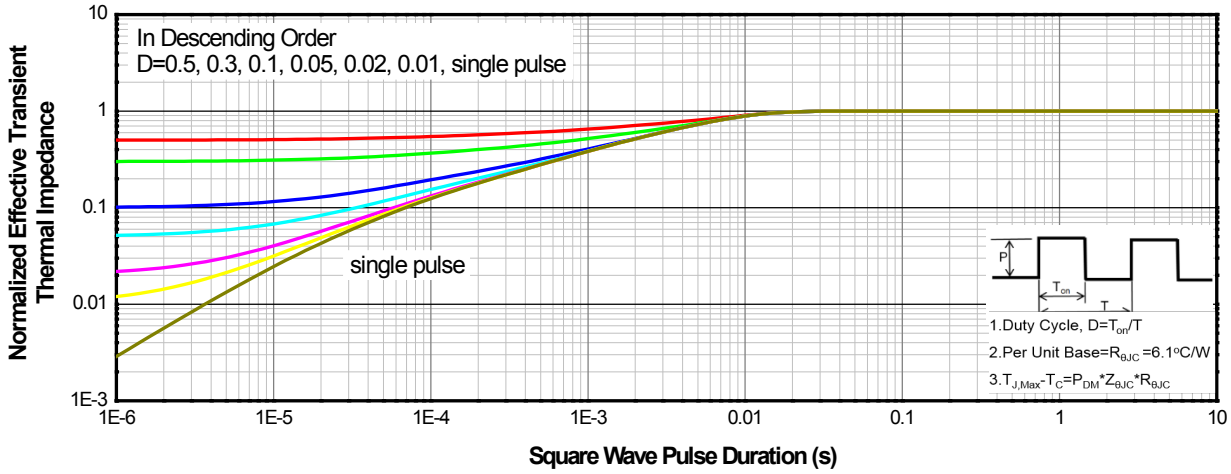
Single Pulse power



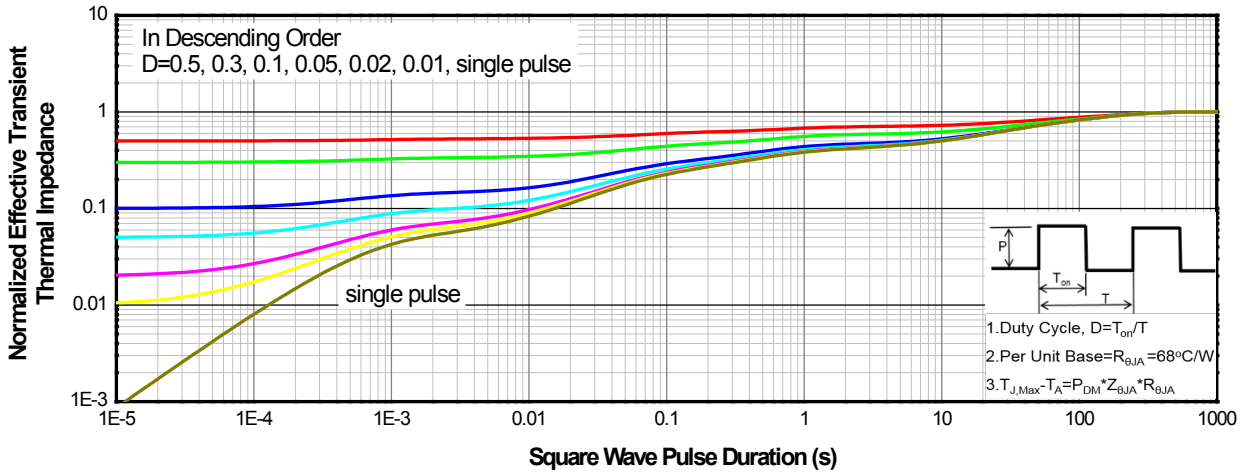
Safe Operating Power



Gate Charge Characteristics



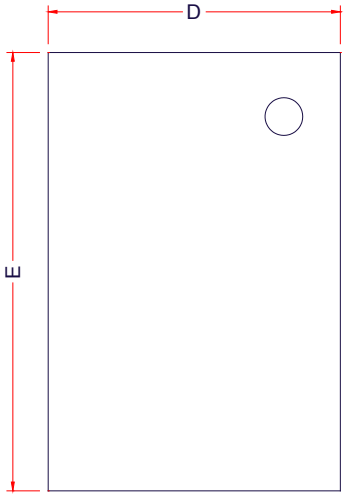
Transient Thermal Response (Junction-to-Case)



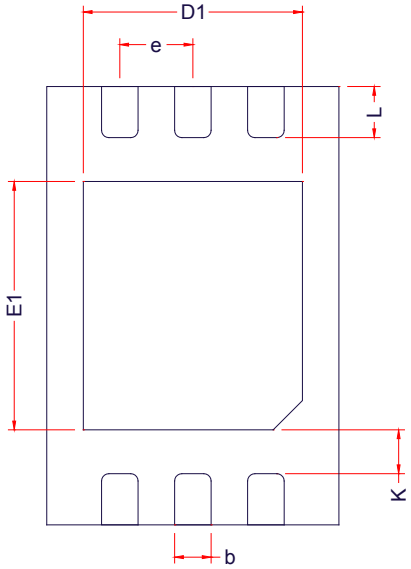
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

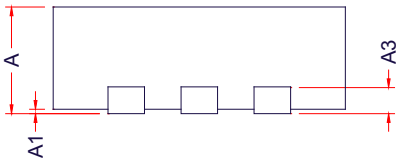
DFN2x3-6L



TOP VIEW



BOTTOM VIEW

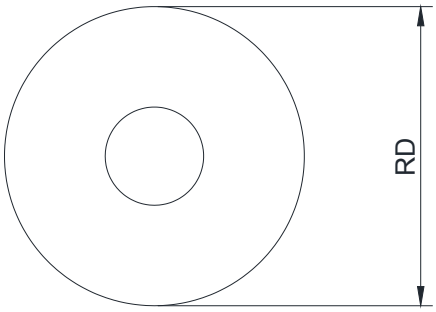


SIDE VIEW

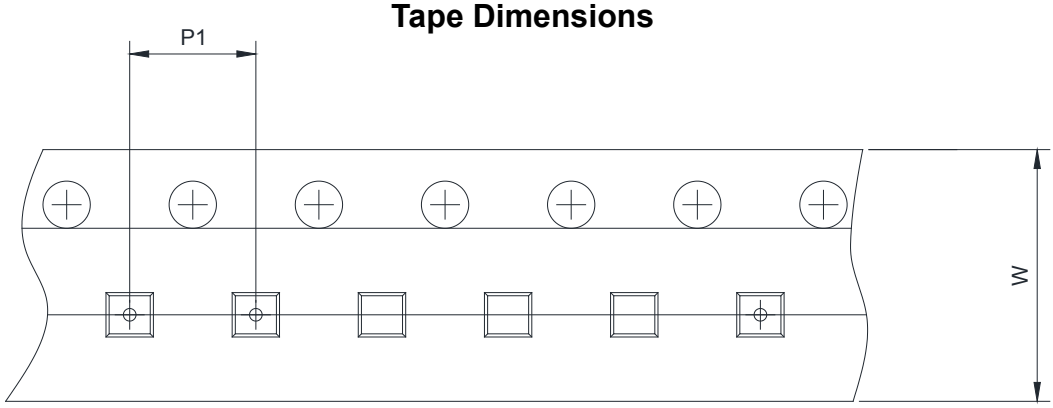
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20Ref.	
D	1.95	2.00	2.05
E	2.95	3.00	3.05
D1	1.45	1.50	1.55
E1	1.65	1.70	1.75
K	0.20	-	-
b	0.20	0.25	0.30
e		0.50BSC	
L	0.30	0.35	0.40

TAPE AND REEL INFORMATION

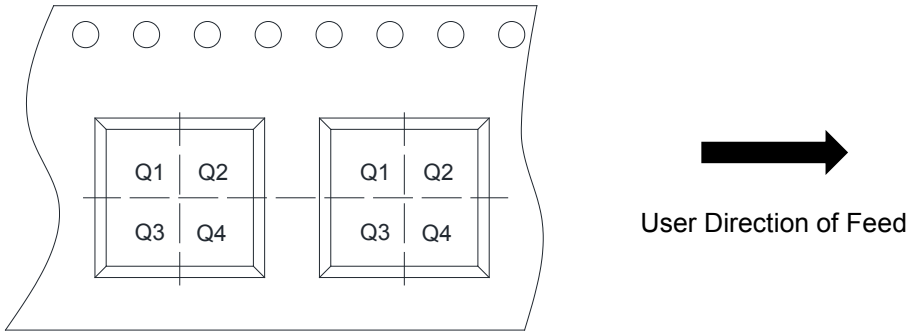
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4