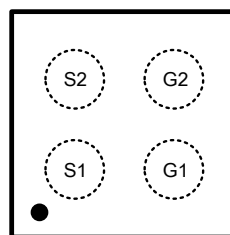
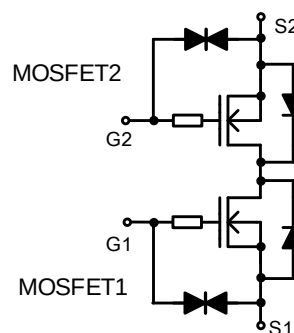
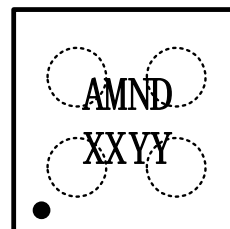


WNMD2202
Dual N-Channel, 12V, 5.6A, Power MOSFET
<https://www.omnivision-group.com>

V _{SSS} (V)	Max R _{SS(on)} (mΩ)
12	15.0 @ V _{GS} =4.5V
	17.5 @ V _{GS} =3.8V
	20.0 @ V _{GS} =3.1V
	27.0 @ V _{GS} =2.5V
ESD Rating:2000V HBM	


CSP-4L (Top view)
Descriptions

The WNMD2202 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent R_{SS(ON)} with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2202 is available in CSP-4L package. Standard Product WNMD2202 is Pb-free and Halogen-free.


Pin Configuration


A = Device Code

M = Month

ND = Week

XXYY= Coordinate

Marking
Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-4L

Applications

- Lithium-Ion battery protection circuit

Order information

Device	Package	Shipping
WNMD2202-4/TR	CSP-4L	3000/Reel&Tape

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Source -Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Source Current	$T_A=25^{\circ}\text{C}$	I_S^a	5.6
		I_S^b	9.5
Pulsed Source Current ^{ac}	I_{SM}	49	A
Maximum Power Dissipation	$T_A=25^{\circ}\text{C}$	P_D^a	0.56
		P_D^b	1.62
Operating Junction Temperature	T_J	-55 to 150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^{\circ}\text{C}$

Thermal resistance ratings

Single Operation				
Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}^a$	150	225	$^{\circ}\text{C/W}$
	$R_{\theta JA}^b$	67	77	

Note:

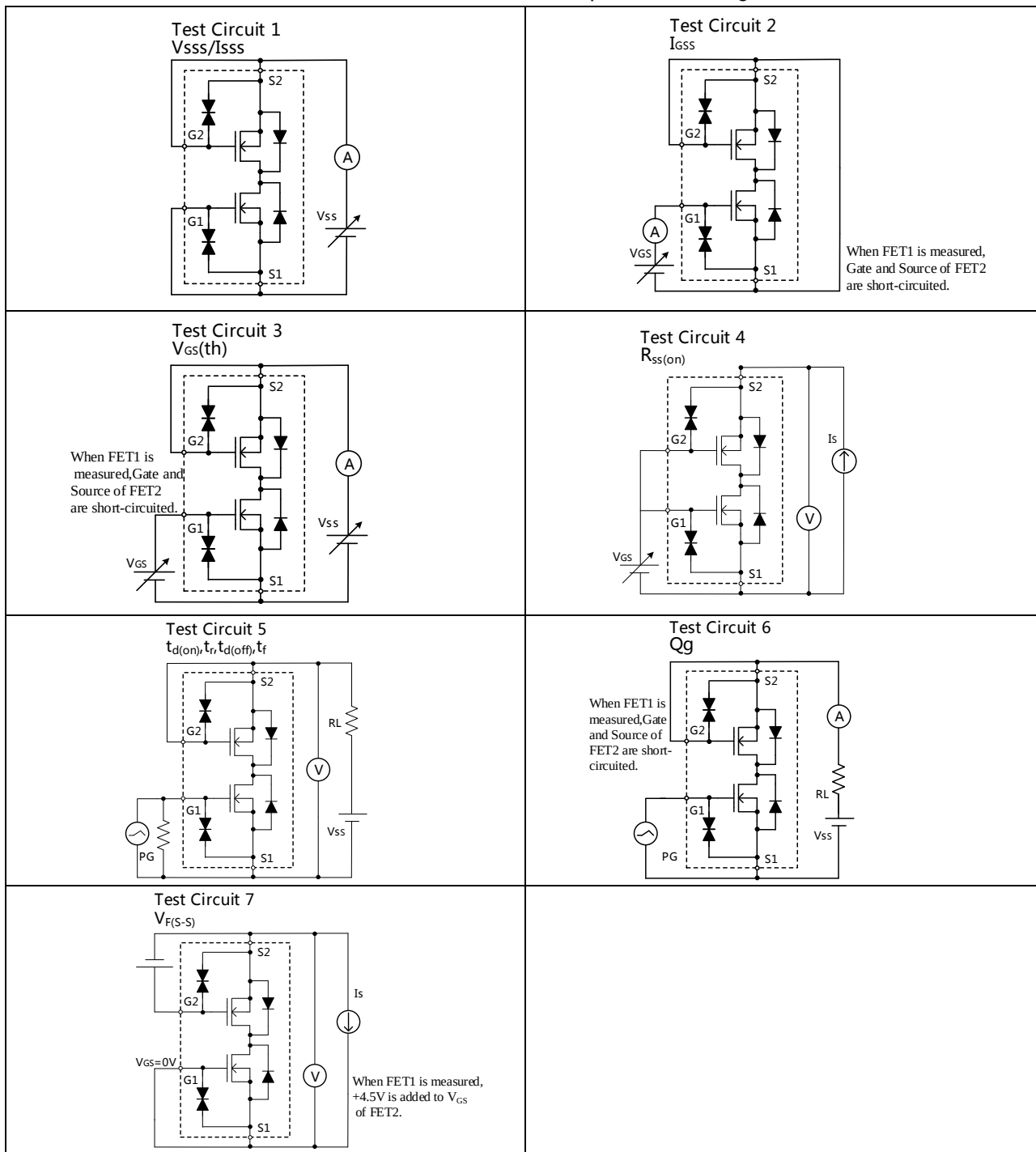
- FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) minimum pad covered with copper.
- Ceramic substrate (70 mm X 70 mm X t1.0 mm, 70um Copper) fully covered with copper.
- Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J=25^{\circ}\text{C}$, the maximum allowed junction temperature of 150°C .
- The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

Electronics Characteristics (T_A=25°C, unless otherwise noted)

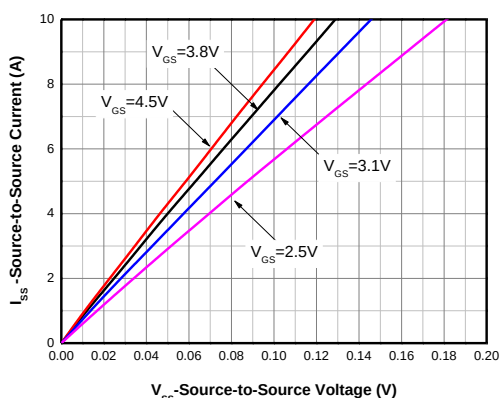
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V _{SSS}	V _{GS} = 0 V, I _S = 1mA	12			V
Zero Gate Voltage Drain Current	I _{SSS}	V _{SS} =12 V, V _{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I _{GSS}	V _{SS} = 0 V, V _{GS} = ±8V TEST CIRCUIT 2			±10	uA
		V _{SS} = 0 V, V _{GS} = ±5V TEST CIRCUIT 2			±1	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	V _{GS(th)}	V _{SS} = 10 V, I _S = 1mA TEST CIRCUIT 3	0.5	0.9	1.3	V
Source to Source On-state Resistance	R _{SS(on)}	V _{GS} = 4.5V, I _S = 3.0A TEST CIRCUIT 4	9.0	12.0	15.0	mΩ
		V _{GS} = 3.8V, I _S = 3.0A TEST CIRCUIT 4	9.5	13.0	17.5	
		V _{GS} = 3.1V, I _S = 3.0A TEST CIRCUIT 4	10.5	14.5	20.0	
		V _{GS} = 2.5V, I _S = 3.0A TEST CIRCUIT 4	11.5	17.5	27.0	
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	V _{F(S-S)}	V _{GS} = 0 V, I _F = 3.0A TEST CIRCUIT 7	0.5	0.75	1.2	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V _{GS} = 4.5V, V _{SS} =10V, I _S =3.0A, TEST CIRCUIT 5		0.3		us
Rise Time	tr			1.2		
Turn-Off Delay Time	td(OFF)			2.7		
Fall Time	tf			2.6		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1kHz, V _{SS} = 10 V		660		pF
Output Capacitance	C _{OSS}			170		
Reverse Transfer Capacitance	C _{RSS}			140		
Total Gate Charge	Q _{G(TOT)}	V _{G1S1} = 4.5 V, V _{SS} =10V, I _S =6.0A TEST CIRCUIT 6		9.5		nC
Gate-to-Source Charge	Q _{GS}			1.6		
Gate-to-Drain Charge	Q _{GD}			3.2		

Test Circuit

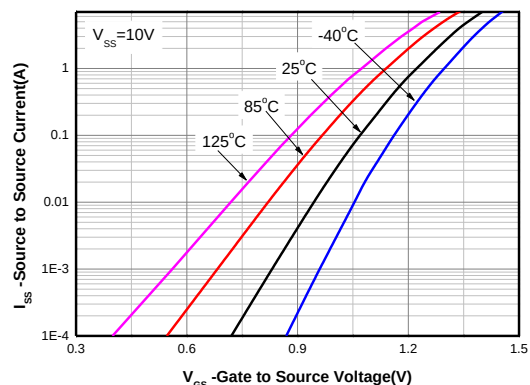
FET1 and the FET2 are both measured. Test circuits are example of measuring the FET1 side



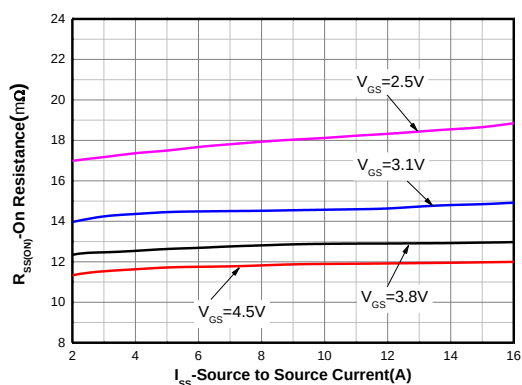
Typical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)



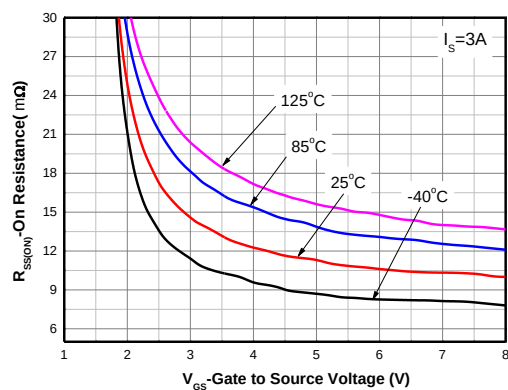
Output Characteristics ^d



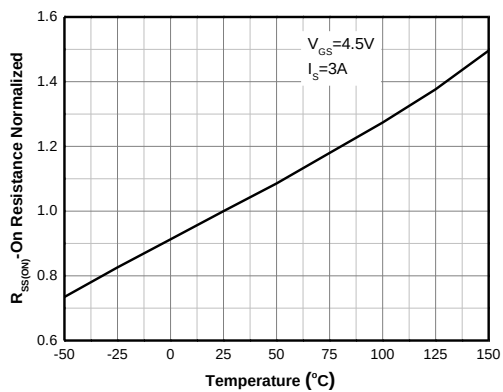
Transfer Characteristics ^d



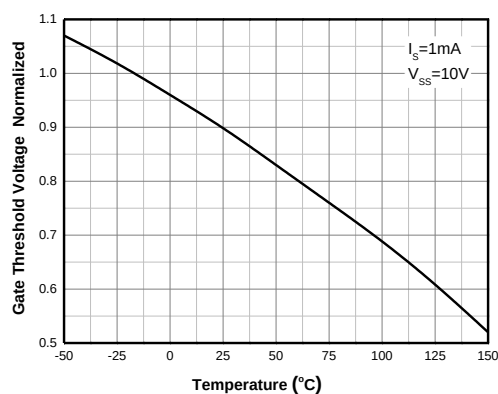
On-Resistance vs. Source Current ^d



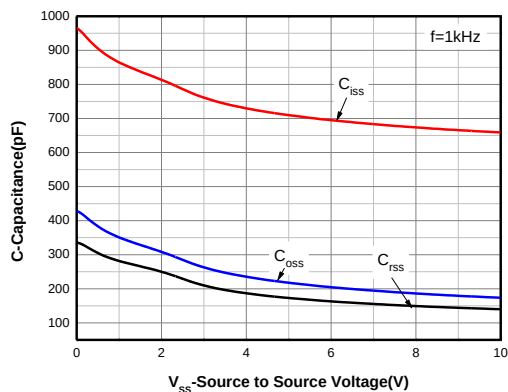
On-Resistance vs. Gate-to-Source Voltage ^d



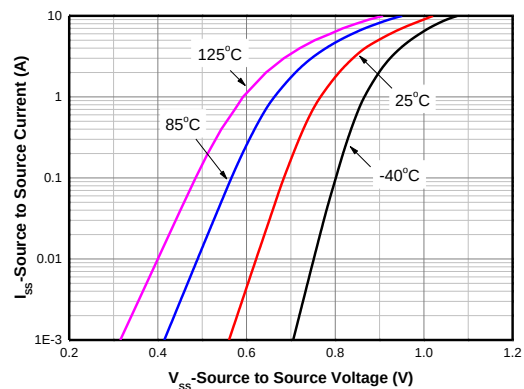
On-Resistance vs. Junction Temperature ^d



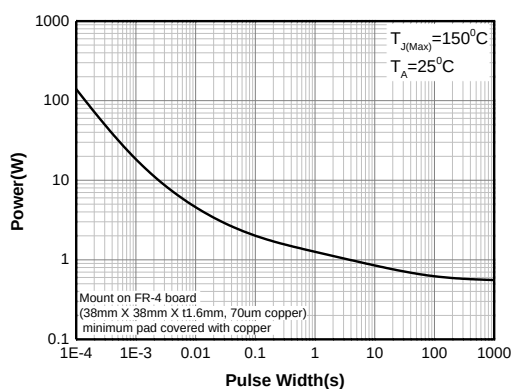
Threshold Voltage vs. Temperature



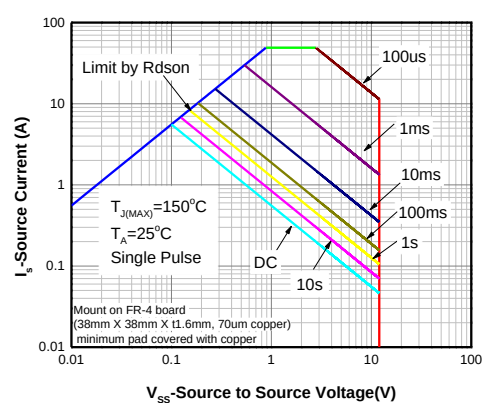
Capacitance



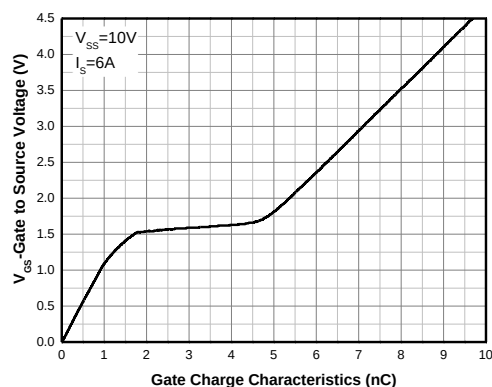
Body Diode Forward Voltage^d



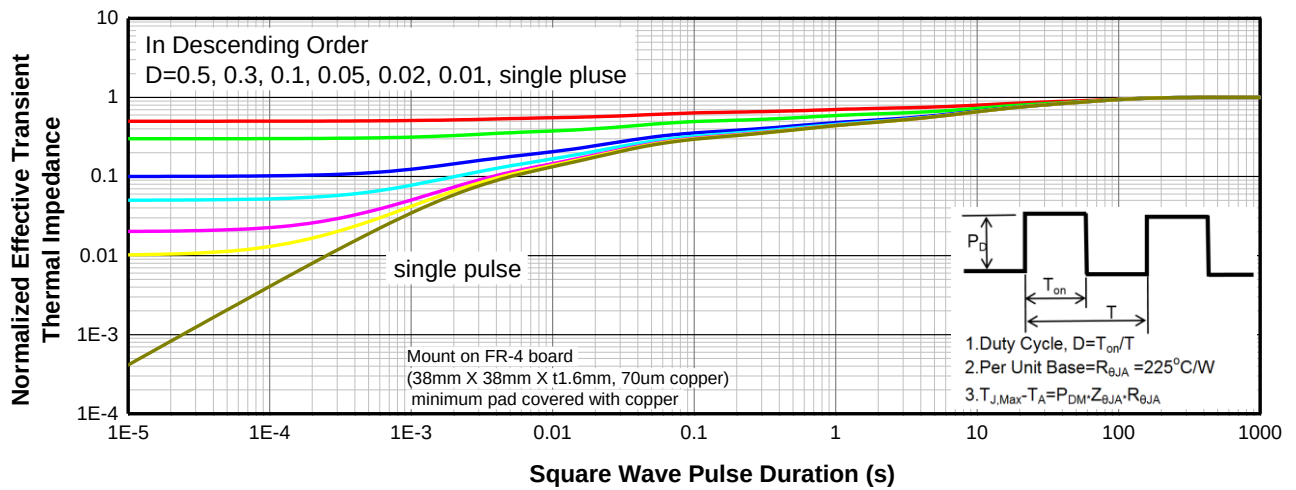
Single Pulse power



Safe Operating Power



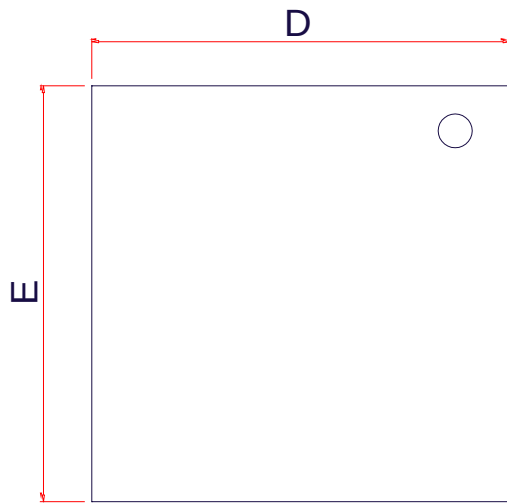
Gate Charge Characteristics



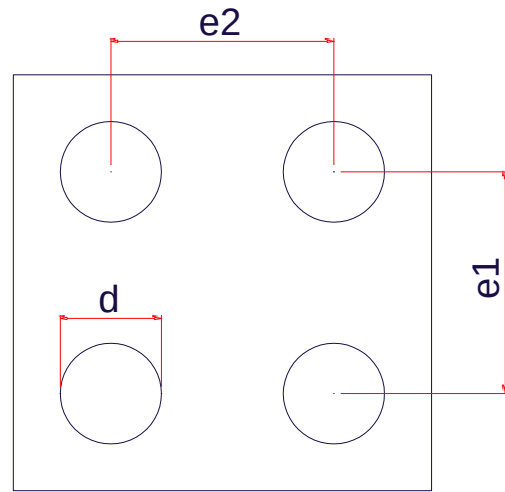
Transient thermal response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

CSP-4L



TOP VIEW



BOTTOM VIEW

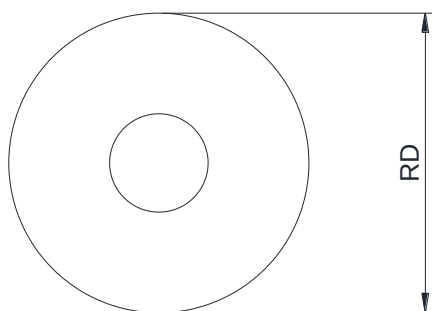


SIDE VIEW

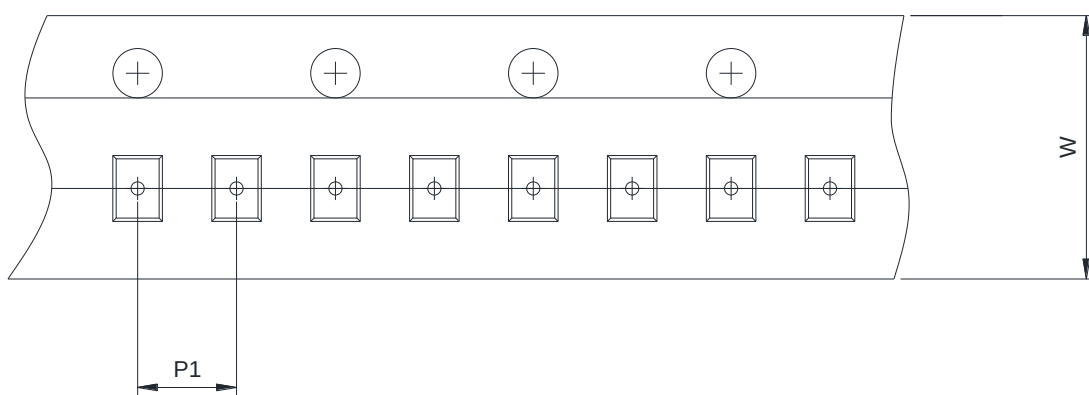
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.09	0.11	0.13
D	1.22	1.26	1.30
E	1.22	1.26	1.30
e	0.65BSC		
d	0.28	0.30	0.32

TAPE AND REEL INFORMATION

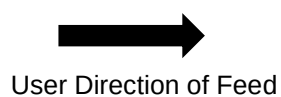
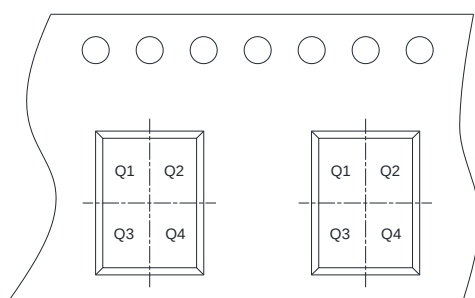
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☒ 7inch	☐ 13inch
W	Overall width of the carrier tape	☒ 8mm	☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm	☒ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☐ Q1	☒ Q2 ☐ Q3 ☐ Q4