WCR670N65T/TF/TG
650V N-Channel Super Junction MOSFET

Description

The WCR670N65 series is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. This device is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

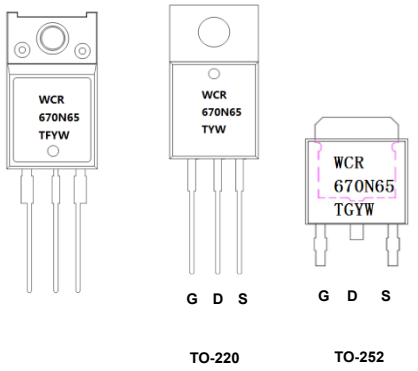
Features

- 700V@T_J=150°C
- Typ.$R_{DS(on)}$=0.55Ω
- Low gate charge
- 100% avalanche tested
- 100% R_g tested

Order Information

Device	Package	Marking	Units/Tube	Units/Real
WCR670N65T-3/T	TO-220	WCR670N65TYW(1)	50	
WCR670N65TF-3/T	TO-220F	WCR670N65TFYW(2)	50	
WCR670N65TG-3/TR	TO-252E-2L	WCR670N65TGYW(3)		2500

Note 1: WCR670N65T=Device code ;Y=Year ;W=Week (A~z);
Note 2: WCR670N65TF=Device code ;Y=Year ;W=Week (A~z);
Note 3: WCR670N65TG=Device code ;Y=Year ;W=Week (A~z);



TO-220 TO-252

Absolution Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**WCR670N65T WCR670N65TG**	**WCR670N65TF**	**Unit**
Drain-Source Voltage		V_{DS}	650		V
Gate-Source Voltage		V_{GS}	±30		
Continuous Drain Current[A]	T_C=25°C	I_D	7.8	4.8	A
	T_C=100°C		4.9	3	
Pulsed Drain Current		I_{DM}	31.2		A
Single Pulsed Avalanche Energy[B]		E_{AS}	113		mJ
Power Dissipation	T_C=25°C	P_D	80	30	W
	Derateabove 25°C		0.64	0.24	W/°C
Operating and Storage Temperature Range		T_J,T_{STG}	-55~150		°C
Lead Temperature		T_L	260		°C
Thermal Resistance Ratings					
Maximum Junction-to-Ambient		$R_{\theta JA}$	62[C]	80	°C/W
Maximum Junction-to-Case		$R_{\theta JC}$	1.55	4.2	

Electronics Characteristics (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-SourceBreakdownVoltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA,T_J=25°C	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =650V, V_{GS} = 0V,T_J=25°C			1	uA
Gate-to-sourceLeakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} =±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	2	3	4	V
Drain-to-source On-resistance	$R_{DS(on)}$[D]	V_{GS} = 10V, I_D = 3.9A		0.55	0.67	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz,V_{DS} = 400 V		481		pF
Output Capacitance	C_{OSS}			15		
Reverse Transfer Capacitance	C_{RSS}			1.4		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V,V_{DS} = 400 V, I_D = 7.8A		13.6		nC
Gate-to-Source Charge	Q_{GS}			3.2		
Gate-to-Drain Charge	Q_{GD}			5.6		
Gate resistance	R_g	V_{GS}=0V ,F=1MHZ,drain open		9.6		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 400 V, I_D = 3.9A,R_G=10 Ω		11		ns
Rise Time	t_r			21		
Turn-Off Delay Time	$t_{d(off)}$			40		
Fall Time	t_f			31		
Drain to Source Diode Characteristics and Maximum Ratings						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 7.8A			1.5	V
Body-Diode Continuous Current	I_S			7.8		A
Body-Diode Pulsed Current	I_{SM}			31.2		A
Body Diode Reverse Recovery Time	T_{rr}	I_F=3.9A,dI/dt=100A/us,V_{DS}=400V		205		nS
Body Diode Reverse Recovery Charge	Q_{rr}			1.4		uC
Peak reverse recovery Current	I_{rrm}			12		A

NOTES:

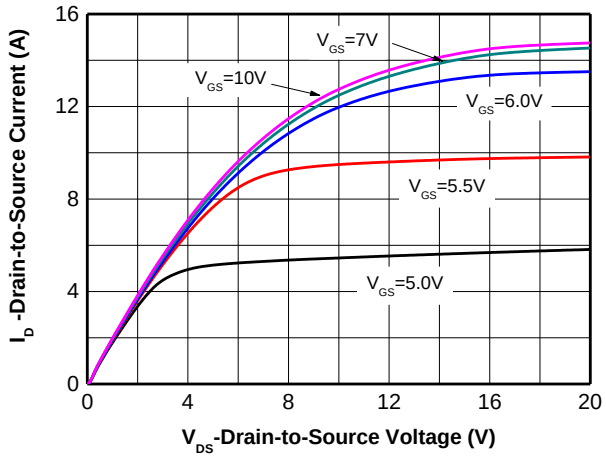
A. Drain current limited by maximum junction temperature. Maximum duty cycle D=0.75

B. L=100mH, I_{AS}=1.5A, V_{DD}=50V, Starting T_J=25℃

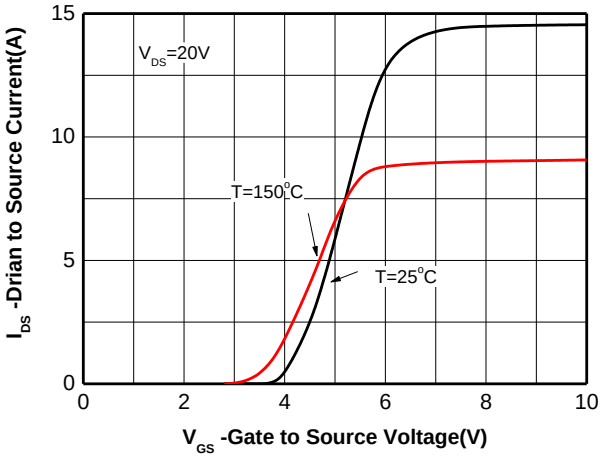
C. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C

D. Pulse Test: Pulse width≤300us, Duty Cycle ≤2%sensitively Independent of Operating Temperature Typical Characteristics

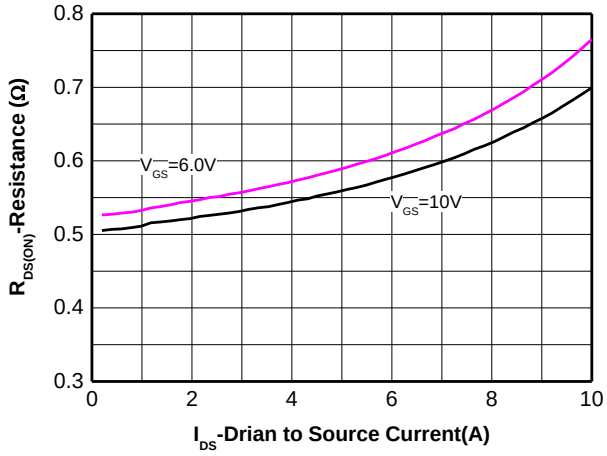
Typical Characteristics (T_A=25°C, unless otherwise noted)



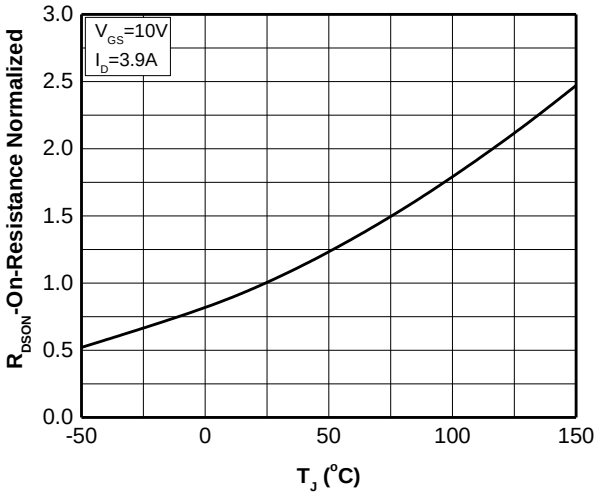
Output characteristics



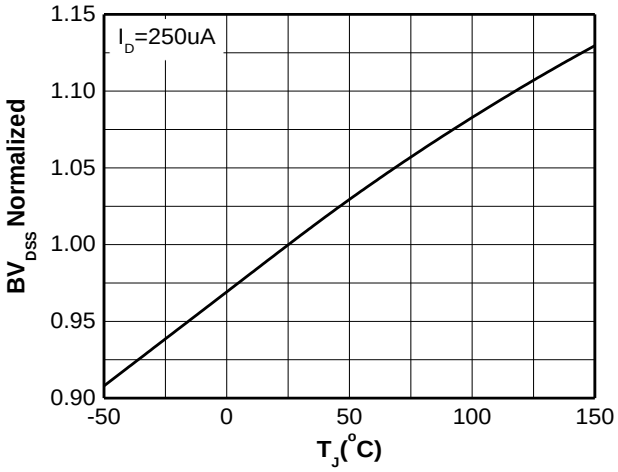
Transfer characteristics



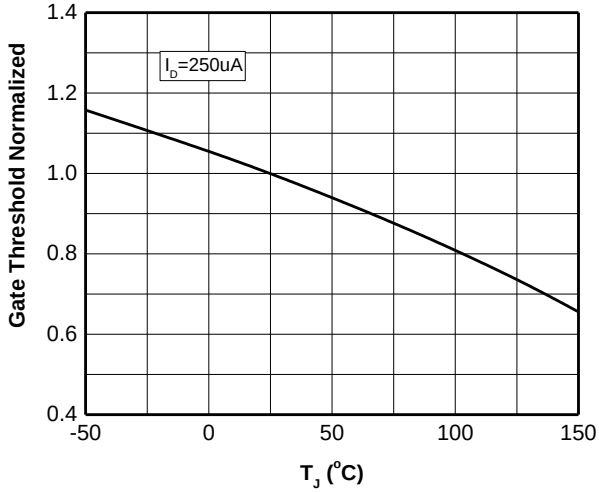
On-Resistance vs. Drain current



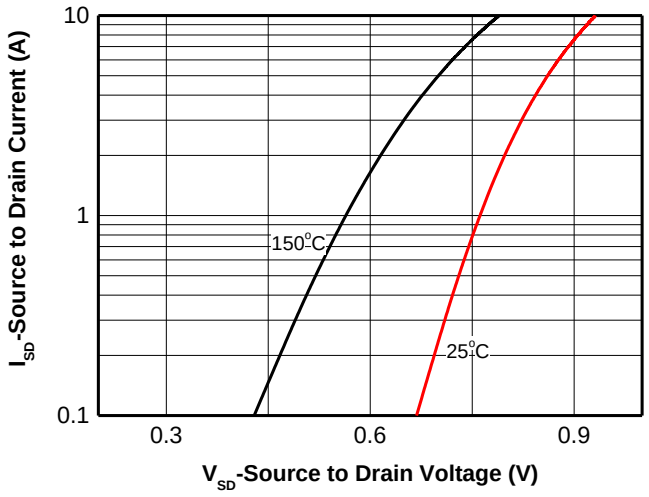
On-Resistance vs. Junction temperature



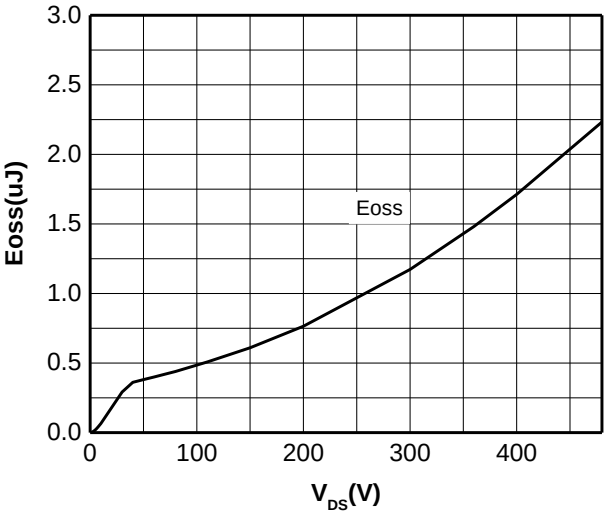
Breakdown Voltage vs. Junction temperature



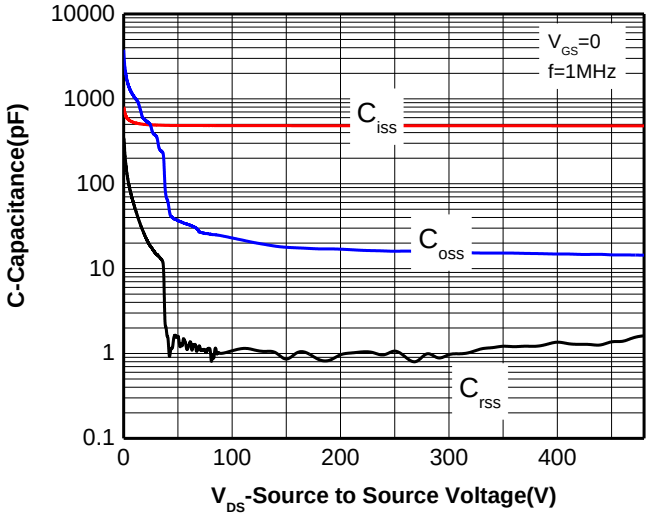
Threshold voltage vs. Junction temperature



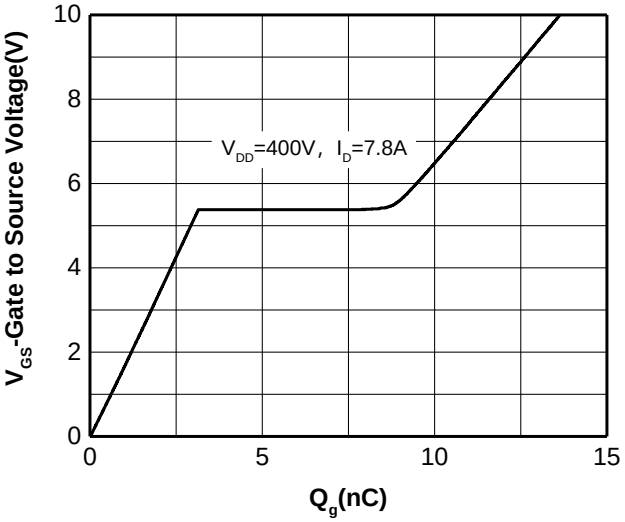
Body diode forward voltage



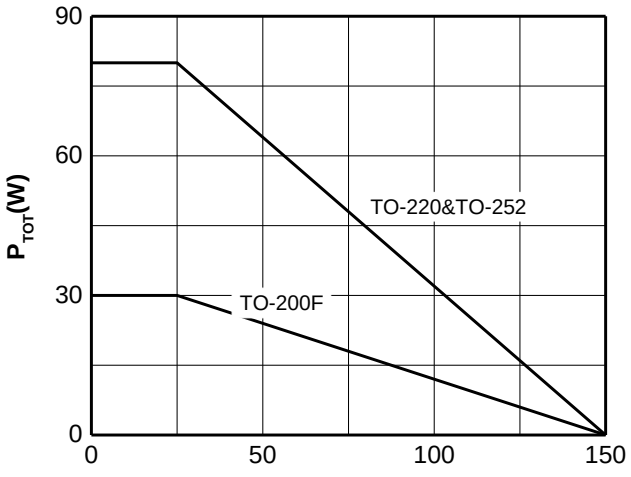
Cossstored Energy



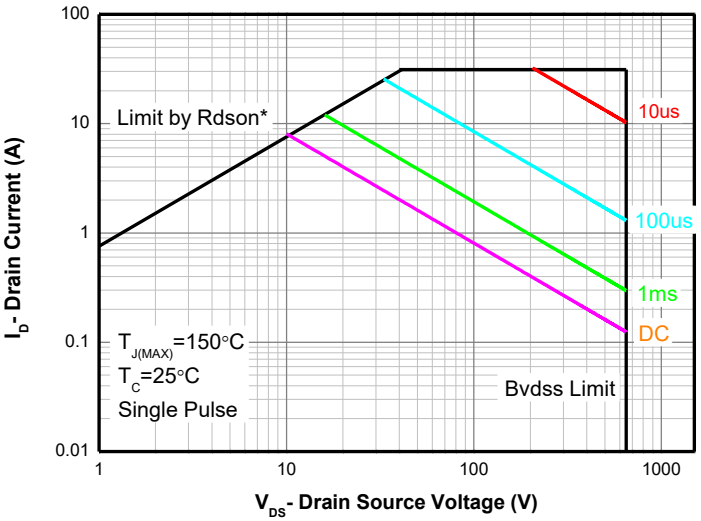
Capacitance



Gate charge Characteristics

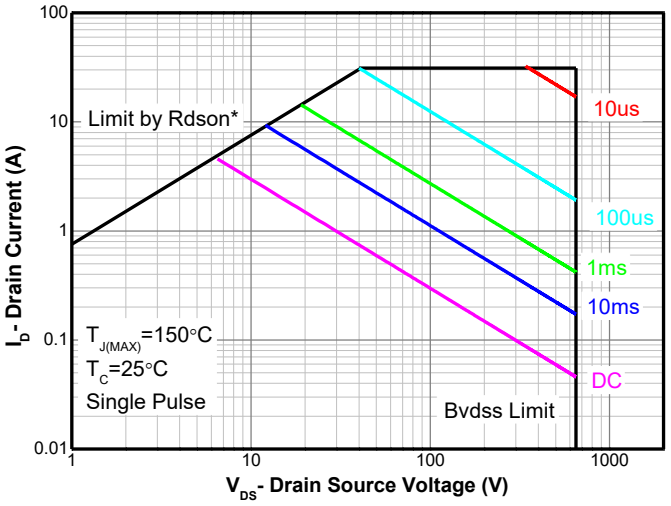


Power dissipation



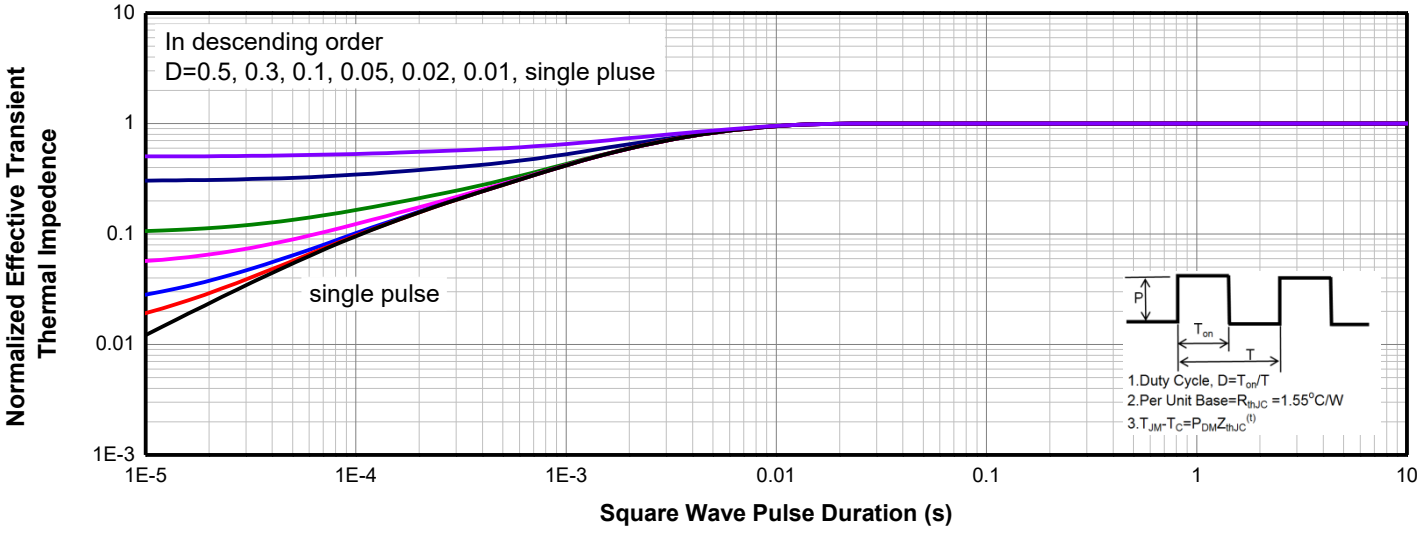
TO-220&TO-252

Safe operating area(Note D)

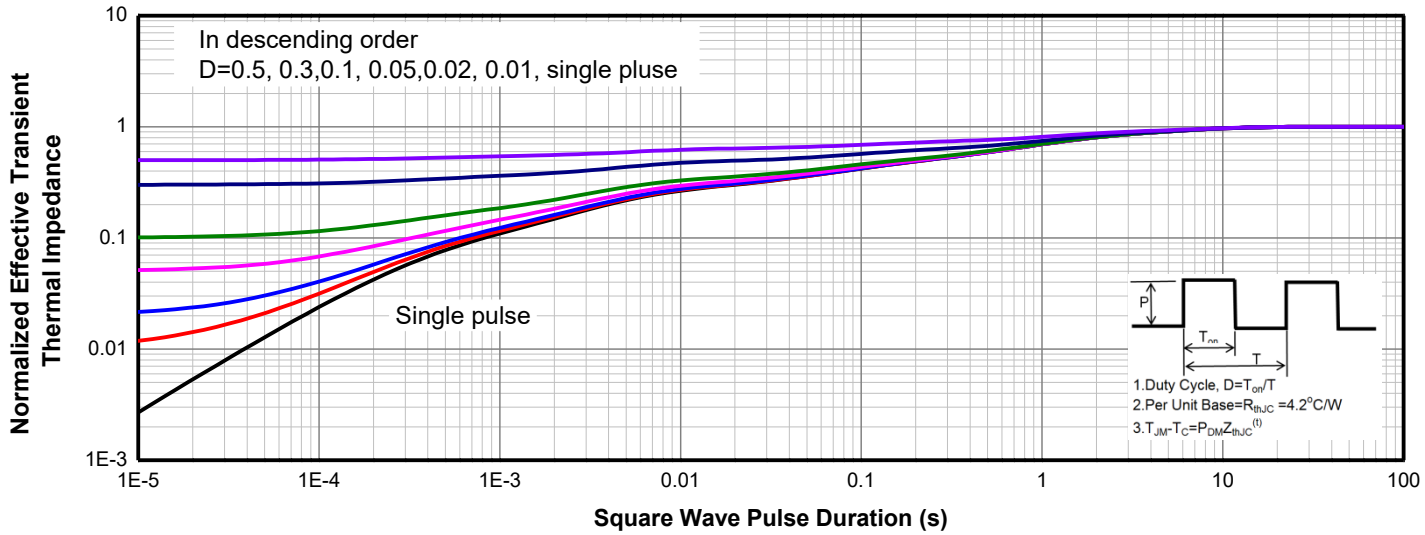


TO-220F

Safe operating area(Note D)



TO-252&TO-220

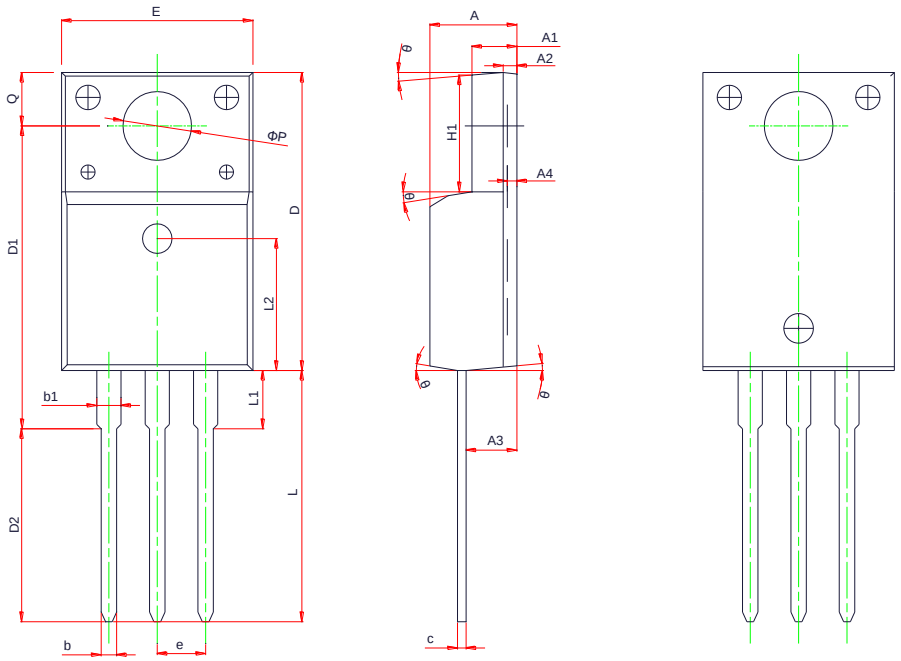


TO-220F

Transient thermal response(Junction to case)(Note D)

PACKAGE OUTLINE DIMENSIONS

TO–220F–3L

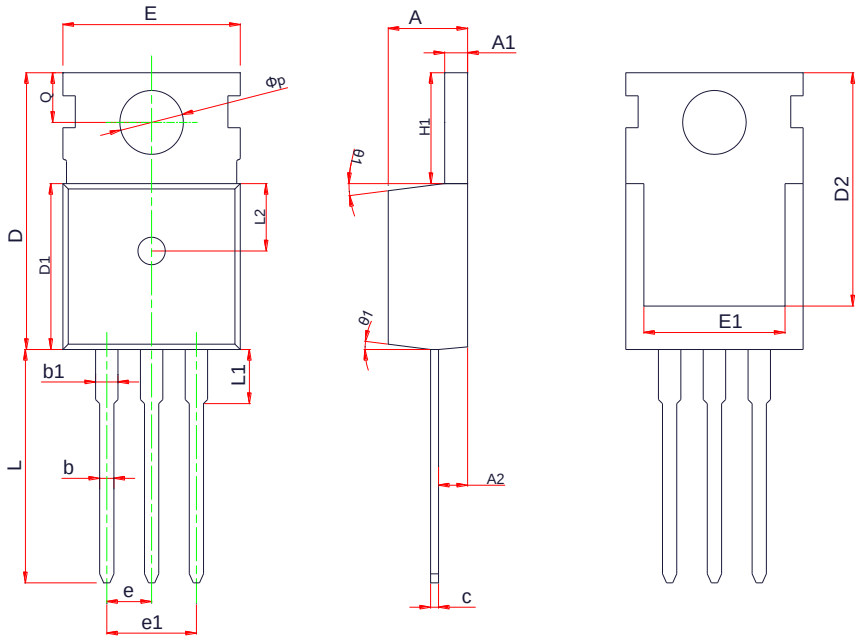


TOP VIEW SIDE VIEW BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	4.50	4.72	4.90
A1	2.45	2.56	2.65
A2		0.72Ref	
A3	2.68	2.78	2.88
A4	-	-	0.45
b	0.70	0.80	0.90
b1	1.18	1.28	1.38
c	0.45	0.52	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
E	9.96	10.16	10.36
e		2.45BSC	
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2		2.54BSC	
φP	3.08	3.18	3.28
Q	3.20	-	3.40
θ	3°	5°	7°

PACKAGE OUTLINE DIMENSIONS

TO–220–3L

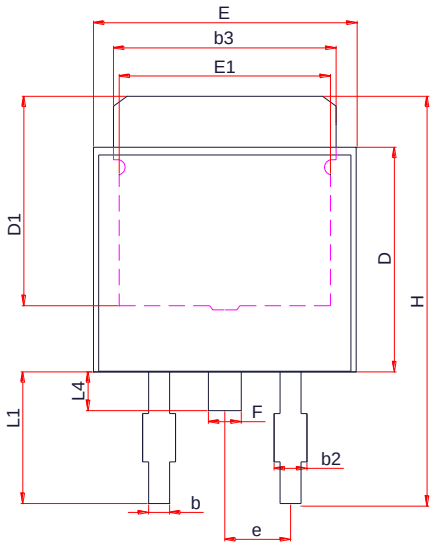


TOP VIEW SIDE VIEW BOTTOM VIEW

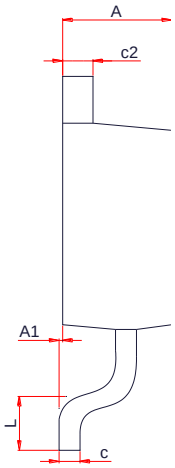
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	0.80	0.90
b1	1.30	-	1.37
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	12.90	13.10	13.30
E	9.70	9.90	10.20
E1	7.70	7.90	8.10
e	2.45Ref		
e1	5.08Ref		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	-	-	3.50
L2	4.06Ref		
ØP	3.55	3.60	3.65
Q	2.73	-	2.87
θ1	3°	5°	7°

PACKAGE OUTLINE DIMENSIONS

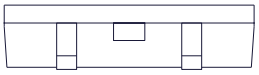
TO–252E–2L



TOP VIEW



SIDE VIEW

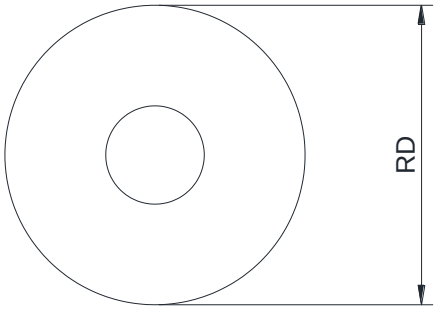


SIDE VIEW

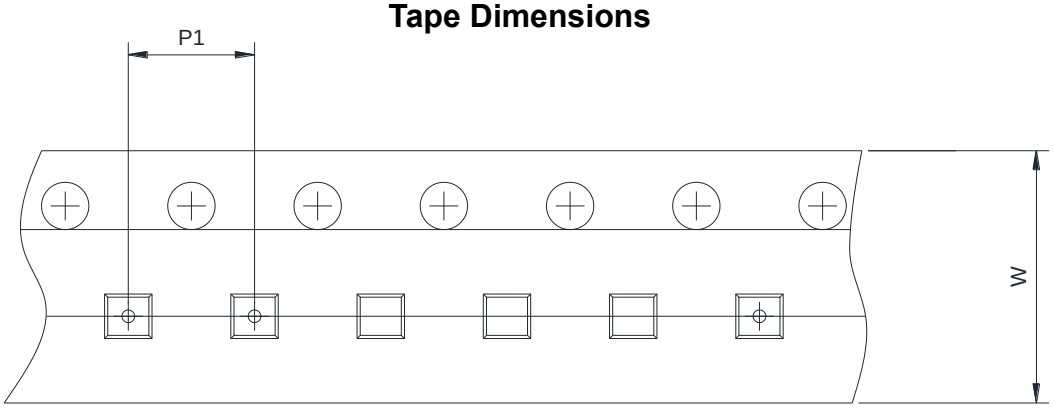
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0	0.08	0.15
b	0.50	0.60	0.70
b2	0.60	0.75	0.90
b3	5.20	5.35	5.50
c2	0.45	0.50	0.55
c	0.51Ref		
D	5.40	5.60	5.80
D1	4.57	-	-
E	6.40	6.60	6.80
E1	3.81	-	-
e	2.30Ref		
F	0.70	0.80	0.90
H	9.40	9.80	10.20
L	1.40	1.59	1.77
L1	2.40	2.70	3.00
L4	0.80	1.00	1.20

TAPE AND REEL INFORMATION

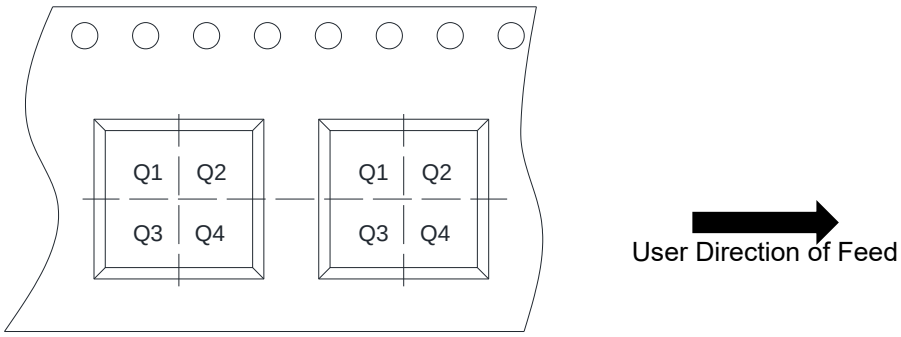
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☐ 12mm	☑ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4

制修订记录					
文件版本	制修日期	修订页次	修订人	变更内容	
Rev. 0.9	20180712	非正式版	衷世雄	非正式版	
Rev. 1.0	20180925	正式版	衷世雄	正式版，热阻更新	
Rev.1.1	20190621	正式版	衷世雄	正式版，更新热阻及 Eas	
批准		审核		编制	
日期		日期		日期	

各部门会签			
应用部	封装部	市场部	生产管理部
市场部上传者/上传时间			
品质部确认者/确认时间			