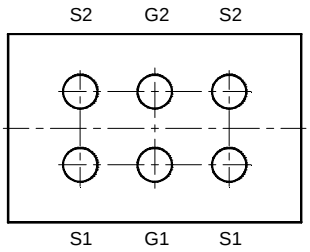
WNMD2183

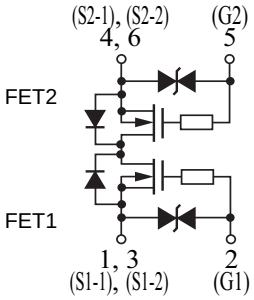
Dual N-Channel, 12V, 14A, Power MOSFET

Http://www.sh-willsemi.com

V_{sss} (V)	Typ $R_{ss(on)}$ (mΩ)
12	5.0@ V_{GS}=4.5V
	5.5@ V_{GS}=3.8V
	6.0@ VGS=3.1V
	7.0@ VGS=2.5V
ESD HBM 2KV	



CSP-6L



Pin configuration (Top view)

Descriptions

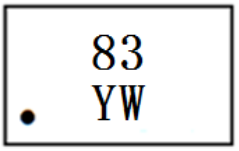
The WNMD2183 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent $R_{SS(ON)}$ with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2183 is available in CSP-6L package. Standard Product WNMD2183 is Pb-free and Halogen-free.

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-6L

Applications

- Lithium-Ion battery protection circuit



83 = Device Code
YW = Special Code

Marking

Order information

Device	Package	Shipping
WNMD2183-6/TR	CSP-6L	5000/Reel&Tape

Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V_{SSS}	V_{GS} = 0 V, I_S = 250uA	12			V
Zero Gate Voltage Drain Current	I_{SSS}	V_{SS} =10 V, V_{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±10V TEST CIRCUIT 2			±10	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{GS} = V_{SS}, I_S = 250uA TEST CIRCUIT 3	0.45	0.7	1.0	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 3.0A TEST CIRCUIT 5	3.5	5.0	6.0	mΩ
		V_{GS} = 3.8V, I_S = 3.0A TEST CIRCUIT 5	3.8	5.5	6.6	
		V_{GS} = 3.1V, I_S = 3.0A TEST CIRCUIT 5	4.1	6.0	8.0	
		V_{GS} = 2.5V, I_S = 3.0A TEST CIRCUIT 5	4.5	7.0	11	
Forward Transfer Admittance	| yfs |	V_{SS} = 10 V, I_S = 3A TEST CIRCUIT 4		12		S
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	$V_{F(S-S)}$	V_{GS} = 0 V, I_F = 6.0A TEST CIRCUIT 6		0.8	1.5	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 4.5 V, V_{SS}=8V, I_S=6A,R_G=6Ω TEST CIRCUIT 8		0.69		us
Rise Time	tr			18.8		
Turn-Off Delay Time	td(OFF)			6.02		
Fall Time	tf			4.2		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1kHz, V_{SS} = 10 V TEST CIRCUIT 7		2918		pF
Output Capacitance	C_{OSS}			402		
Reverse Transfer Capacitance	C_{RSS}			376		
Total Gate Charge	$Q_{G(TOT)}$	V_{G1S1} = 4.5 V, V_{SS} = 10V, I_S =6A TEST CIRCUIT 9		47		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.2		
Gate-to-Source Charge	Q_{GS}			8		
Gate-to-Drain Charge	Q_{GD}			10		

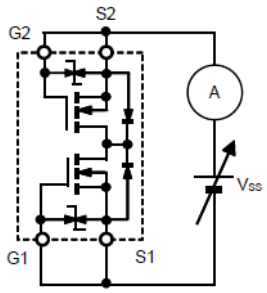
Absolute Maximum ratings

Parameter	Symbol	Rating	Unit
Source to Source Voltage (V_{GS} = 0 V)	V_{SSS}	12	V
Gate to Source Voltage (V_{SS} = 0 V)	V_{GSS}	±10	
Source Current (pulse)Note.1	$I_{S(pulse)}$	60	A
Source Current (DC)	I_S	14	A
Channel Temperature	T_{ch}	-55 to150	°C
Storage Temperature Range	T_{stg}	-55 to150	°C

Note.1 PW≤10μs, duty cycle≤1%;

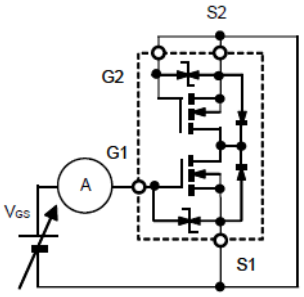
Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

TEST CIRCUIT 1 Isss



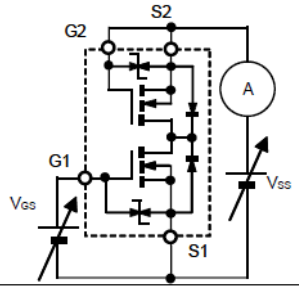
TEST CIRCUIT 2 IGSS

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



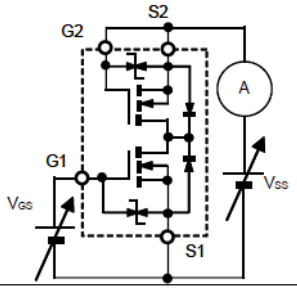
TEST CIRCUIT 3 VGS(off)

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



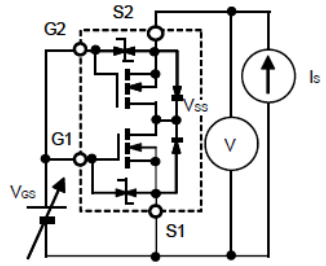
TEST CIRCUIT 4 | yfs |

ΔIs/ΔVGS



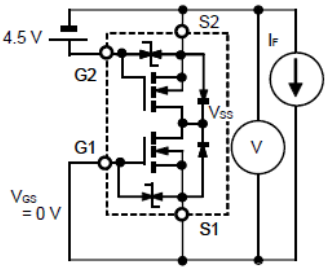
TEST CIRCUIT 5 $R_{SS(on)}$

V_{SS}/I_S

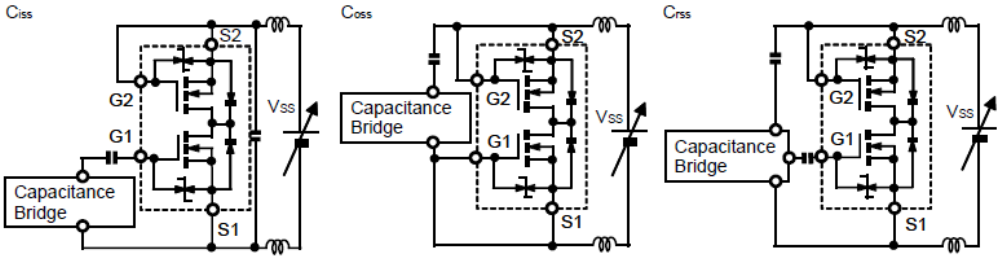


TEST CIRCUIT 6 $V_{F(S-S)}$

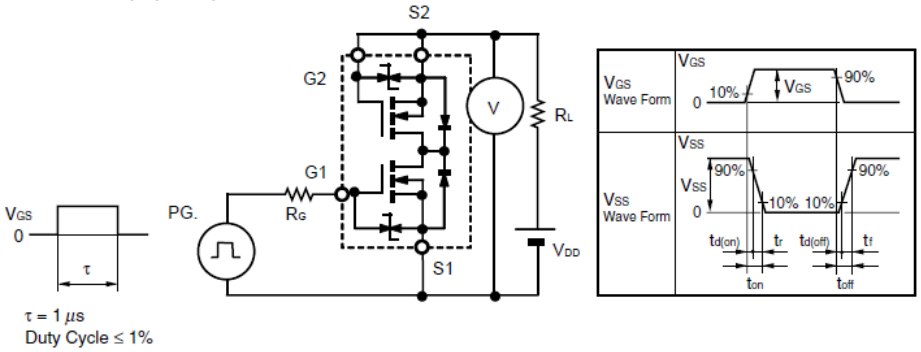
When FET1 is measured,
FET2 is added V_{GS} +4.5 V.



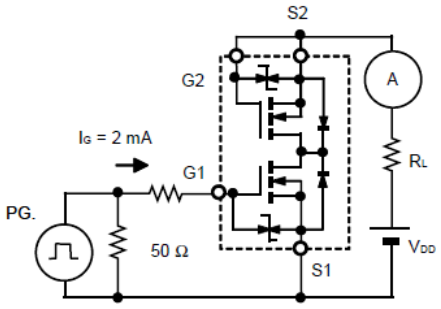
TEST CIRCUIT 7



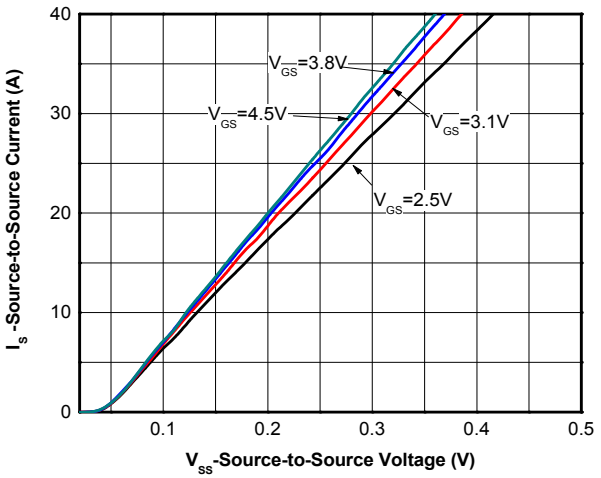
TEST CIRCUIT 8 $t_{d(on)}$, t_r, $t_{d(off)}$, t_f



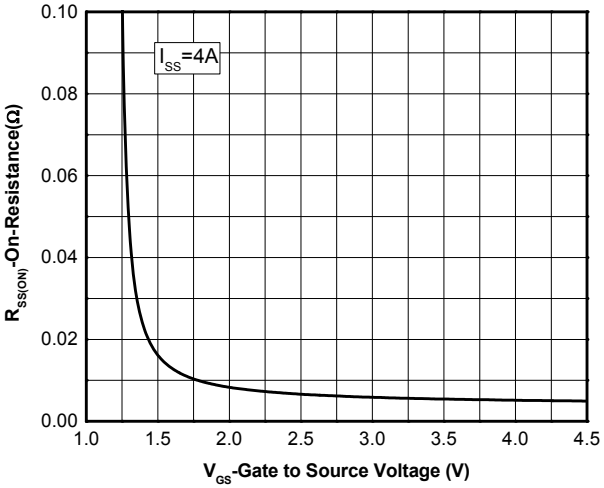
TEST CIRCUIT 9 Q_G



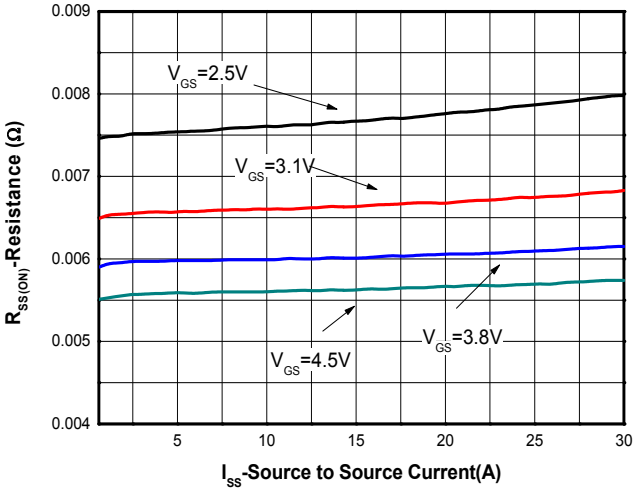
Typical Characteristics (Ta=25°C, unless otherwise noted)



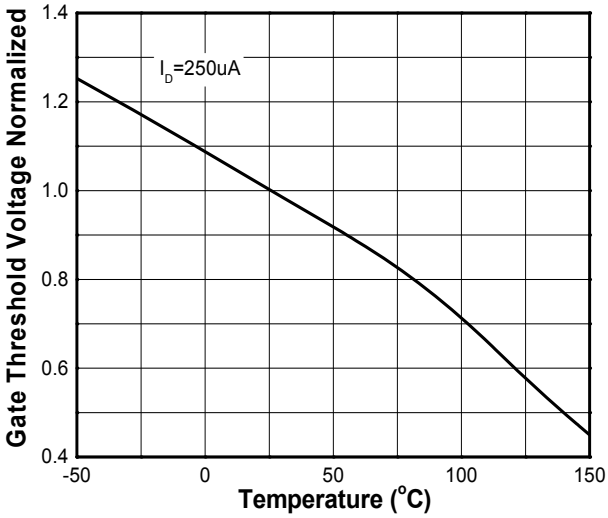
Source current vs. source to source voltage



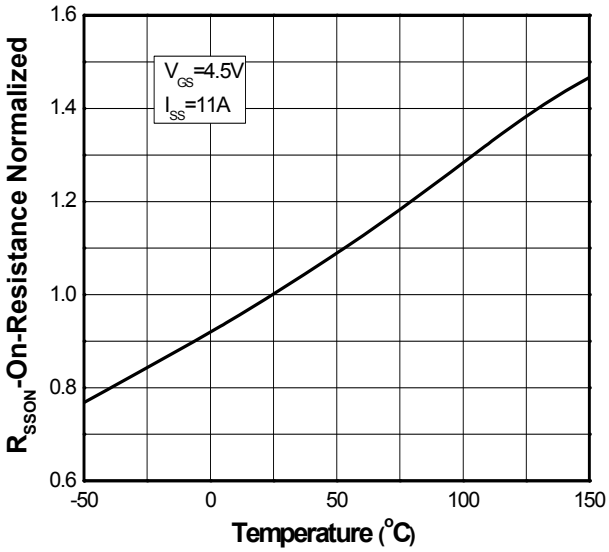
On-Resistance vs.Gate-to-source voltage



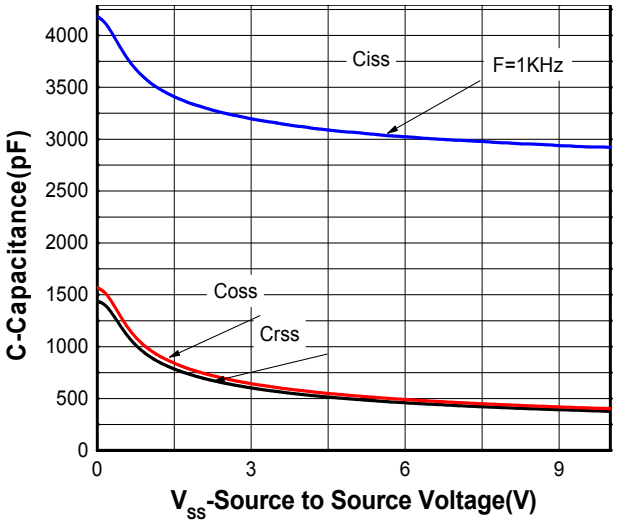
On-Resistance vs.Source current



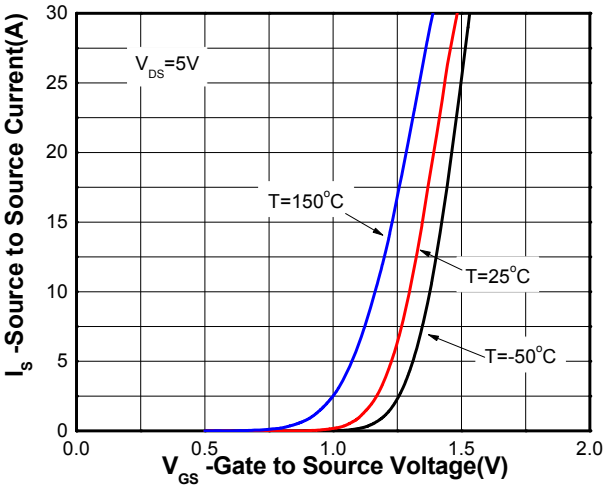
Threshold voltage vs. Temperature



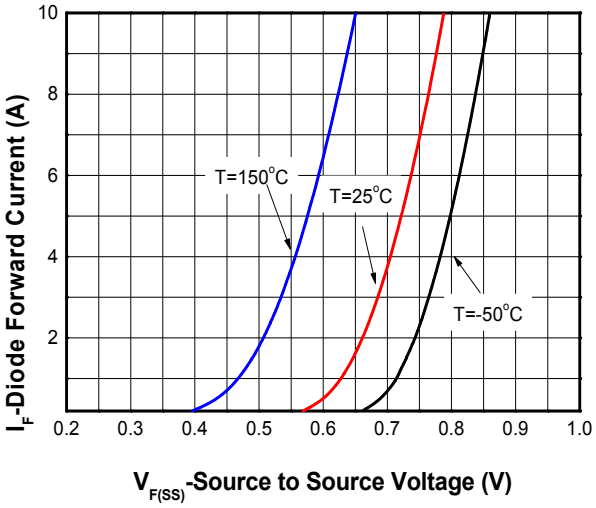
ON-Resistance vs.Junction temperature



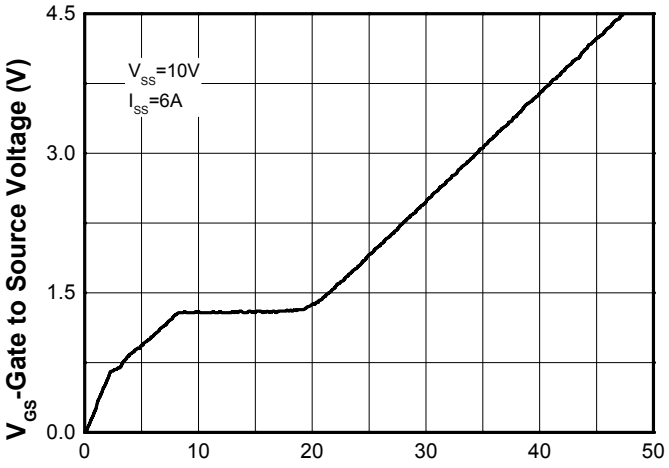
Capacitance



Transfer characteristics



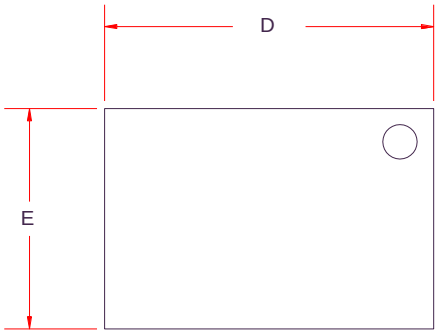
Body diode forward voltage



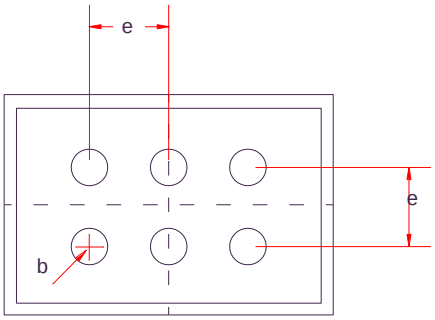
Gate Charge Characteristics

PACKAGE OUTLINE DIMENSIONS

CSP-6L



TOP VIEW

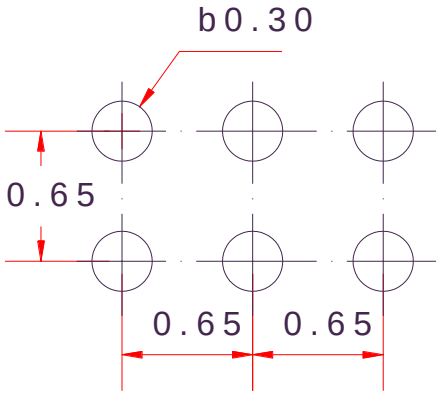


BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.09	0.11	0.13
D	2.65	2.70	2.75
E	1.76	1.81	1.86
e		0.65 Typ.	
b	0.27	0.30	0.33

Recommend PCB Layout (Unit: mm)

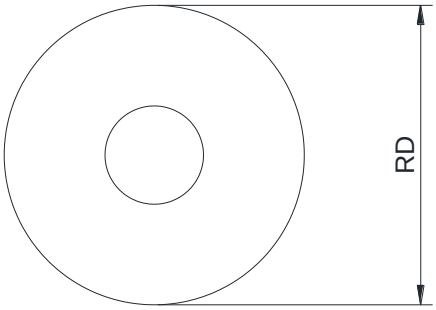


Notes:

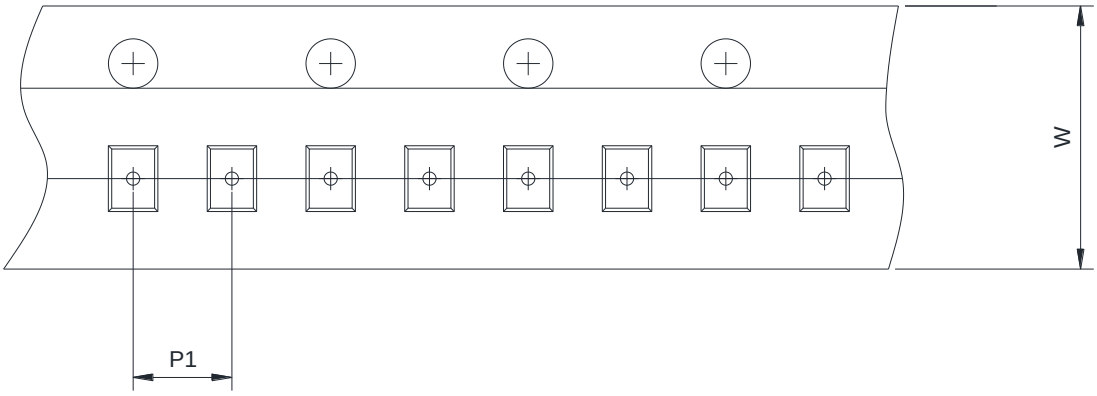
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

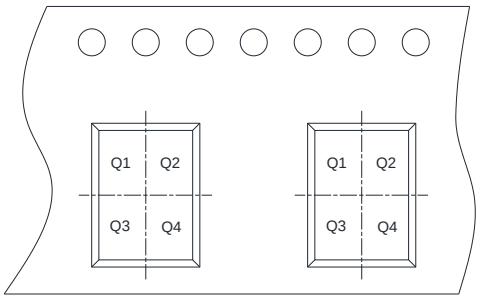
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4