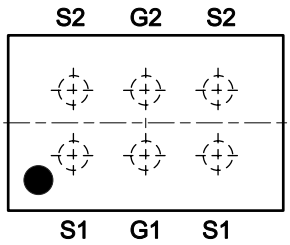
WNMD2190

Dual N-Channel, 12V, 9.2A, Power MOSFET

http://www.omnivision-group.com/

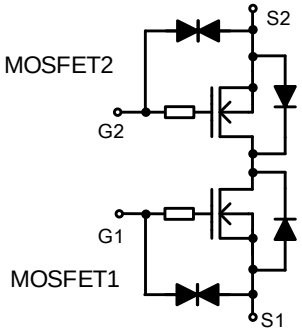
V_{sss} (V)	Max $R_{ss(on)}$ (mΩ)
12	5.1@ V_{GS}=4.5V
	5.5@ V_{GS}=3.8V
	6.8@ V_{GS}=3.1V
	10.0@ V_{GS}=2.5V
ESD Rating:2000V HBM	



CSP-6L (Top view)

Descriptions

The WNMD2190 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent $R_{SS(ON)}$ with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2190 is available in CSP-6L package. Standard Product WNMD2190 is Pb-free and Halogen-free.



Pin Configuration

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-6L

2190 = Device Code
Y = Year
W = Week
ND = Special Code
XXYY = Coordinate

Marking

Applications

- Lithium-Ion battery protection circuit

Order information

Device	Package	Shipping
WNMD2190-6/TR	CSP-6L	3000/Reel&Tape

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Source -Source Voltage		V_{SS}	12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Source Current	T_A=25°C	I_S[a]	9.2	A
		I_S[b]	19.8	
Pulsed Source Current [c]		I_{SM}	87	
Maximum Power Dissipation	T_A=25°C	P_D[a]	0.49	W
		P_D[b]	2.26	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation				
Parameter	**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$[a]	171	257	°C/W
	$R_{\theta JA}$[b]	48	55	

Note:

a. FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) minimum pad covered with copper.

b. Ceramic substrate (70 mm X 70 mm X t1.0 mm, 70um Copper) fully covered with copper.

c. Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d. The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

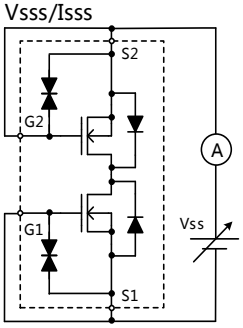
Electronics Characteristics (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V_{SSS}	V_{GS} = 0 V, I_S = 1mA	12			V
Zero Gate Voltage Drain Current	I_{SSS}	V_{SS} =10 V, V_{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±8V TEST CIRCUIT 2			±10	uA
		V_{SS} = 0 V, V_{GS} = ±5V TEST CIRCUIT 2			±1	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	V_{GS}(th)	V_{SS}= 10 V, I_S = 1mA TEST CIRCUIT 3	0.5	0.9	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 4.0A TEST CIRCUIT 4	3.0	4.0	5.1	mΩ
		V_{GS} = 3.8V, I_S = 4.0A TEST CIRCUIT 4	3.2	4.3	5.5	
		V_{GS} = 3.1V, I_S = 4.0A TEST CIRCUIT 4	3.5	4.8	6.8	
		V_{GS} = 2.5V, I_S = 4.0A TEST CIRCUIT 4	3.8	6.2	10.0	
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	$V_{F(S-S)}$	V_{GS} = 0 V, I_F = 4.0A TEST CIRCUIT 7	0.5	0.7	1.2	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 4.0V, V_{SS}=10V, I_S=4.0A, TEST CIRCUIT 5		0.91		us
Rise Time	tr			3.1		
Turn-Off Delay Time	td(OFF)			4.4		
Fall Time	tf			5.7		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1kHz, V_{SS} = 10 V		2038		pF
Output Capacitance	C_{OSS}			428		
Reverse Transfer Capacitance	C_{RSS}			358		
Total Gate Charge	$Q_{G(TOT)}$	V_{G1S1} = 4.0 V, V_{SS} = 10V, I_S =4.0A TEST CIRCUIT 6		33		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.6		
Gate-to-Source Charge	Q_{GS}			5		
Gate-to-Drain Charge	Q_{GD}			13		

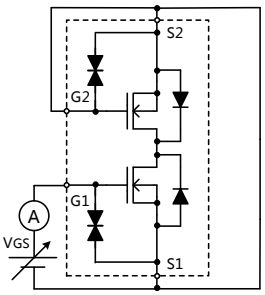
Test Circuit

FET1 and the FET2 are both measured. Test circuits are example of measuring the FET1 side

Test Circuit 1
Vsss/Isss



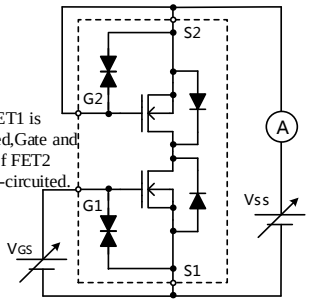
Test Circuit 2
I_{GSS}



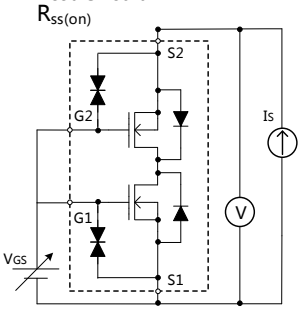
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS}(th)$

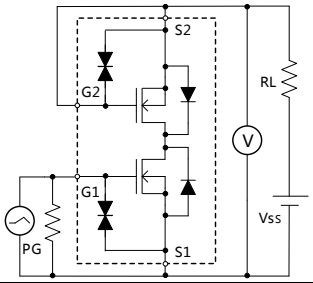
When FET1 is measured,Gate and Source of FET2 are short-circuited.



Test Circuit 4
$R_{ss(on)}$

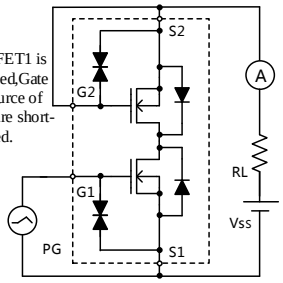


Test Circuit 5
$t_{d(on)}, t_r, t_{d(off)}, t_f$

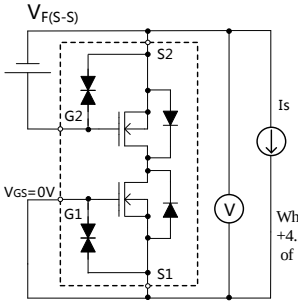


Test Circuit 6
Qg

When FET1 is measured,Gate and Source of FET2 are short-circuited.

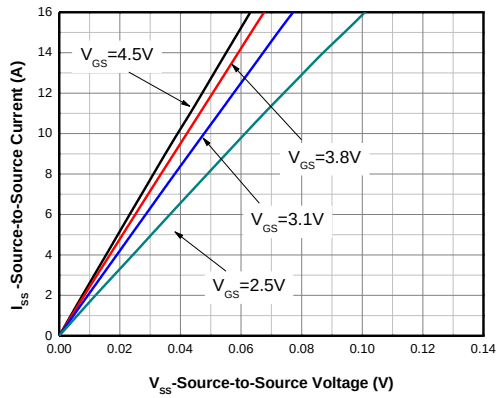


Test Circuit 7
$V_{F(S-S)}$

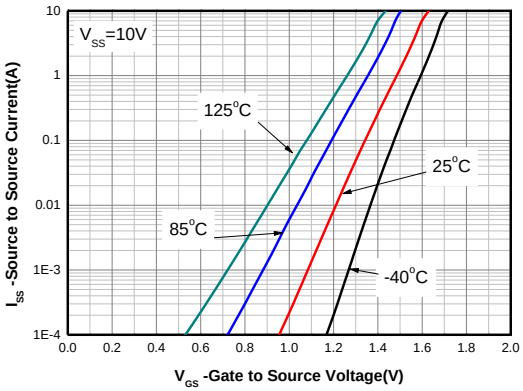


When FET1 is measured, +4.5V is added to V_{GS} of FET2.

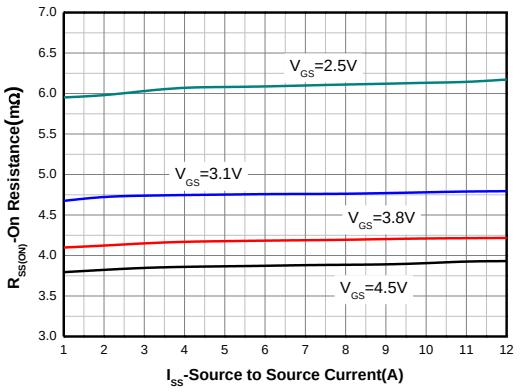
Typical Characteristics (T_A=25°C, unless otherwise noted)



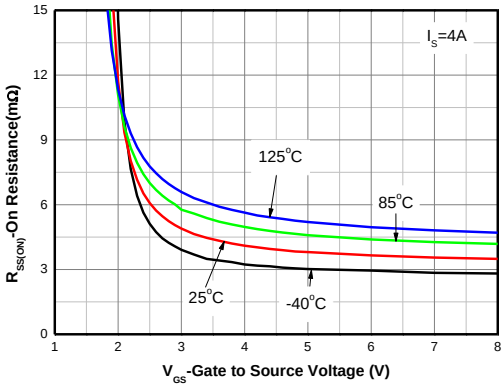
Output Characteristics [d]



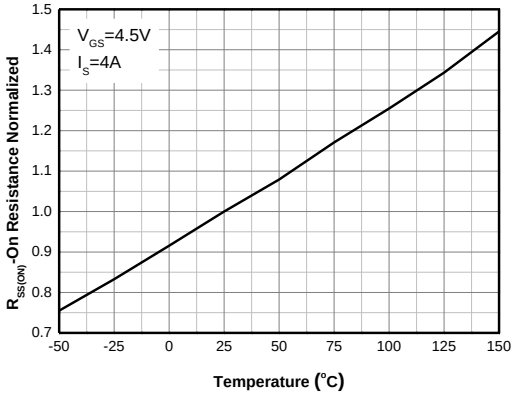
Transfer Characteristics [d]



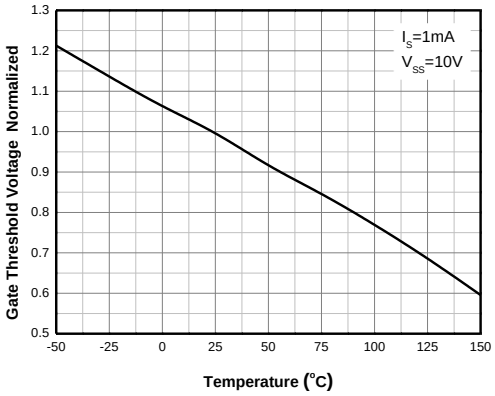
On-Resistance vs. Source Current [d]



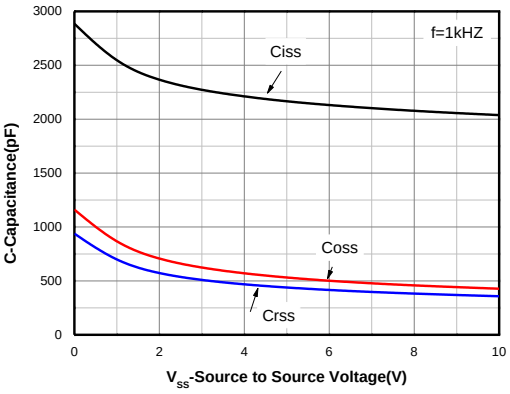
On-Resistance vs. Gate-to-Source Voltage [d]



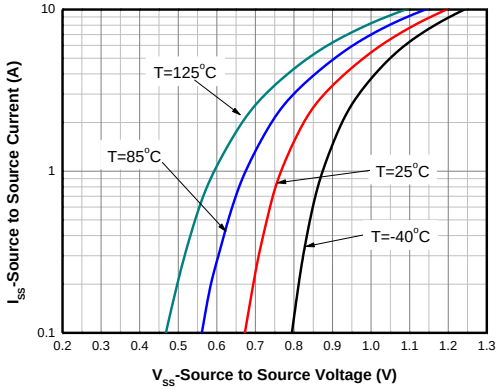
On-Resistance vs. Junction Temperature [d]



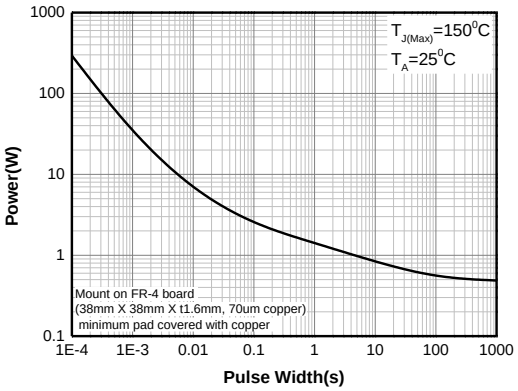
Threshold Voltage vs. Temperature



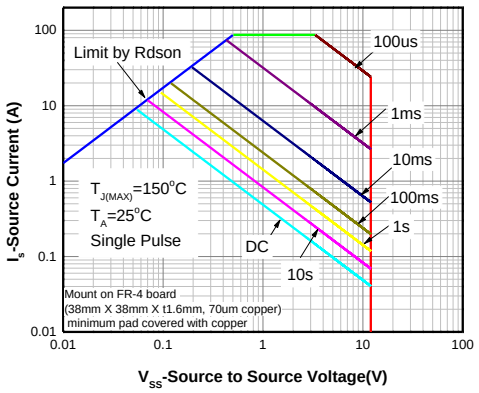
Capacitance



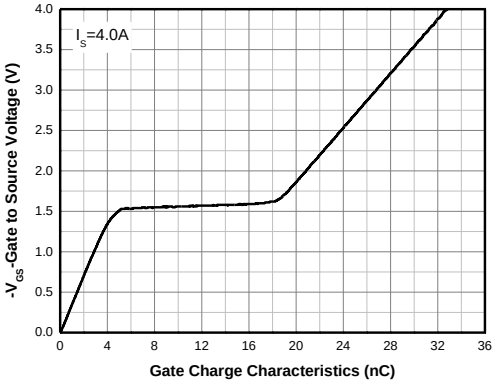
Body Diode Forward Voltage [d]



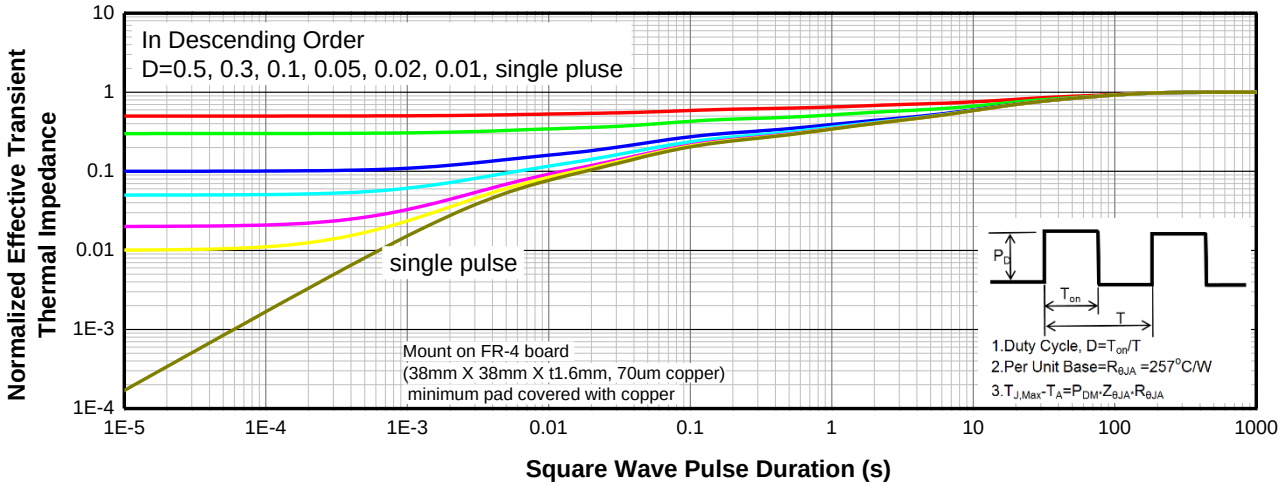
Single Pulse power



Safe Operating Power



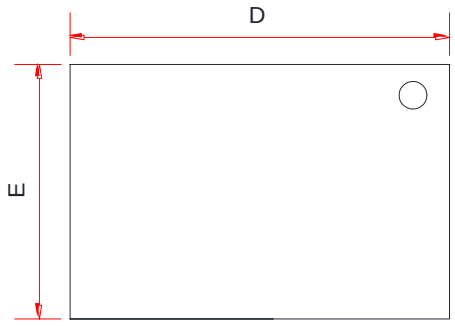
Gate Charge Characteristics



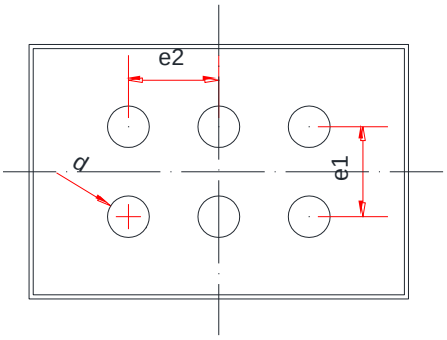
Transient thermal response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

CSP-6L



TOP VIEW

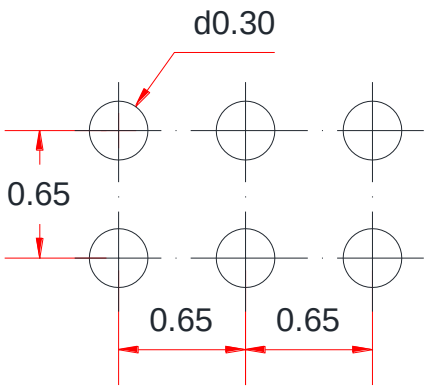


BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.09	0.11	0.14
D	2.10	2.14	2.18
E	1.63	1.67	1.71
e1	0.650 Typ.		
e2	0.650 Typ.		
d	0.27	0.30	0.33

Recommend PCB Layout (Unit: mm)

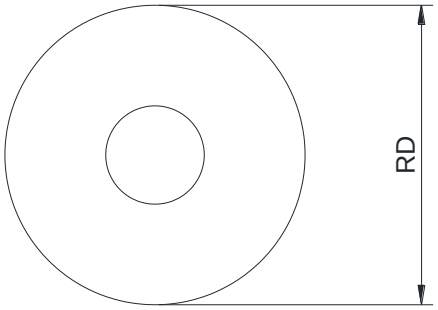


Notes:

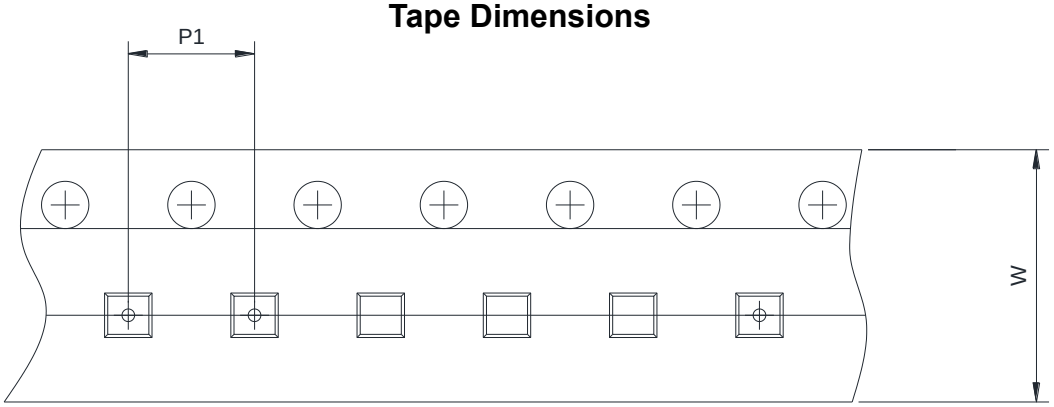
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

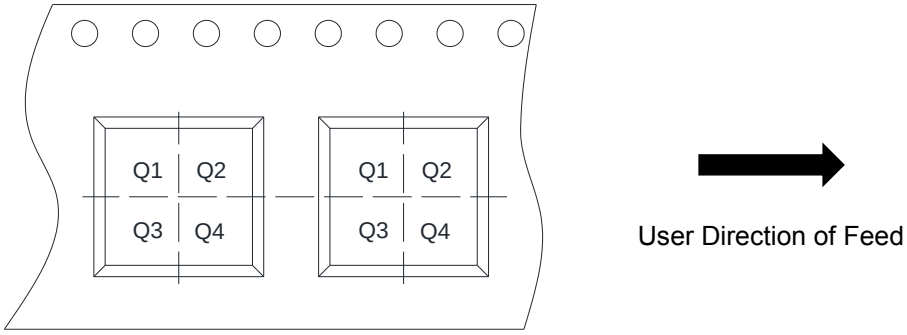
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☐ Q1 ☐ Q2 ☐ Q3 ☑ Q4