

### **Features**

- ☐ Transient protection for high-speed data lines
  IEC 61000-4-2 (ESD) ±16kV (Air)
  ±8kV (Contact)
- ☐ Protects one high-speed data line
- ☐ Low reverse current:10nA typical (VR=5V)
- Working voltage: 5V
- ☐ Low capacitance: 0.30pF(Typical)
- ☐ Solid-state silicon-avalanche technology

## **Description**

TT0541SA are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. They are designed to replace 0201 size mul-tilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation. TT0541SA has a typical capacitance of only 0.30pF. This allows it to be used on circuits operating.

TT0541SA is in a 2-pin DFN0603 package. It measures 0.6 x 0.3 mm with a nominal height of only 0.30mm. Leads are finished with lead-free NiAu. Each device will protect one line operating at 5 volts. It gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and MP3 players.

### **Applications**

- ☐ HDMI 1.3/1.4 and HDMI 2.0
- ☐ USB 2.0 and USB 3.0
- MHL
- ☐ LVDS Interfaces
- ☐ FM Antenna
- □ PCI Express
- eSATA Interfaces

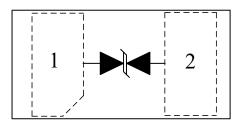
### **Mechanical Characteristics**

- ☐ DFN0603 package
- ☐ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- □ Nominal Dimensions: 0.6 x 0.3 x 0.3 mm
- ☐ Lead Finish: NiAu
- ☐ Molding compound flammability rating: UL 94V-0
- ☐ Packaging: Tape and Reel

### **Circuit Diagram**



# **Pin Configuration**



DFN0603-2L (Top View)

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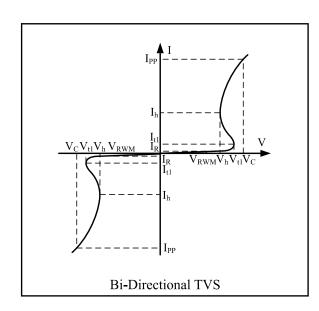


## **Absolute Maximum Rating**

Symbol	Parameter	Value	Units
${ m I}_{ m PP}$	Peak Pulse Current(tp=8/20us)	4	A
$ m V_{ESD}$	ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2 (Contact)	±16 ±8	kV
$T_{OPT}$	Operating Temperature	-55/+125	°C
$T_{STG}$	Storage Temperature	-55/+150	°C

# **Electrical Characteristics (T = 25°C)**

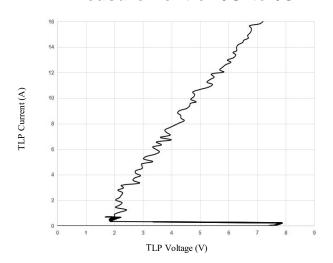
Symbol	Parameter
$V_{RWM}$	Nominal Reverse Working Voltage
$I_R$	Reverse Leakage Current @ V <sub>RWM</sub>
$V_{t1}$	Trigger Voltage
$I_{t1}$	Trigger Current @ Vt1
$V_h$	Holding Voltage
$I_h$	Holding Current @ V <sub>h</sub>
$V_{\rm C}$	Clamping Voltage @ I <sub>PP</sub>
$I_{PP}$	Maximum Peak Pulse Current
$C_{ESD}$	Parasitic Capacitance
$\mathrm{C}_{\Delta}$	Variation in C <sub>ESD</sub> with Reverse Bias



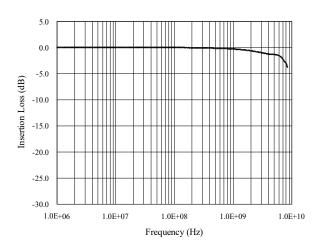
Symbol	Test Condition	Minimum	Typical	Maximum	Units
$ m V_{RWM}$				5.0	V
$I_R$	$V_{RWM} = 5.0  V,  T = 25^{\circ} C$			0.1	uA
$V_{t1}$	$I_{t1} = 1 \text{mA}$	6.0		10.0	V
$V_{h}$	I <sub>h1</sub> =100mA	2.0		3.0	V
$V_{\rm C}$	$I_{PP} = 4 \text{ A}, t_p = 8/20 \mu s$			7.0	V
$C_{ESD}$	$V_R = 0 V, f = 1 MHz$		0.3		pF



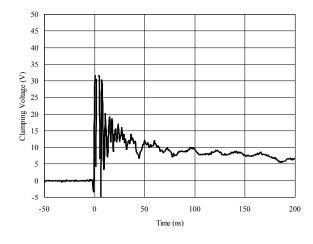
### TLP Measurement of I/O to I/O



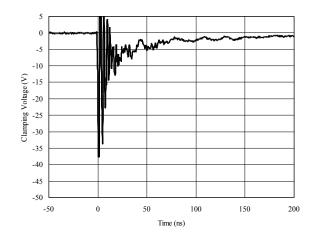
### Insertion Loss S21 of I/O to I/O



# ESD Clamping of I/O to I/O (+8kV Contact per IEC 61000-4-2)



# ESD Clamping of I/O to I/O (-8kV Contact per IEC 61000-4-2)





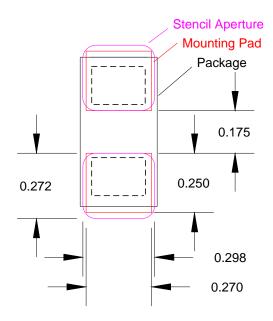
## **Application Information**

#### **Assembly Guidelines**

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The table below provides TITAN's recommended assembly guidelines for Mounting this device. The figure at the right details TITAN's recommended aperture based on the below recommendations. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. The exact manufacturing parameters will require some experimentation to get the desired solder application.

Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

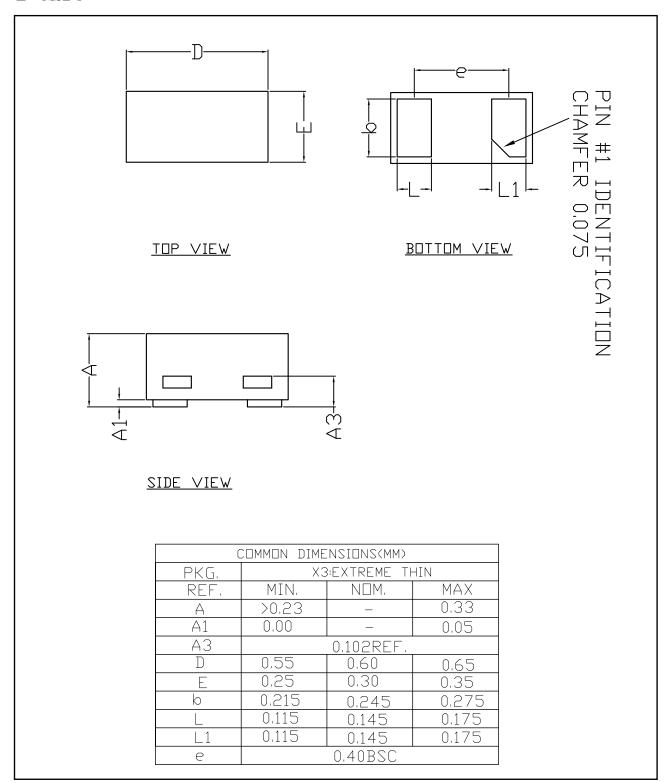
### **Recommended Mounting Pattern**





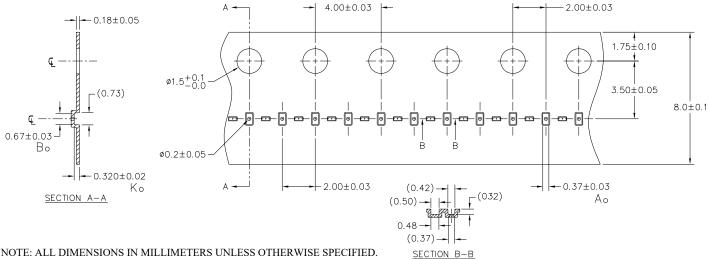
## **Package Outline**

- ☐ DFN0603 package
- ☐ 2 leads
- ☐ MSL-1





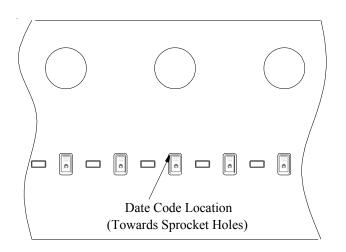
## **Carries Tape Specification**



NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

A0	В0	K0
0.37 +/-0.03	0.67 +/-0.03	0.32 +/-0.02 mm

Note: All dimensions in mm unless otherwise specified



**Device Orientation in Tape** 

## **Marking Codes**

# **Ordering Information**

Part Number	Qty per Reel	Reel Size
TT0541SA	10, 000	7 inch

#### Note:

(1) "2S" is part number, fixed