

## GENERAL DESCRIPTION

OB3639A is an offline LED lighting controller with high power factor, low THD and high constant current (CC) precision. It can achieve low system cost for an isolated lighting application by primary side control in a single stage converter. It significantly simplifies the LED lighting system design by eliminating the secondary side feedback components and the opto-coupler.

The proprietary CC control is used and the system can achieve high power factor with constant on-time control. Quasi-resonant (QR) operation and clamping frequency greatly improve the system efficiency. The advanced start-up technology is used to meet the start-up time requirement (<0.5s). The constant output current is compensated for tolerance of transformer inductance variation. And the line compensation and load compensation are built in OB3639A for high precisely constant output current control.

OB3639A offers comprehensive protection coverage with auto-recovery features including programmable VIN foldback, programmable VIN OVP, programmable thermal foldback, LED open loop protection, LED short circuit protection, cycle-by-cycle current limiting, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

OB3639A is offered in SOP-8 package.

## FEATURES

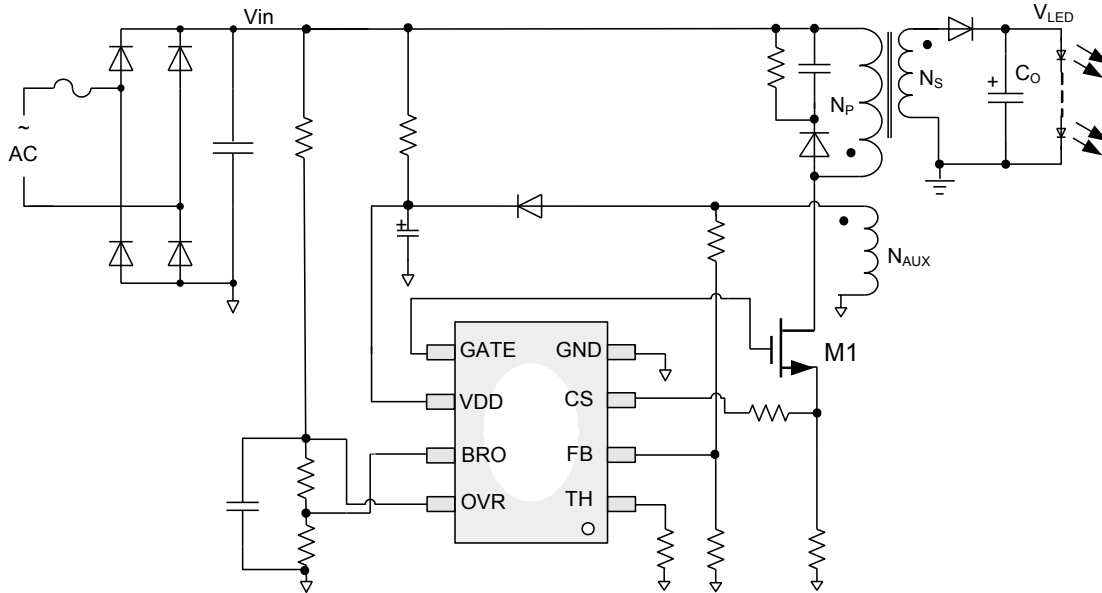
- High PF (>0.9)
- Low THD (<10%)
- Programmable VIN foldback
- Programmable VIN OVP
- Programmable thermal foldback
- High precision constant current
- Fast start-up (<0.5s)
- Low system cost and high efficiency
- Quasi-resonant operation
- Programmable CC regulation
- Built-in line/load compensation
- LED short circuit protection
- LED open loop protection
- Cycle-by-cycle current limiting
- VDD over voltage protection
- Up to 80W application

## APPLICATIONS

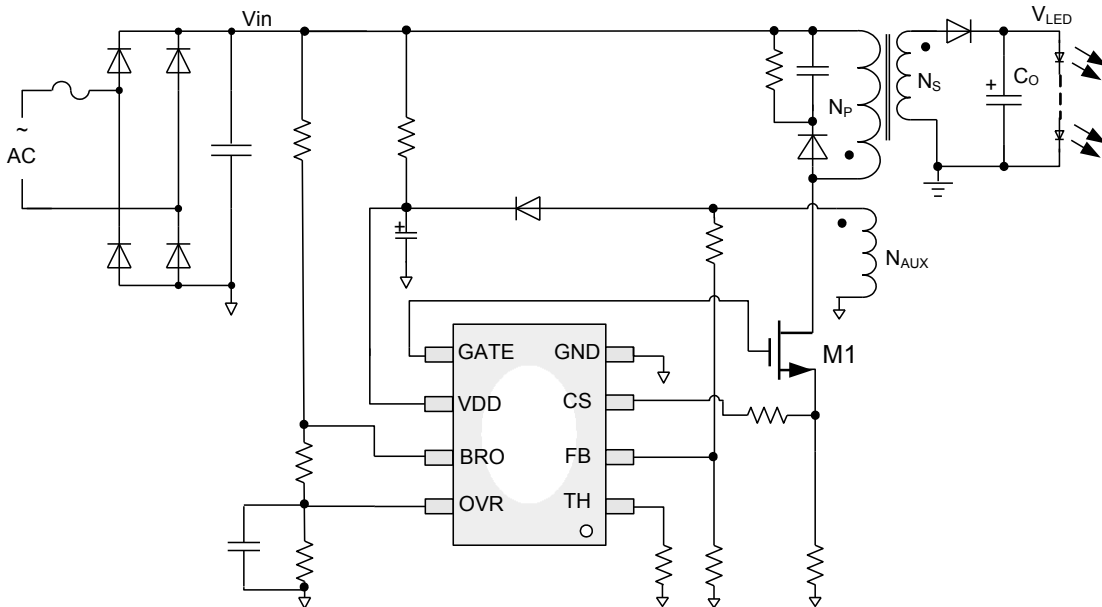
- LED lighting

**TYPICAL APPLICATION**

**Application Schematic 1:**  $V_{in\_ovr\_min}/V_{in\_bro} \leq 3.4$



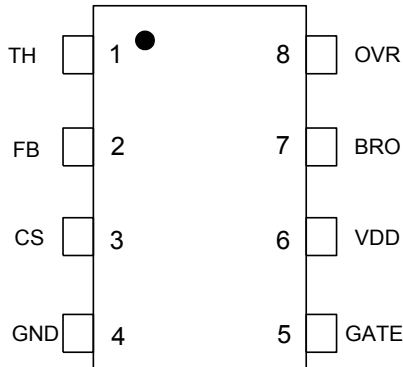
**Application Schematic 2:**  $V_{in\_ovr\_min}/V_{in\_bro} \geq 3.4$



### GENERAL INFORMATION

#### Pin Configuration

The pin map is shown as below for SOP8.



#### Ordering Information

Part Number	Description
OB3639ACP	SOP8, Halogen-free in Tube
OB3639ACPA	SOP8, Halogen-free in T&R

**Note:** All Devices are offered in Halogen-free Package if not otherwise noted.

#### Package Dissipation Rating

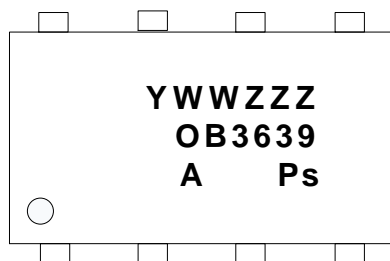
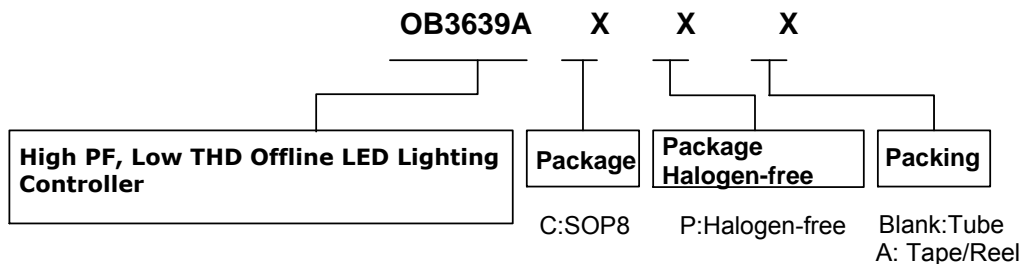
Package	R $\theta$ JA (°C/W)
SOP8	150

#### Absolute Maximum Ratings

Parameter	Value
VDD Voltage	-0.3 to 40V
Gate Voltage	-0.3 to 40V
CS Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
TH Voltage	-0.3 to 7V
BRO Input Voltage	-0.3 to 7V
OVR Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>j</sub>	-40 to 150 °C
Min/Max Storage Temperature T <sub>stg</sub>	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

### Marking Information

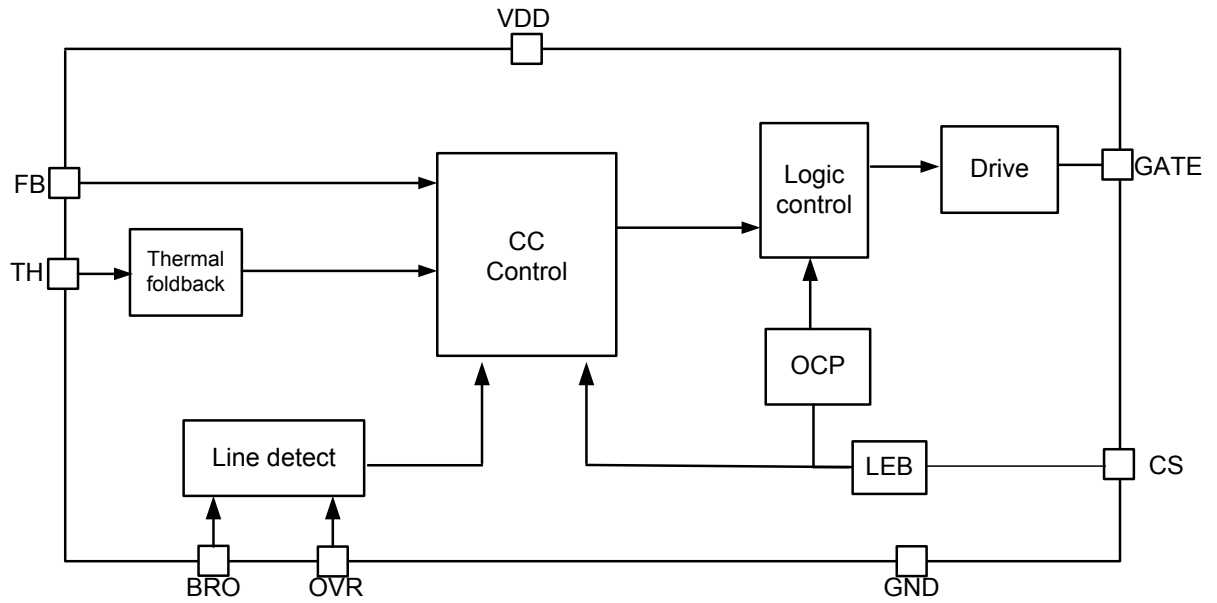


Y: Year Code  
 WW: Week Code (01-52)  
 ZZZ:Lot Code  
 P:Halogen-free Package  
 A:Character Code  
 S: Internal Code(Optional)

**TERMINAL ASSIGNMENTS**

Pin Num	Pin Name	I/O	Description
1	TH	O	Programmable thermal foldback
2	FB	I	Voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
3	CS	I	Current sensing terminal.
4	GND	P	Power Ground.
5	GATE	O	Gate driver output for power MOSFET.
6	VDD	P	Power supply Input.
7	BRO	I	Programmable Vin foldback
8	OVR	I	Programmable line OVP

**BLOCK DIAGRAM**

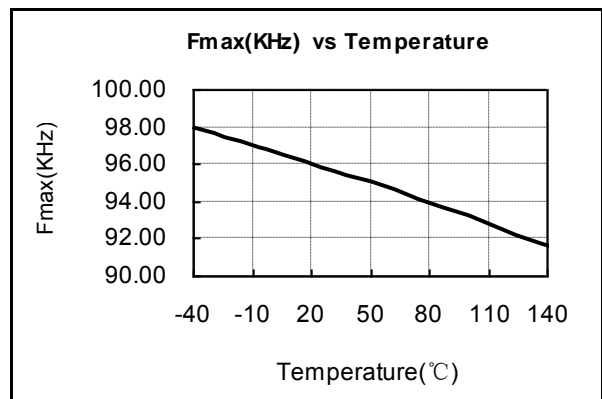
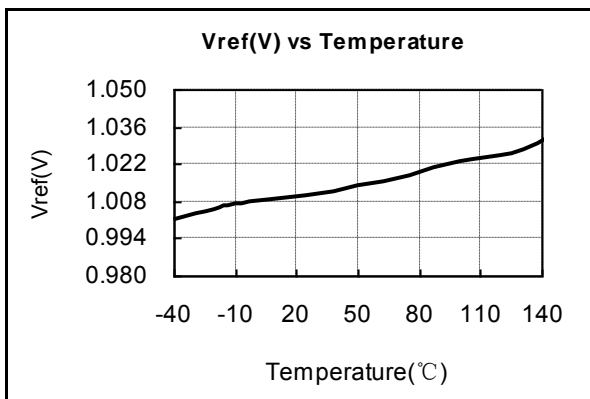
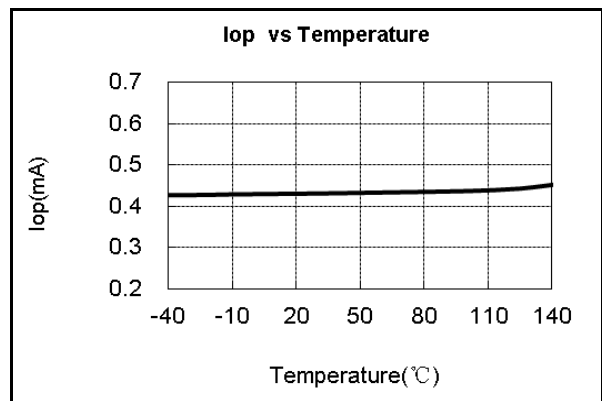
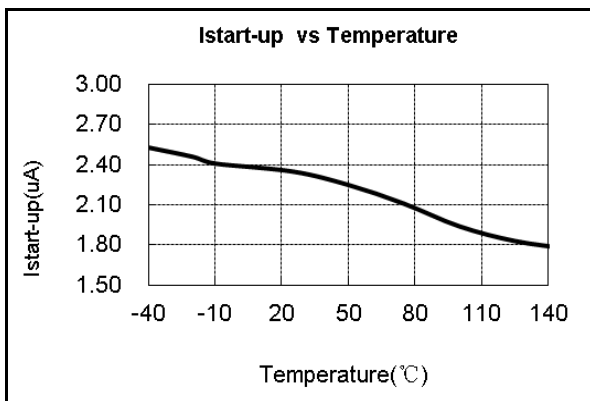
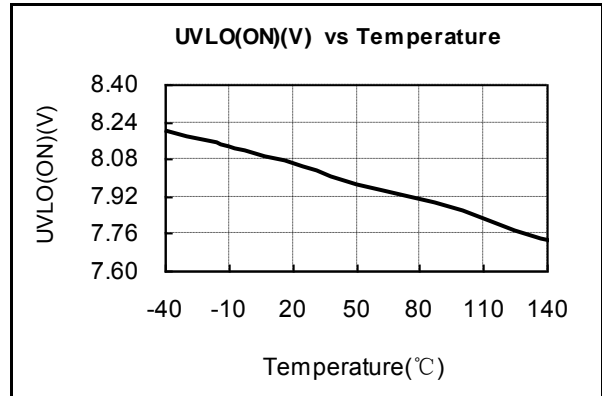
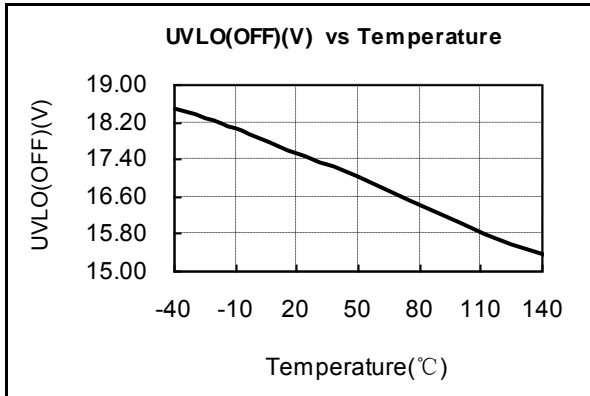


### ELECTRICAL CHARACTERISTICS

(TA = 25°C, VDD=20V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
<b>Supply Voltage (VDD) Section</b>						
I <sub>start-up</sub>	Start up current	VDD=UVLO(OFF)-1V		3	7	uA
I <sub>op</sub>	Operation current	VDD=20V, no loading		0.4	0.6	mA
UVLO(OFF)	VDD under voltage lockout exit		16	18	20	V
UVLO(ON)	VDD under voltage lockout enter		7	8	9	V
VDD_clamp	VDD clamp	IDD=2mA	24	26	28	V
VDD_OVP	VDD Over Voltage Protection		25	27	29	V
<b>Current Sense Input Section</b>						
TLEB	Lead Edge Blanking time			0.4		us
V <sub>th_ocp</sub>	Over Current Threshold	FB>0.45V	1.05	1.1	1.15	V
		FB<=0.45V		0.5		V
<b>FB Input Section</b>						
V <sub>out_ovp</sub>	Output Over Voltage Protection		3.325	3.5	3.675	V
V <sub>out_scp</sub>	Output Short Circuit Protection			0.45		V
I <sub>FB</sub>	Maximum Sink current from FB				4	mA
<b>QR Section</b>						
F <sub>max</sub>	Maximum Clamping Frequency			150		KHz
T <sub>off_max</sub>	Maximum Off Time			70		us
T <sub>off_min</sub>	Minimum Off Time	CS>0.15V		2		us
		CS<=0.15V		0.5		us
T <sub>on_max</sub>	Maximum On Time			25		us
<b>Error Amplifier Section</b>						
V <sub>ref</sub>	Error Amplifier Reference Voltage		0.196	0.200	0.204	V
<b>Gate Driver Section</b>						
V <sub>ol</sub>	Output Low Level	I <sub>out</sub> =10mA			1	V
V <sub>oh</sub>	Output High Level	I <sub>out</sub> =10mA	6			V
V <sub>clamp</sub>	Output Clamping Voltage			12		V
T <sub>r</sub>	Rising Edge Time	CL=1nF, VDD=16V		80	150	ns
T <sub>f</sub>	Falling Edge Time	CL=1nF, VDD=16V		30	70	ns
<b>Thermal foldback section</b>						
Th1	RTH=0R (VTH<1V)			155		°C
Th2	RTH=91K (VTH 1~2V)			110		°C
Th3	RTH=180K (VTH 2~4.0V)			100		°C
Th4	TH floating(VTH >4.0V)			90		°C
<b>Protection Reference Section</b>						
V <sub>ref_vin_fb</sub>	Threshold voltage of Vin foldback			0.8		V
V <sub>ref_ovp</sub>	Line OVP threshold voltage		2.72	2.8	2.88	V
V <sub>ref_ovp_hy</sub>	Hysteresis			100		mV

**CHARACTERIZATION PLOTS**



### OPERATION DESCRIPTION

OB3639A is a primary-side-control and high power factor, low THD fly-back PWM controller specialized for LED lighting application. It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. OB3639A works at Quasi-Resonant operation with maximum working frequency clamping, which can improve the efficiency of LED lighting system design.

#### Start up Control

The advanced start-up technology is used in OB3639A to meet the start-up time requirement (<0.5s). Low start-up current is designed in OB3639A so that VDD could be charged up above UVLO threshold with small charging current.

At the startup, OB3639A operates at open loop and over-current protection is set cycle-by-cycle until it senses the output voltage by FB pin up to about 1.6V. After that OB3639A operates in close loop and the transconductance of error amplifier is set to 1uS (typical).

#### LED Constant Current Regulation

The LED output current equals to the average of the output rectifier diode current. So the LED output current is related with the transformer peak current value and the transformer current discharge time. The transformer current discharge time is sensed through FB pin and the transformer peak current value is determined by internal reference voltage. A proprietary CC control block calculates LED output current through the CS pin peak current value and the transformer current discharge time. The output of the calculation is compared with an internal precise reference to generate an error voltage, which determines the turn-on time in voltage mode control. The LED output current can be approximated as:

$$I_{LED} = \eta \cdot \frac{N}{2} \cdot \frac{V_{ref}}{R_{CS}}$$

$\eta$  — The transformer coupling coefficient.

N — Turn ratio of primary side winding to secondary side winding.

Rcs — The sensing resistor connected between the MOSFET source and GND.

Vref — Internal reference voltage.

#### PFC and THD

The duration of the turn on period  $t_{on}$  is generated and keeps constant by patented control method. In a fly-back topology, constant turn on time and quasi-resonant operation provide high power factor (PF) and low total harmonic distortion (THD).

#### Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting (OCP) is offered in OB3639A. The switching current is detected by a sense resistor connected between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filter is no longer required. The current limit comparator is disabled at this blanking time and thus the external MOSFET cannot be turned off during this blanking time.

#### Quasi-Resonant Operation

OB3639A performs quasi-resonant detection through FB pin by monitoring the voltage activity on the auxiliary windings in series with external resistors. When the stored energy of fly-back transformer is fully released to the output, the voltage at FB pin decreases. When FB pin voltage falls below 0.05V (typical), an internal FB comparator is triggered and a new PWM switching cycle is initiated following the FB triggering.

#### Line/Load Compensation

OB3639A provides internal line compensation and load compensation to avoid using outside sensing devices. The compensated voltage is added to CS voltage cycle-by-cycle and LED output current is kept constant under different line voltage and output voltage.

#### VDD Over Voltage Protection

VDD is supplied with transformer auxiliary winding output. When VDD is higher than 27V (typical), VDD OVP protection is triggered and GATE is shut down, and the device enters power on startup sequence thereafter.

#### LED Short Circuit Protection

When LED string is short, the positive plateau of auxiliary winding voltage is also near zero and the FB voltage is low. If the voltage at FB pin is lower than a threshold of approximately 0.25V (typical), the IC will work at minimum frequency and the threshold voltage of OCP is reduced to 0.5V (typical). The power dissipation is greatly reduced in this way.

#### LED Open Circuit Protection

When the LED string open circuit happens, the positive plateau of auxiliary winding voltage increases and the FB pin voltage is high. If the voltage at FB pin is higher than a threshold of approximately 3.5V (typical), the IC will shut down and enter power on startup sequence thereafter.



**Gate Driver**

The GATE pin is connected to the gate of an external power switch. An internal 12V (typical) clamp is added for MOSFET gate protection at high VDD voltage. When VDD voltage drops below UVLO (ON), the GATE pin is internally pulled low to maintain the off state.

**Programmable thermal foldback**

Thermal foldback point could be set by adjusting the resistor from TH pin to GND as the following table:

TH pin setting	Thermal foldback point
RTH=0ohm	155°C
RTH=91Kohm	110°C
RTH=180Kohm	100°C
TH pin floating	90°C

**Programmable VIN foldback**

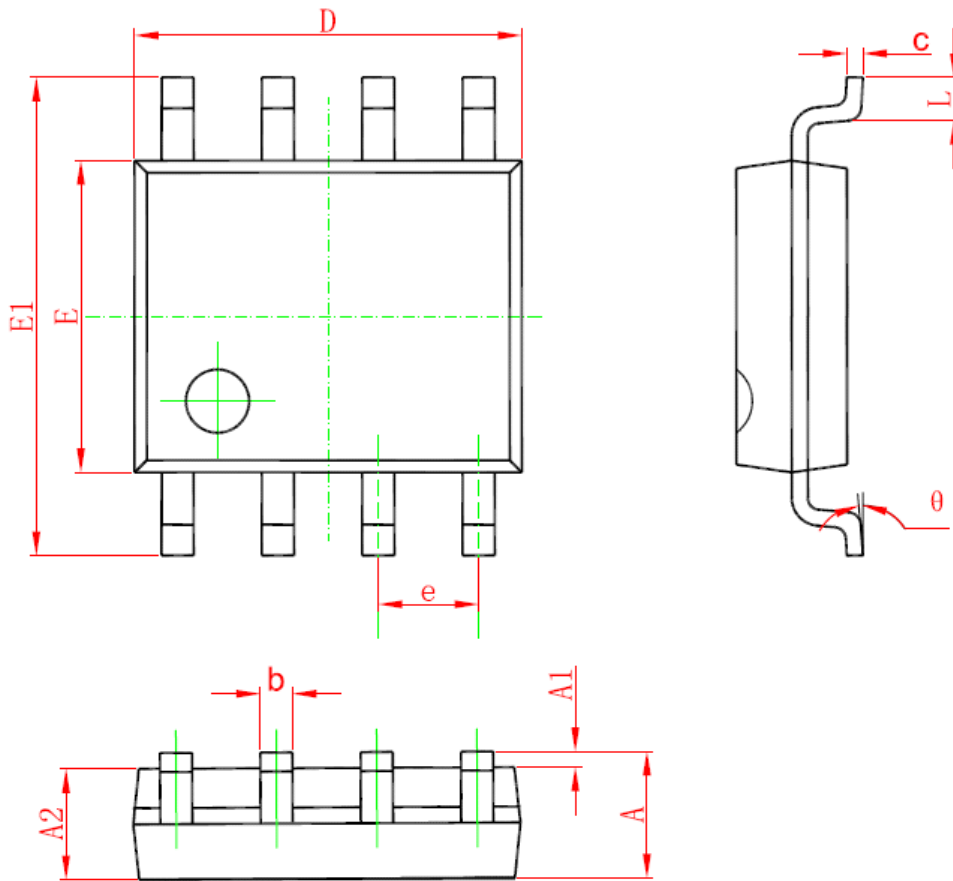
Line voltage is detected by resistor divider from BRO pin. When the detected voltage from BRO pin is lower than 0.8V (typical), the output current will decrease as line voltage gets low.

**Programmable line OVP**

Line voltage is also detected by the resistor divider from OVR pin. When the detected voltage from OVR is larger than 2.8V (typical), line voltage over voltage protection is triggered and the switching of system will stop.

**PACKAGE MECHANICAL DATA**

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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