



20N60-HCQ

Preliminary

Power MOSFET

20A, 600V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **20N60-HCQ** is a N-channel enhancement MOSFET using UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$, high switching speed, high current capacity and low gate charge.

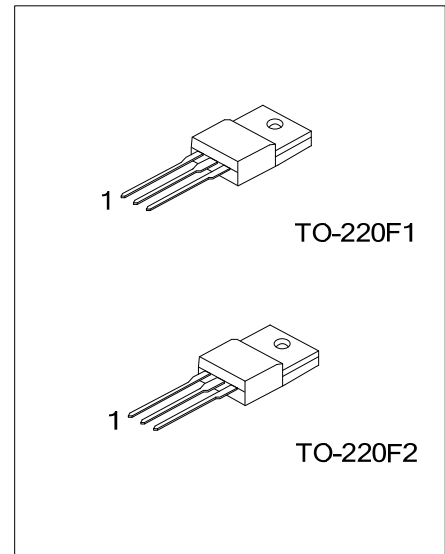
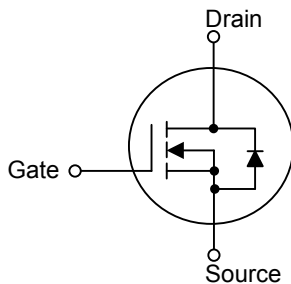
The UTC **20N60-HCQ** is universally applied in low voltage such as automotive, high efficiency switching for AC/DC converters and DC motor control, etc.

FEATURES

* $R_{DS(ON)} \leq 0.5 \Omega @ V_{GS}=10V, I_D=10A$

* High Switching Speed

SYMBOL



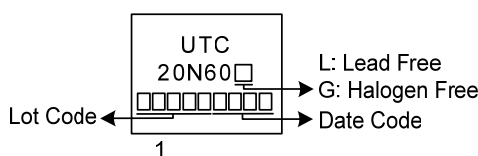
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
20N60L-TF1-T	20N60G-TF1-T	TO-220F1	G	D	S	Tube
20N60L-TF2-T	20N60G-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>20N60G-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1, TF2: TO-220F2</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	± 30	V
Continuous Drain Current	Continuous	I_D	20	A
	Pulsed	I_{DM}	40	A
Single Pulsed Avalanche Energy		E_{AS}	479	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.6	V/ns
Power Dissipation		P_D	48	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating : Pulse width limited by maximum junction temperature.
 3. $L=10\text{mH}$, $I_{AS}=9.7\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$
 4. $I_{SD} \leq 20\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

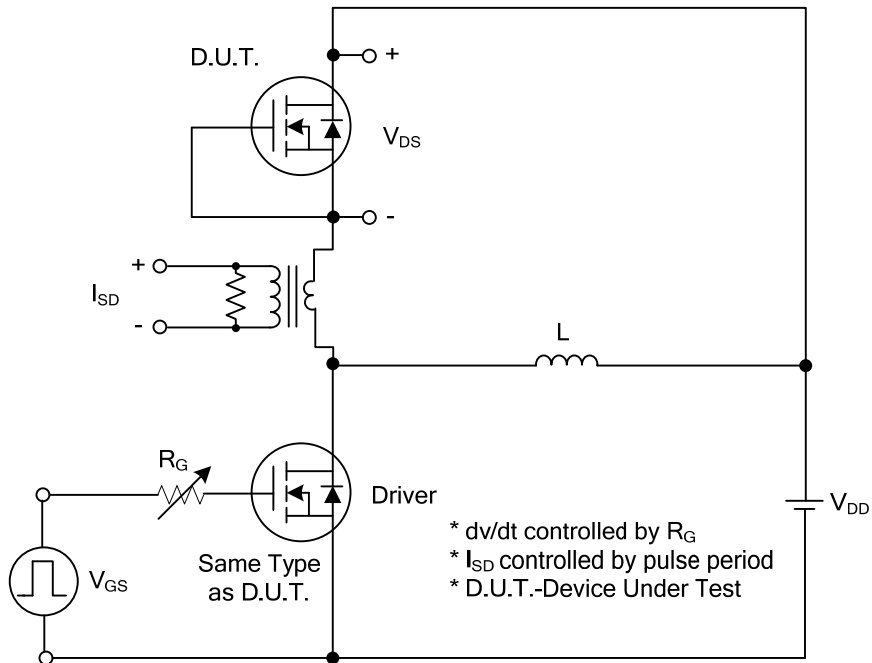
PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.6	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

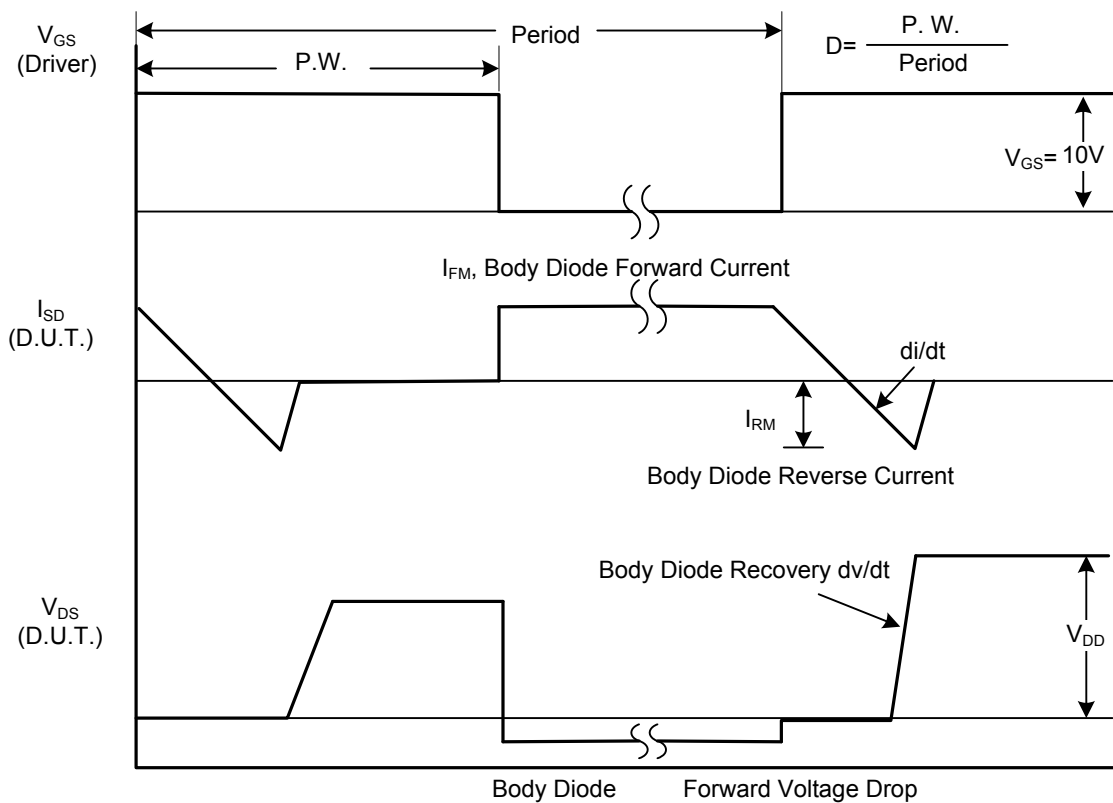
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	600			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=10\text{A}$			0.5	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		2905		pF
Output Capacitance	C_{OSS}			258		pF
Reverse Transfer Capacitance	C_{RSS}			14		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		65		nC
Gate to Source Charge	Q_{GS}			20		nC
Gate to Drain Charge	Q_{GD}			19		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$, $R_G=25\Omega$ (Note 1, 2)		40		ns
Rise Time	t_R			22		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			170		ns
Fall-Time	t_F			50		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				20	A
Maximum Body-Diode Pulsed Current	I_{SM}				40	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=20\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=20\text{A}$, $V_{GS}=0\text{V}$, $di_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		475		ns
Reverse Recovery Charge	Q_{rr}				17	

- Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

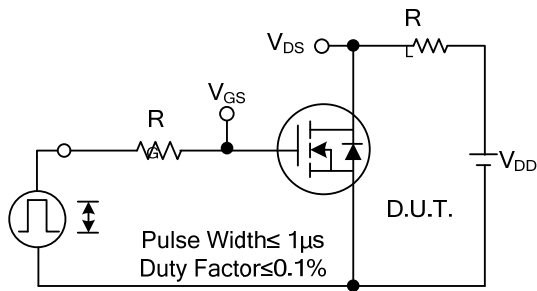


Peak Diode Recovery dv/dt Test Circuit

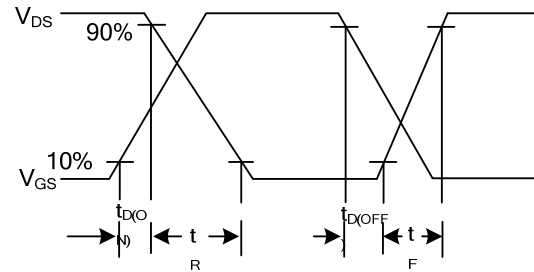


Peak Diode Recovery dv/dt Waveforms

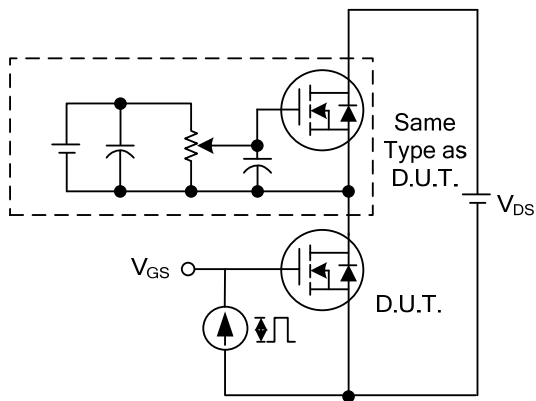
■ TEST CIRCUITS AND WAVEFORMS



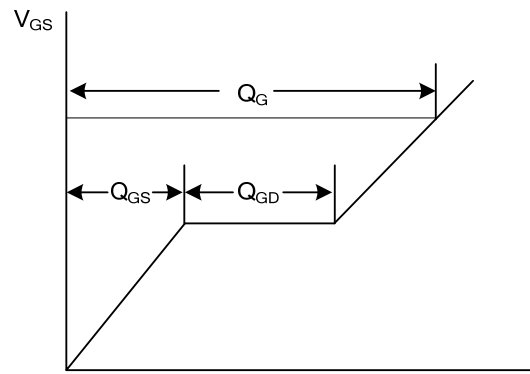
Switching Test Circuit



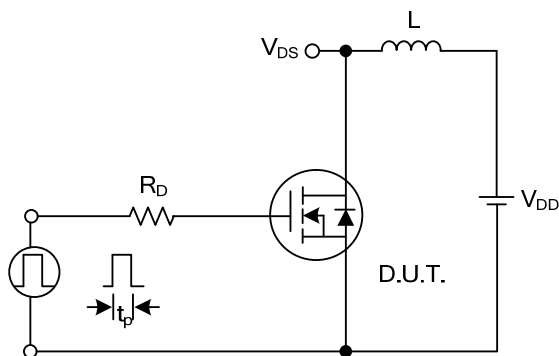
Switching Waveforms



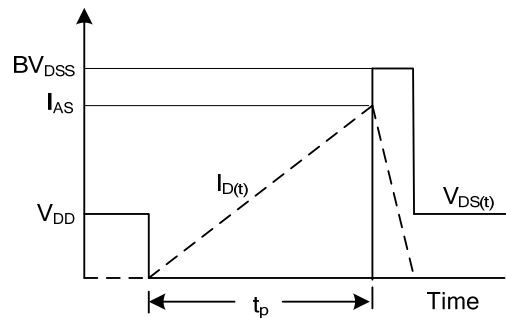
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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