

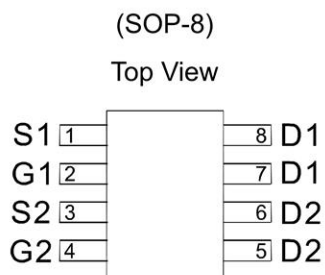
### GENERAL FEATURES

- $R_{DS(ON)} \leq 16 \text{ m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 20 \text{ m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

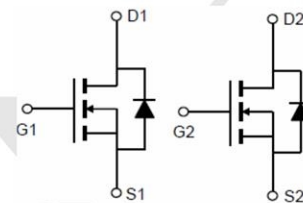
### Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### Package and Pin Configuration

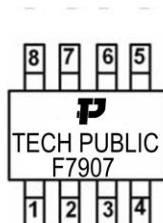


### Circuit diagram



Schematic diagram

### Marking:



### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

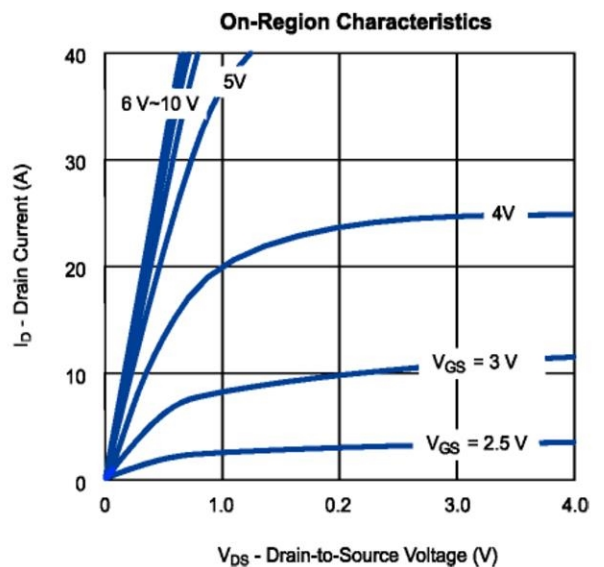
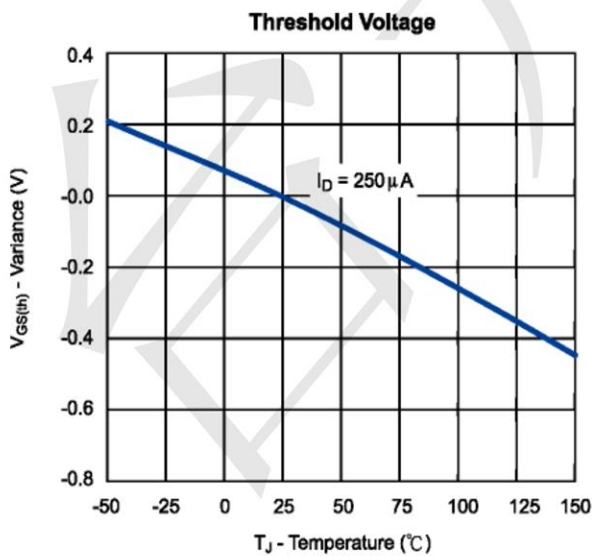
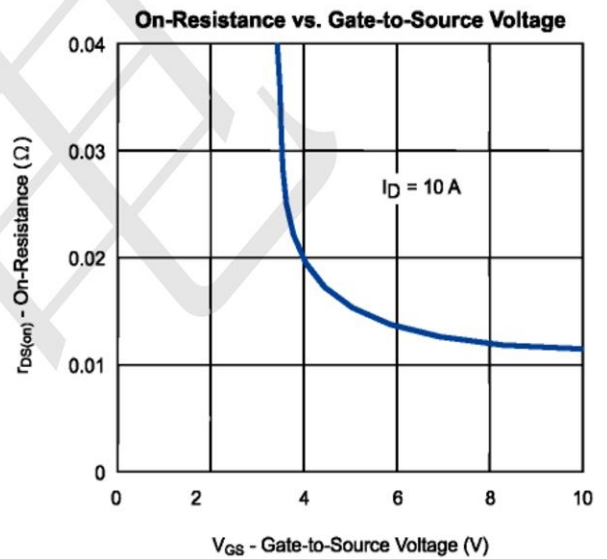
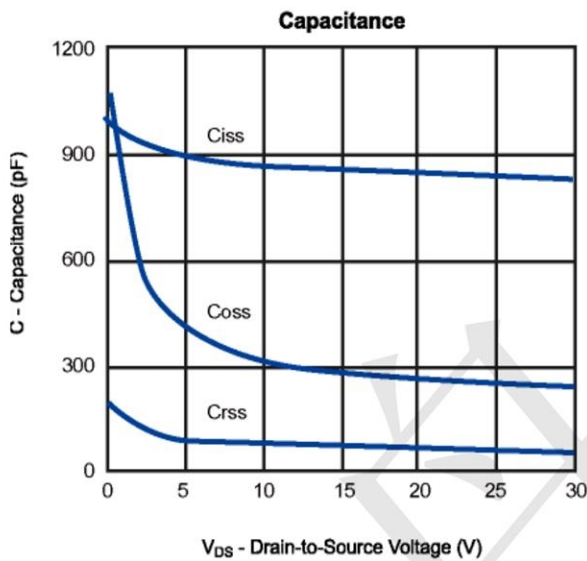
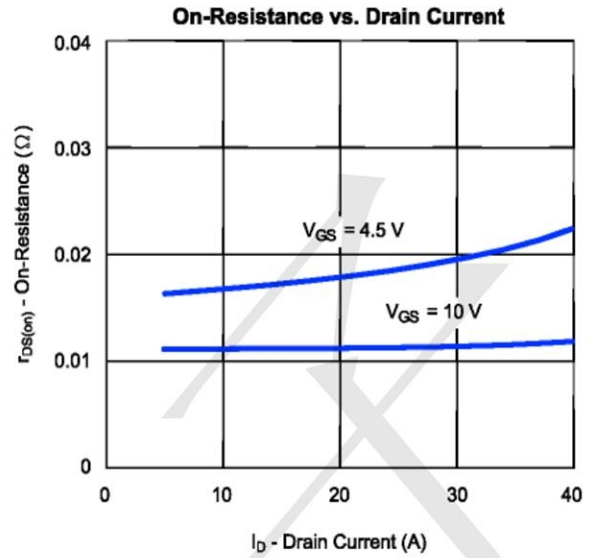
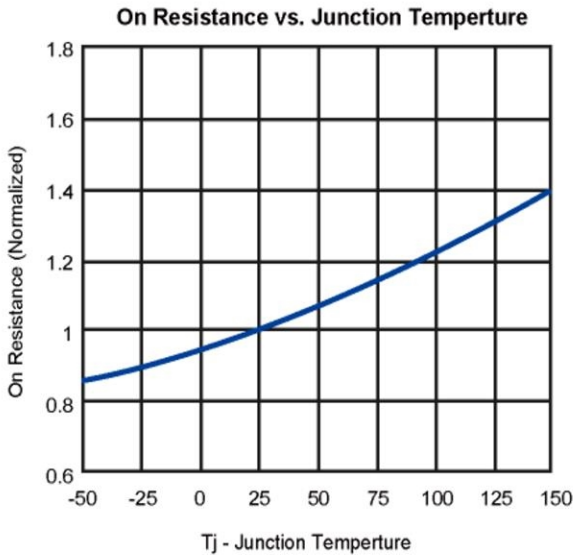
Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	10
		$T_A=70^\circ\text{C}$	8.3
Pulsed Drain Current	$I_{DM}$	38	A
Maximum Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.2
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	52.0	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** ( $T_A=25^\circ\text{C}$  Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1		3	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	$\mu A$
$R_{DS(ON)}$	Drain-Source On-Resistance <sup>a</sup>	$V_{GS}=10V, I_D=10A$		11.2	16	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$		15.6	20	
$V_{SD}$	Diode Forward Voltage	$I_S=8.2A, V_{GS}=0V$		0.8	1.2	V
<b>DYNAMIC</b>						
$R_g$	Gate Resistance	$f=1\text{MHz}$		1		$\Omega$
$Q_g$	Total Gate Charge	$V_{DS}=10V, V_{GS}=4.5V, I_D=8.2A$		9.5		nC
$Q_{gs}$	Post-V <sub>th</sub> Gate-Source Charge			3.6		
$Q_{gd}$	Gate-Drain Charge			3.4		
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$		841		pF
$C_{oss}$	Output Capacitance			250		
$C_{rss}$	Reverse Transfer Capacitance			71		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, R_L=15\ \Omega$ $I_D=1A, V_{GEN}=10V,$ $R_G=6\ \Omega$		14		ns
$t_r$	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			43		
$t_f$	Turn-Off Fall Time			4		

Notes: a. pulse test: pulse width  $\leq 300\ \mu s$ , duty cycle  $\leq 2\%$ , Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice





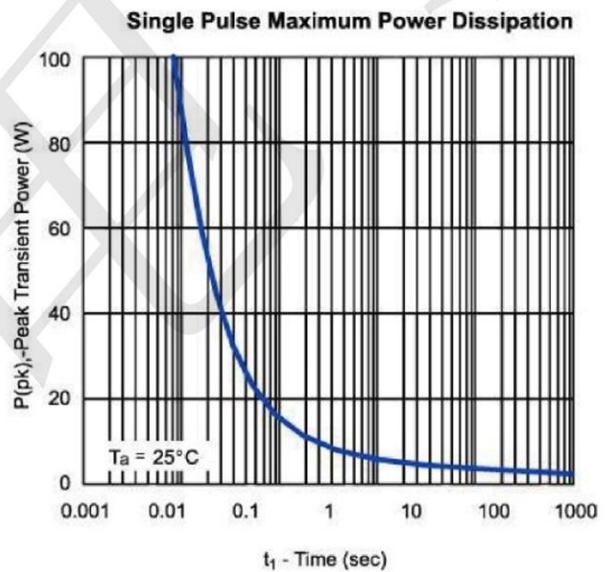
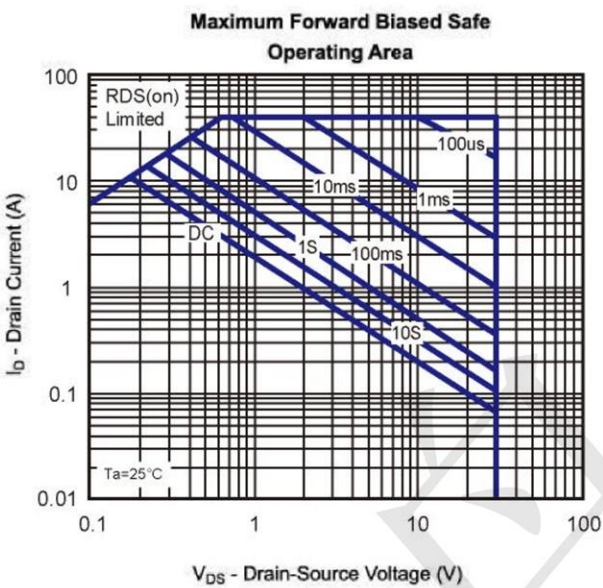
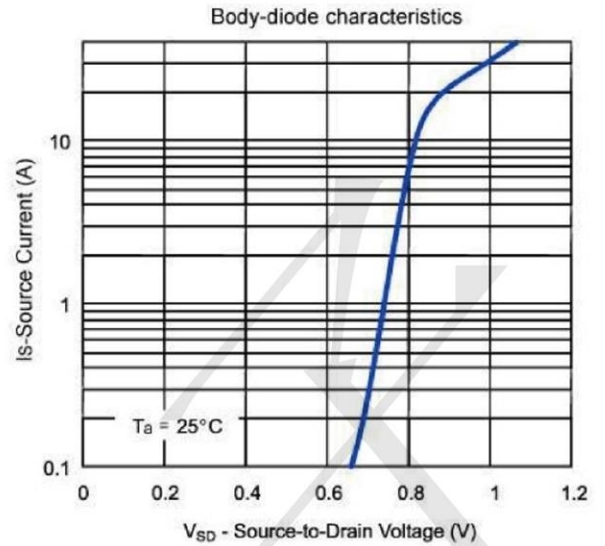
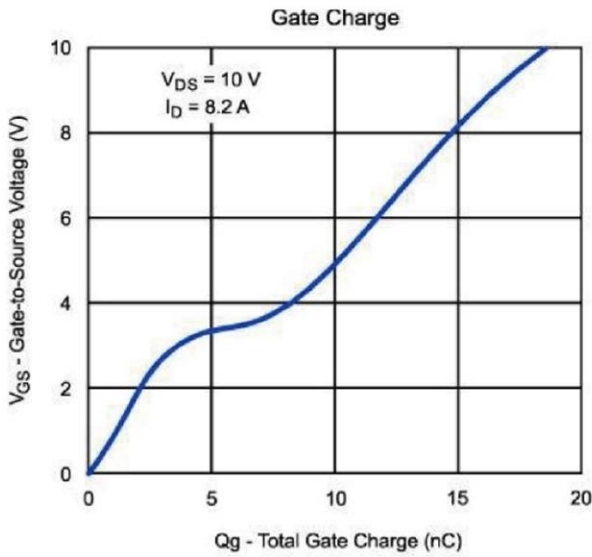
TECH PUBLIC

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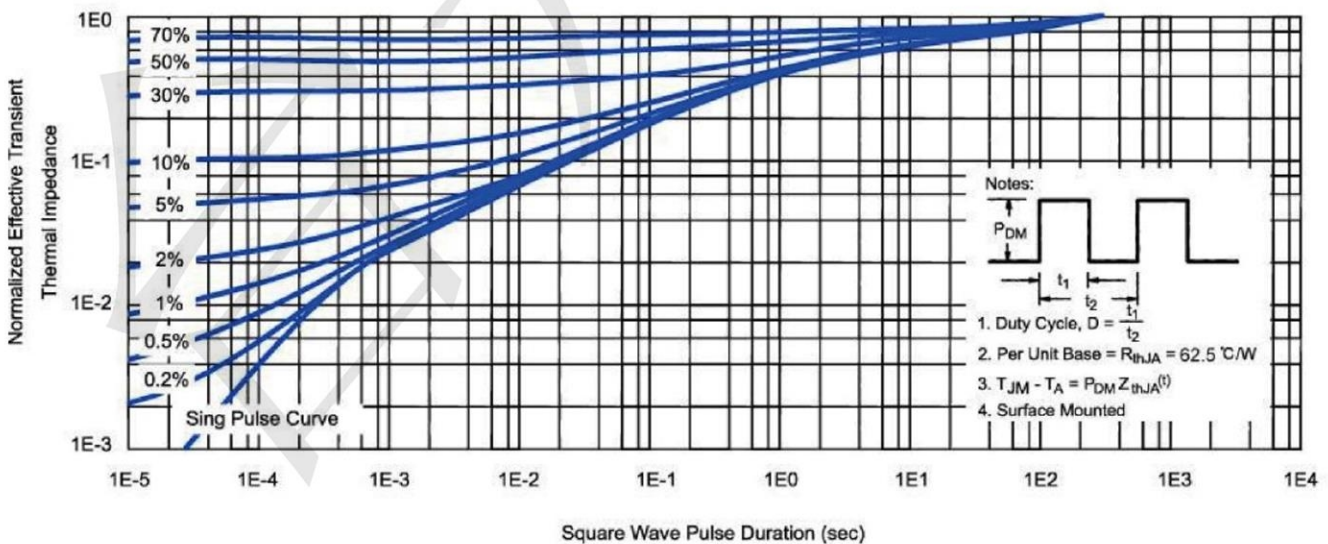
IRF7907TRPBF

Dual N-Channel Enhancement Mode Power MOSFET

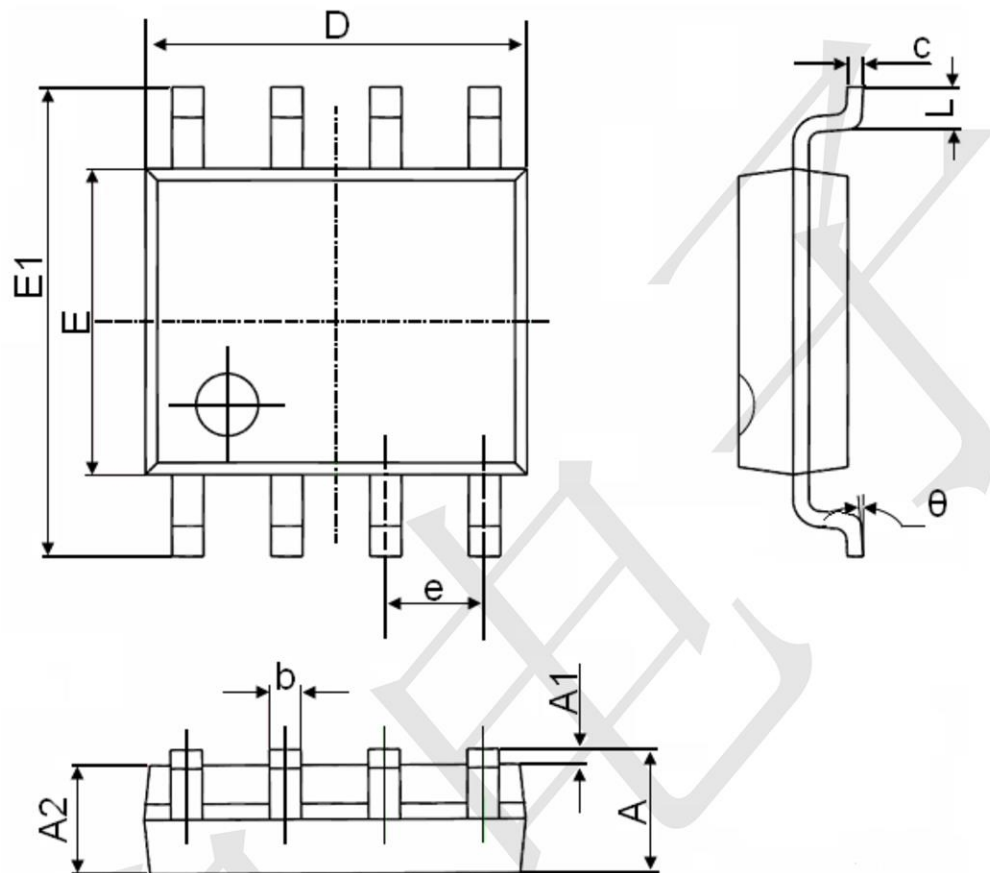
www.sot23.com.tw



Normalized Thermal Transient Impedance, Junction-to-Ambient



**SOP-8 Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°