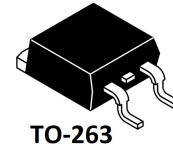
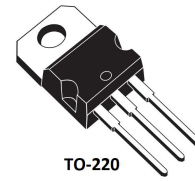


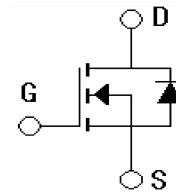
Features

- $V_{DS}=100V, I_D=120A$
 $R_{DS(on)}=6m\Omega @ V_{GS}=10V$
- High density cell design for ultra low R_{dson}
- Low gate charge
- Improved dv/dt capability
- RoHS product



Applications

- Power switching application
- Isolated DC/DC converters in Telecom and Industrial
- Synchronous Rectification in DC/DC Converters



Absolute Ratings ($T_C=25^\circ C$)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current-continuous	I_D	120	A
Drain Current-continuous ($T_C=100^\circ C$)	$I_D(T_C=100^\circ C)$	100	A
Drain Current-pulse (note 1)	I_{DM}	540	A
Single Pulsed Avalanche Energy (note 2)	E_{AS}	420	mJ
Maximum Power Dissipation	PD $T_C=25^\circ C$ Derate above $25^\circ C$	245	W
		2.0	W/ $^\circ C$
Operating and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

Electrical Characteristics($T_{CASE}=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Tests conditions	Min	Typ	Max	Units
Drain-Source Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On-Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{DS}=10V, I_D=20A$	-	6	6.8	m Ω
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=30A$ (note 4)	-	65	-	S
Gate resistance	R_g	$V_{ds}=0V$, Scan F mode		2.5		Ω
Dynamic Characteristics						
Input capacitance	C_{iss}	$V_{DS}=48V, V_{GS}=0V, f=100KHZ$	-	3525	-	pF
Output capacitance	C_{oss}		-	543	-	pF
Reverse transfer capacitance	C_{rss}		-	26	-	pF

Electrical Characteristics($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Tests conditions	Min	Typ	Max	Units
Switching-Characteristics						
Turn-On delay time	t _{d(on)}	V _{DD} =20V, I _D =-30A, R _G =3Ω V _{GS} =10V (note 4,5)	-	21	-	ns
Turn-On rise time	t _r		-	36	-	ns
Turn-Off delay time	t _{d(Off)}		-	44	-	ns
Turn-Off rise time	t _f		-	20	-	ns
Total Gate Charge	Q _g	V _{DS} =80V, I _D =30A, V _{GS} =10V (note 4,5)	-	54	-	nC
Gate-Source charge	Q _{gs}		-	17	-	nC
Gate-Drain charge	Q _{gd}		-	13	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain-Source Diode Forward Curret	V _{SD}	V _{GS} =0V, I _S =50A	-	-	1.4	V
Diode Forward Current	I _S	TC=25℃	-	-	120	A
Reverse recovery time	T _{rr}	I _S =30A, DI/DT=100A/ μ S	-	64	-	nS
Reverse recovery charge	Q _{rr}		-	135	-	nC

Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, junction to Case	$R_{th(j-C)}$	0.51	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{th(j-A)}$	47	$^{\circ}\text{C}/\text{W}$

Notes:

1. Pulse width limited by maximum junction temperature
2. $I_{AS}=41\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J=25^{\circ}\text{C}$
3. $I_{SD} \leq 30\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially independent of operating temperature

Electrical Characteristics

Fig. 1. On-state characteristics

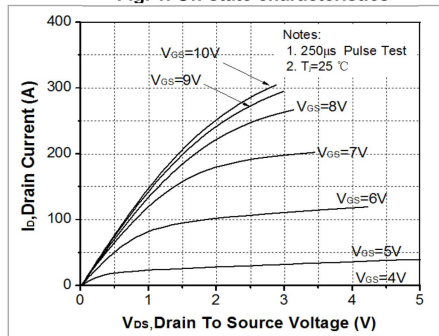


Fig. 2. Transfer Characteristics

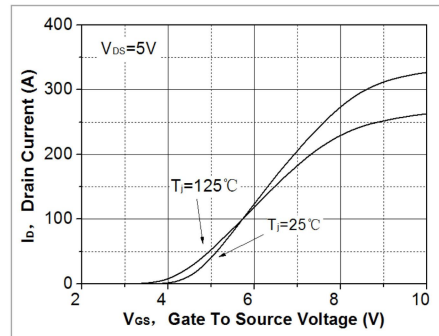


Fig. 3. On-resistance variation vs. drain current and gate voltage

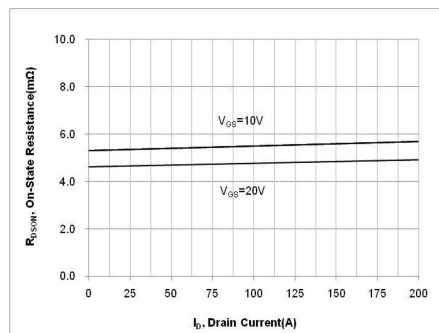


Fig. 4. On-state current vs. diode forward voltage

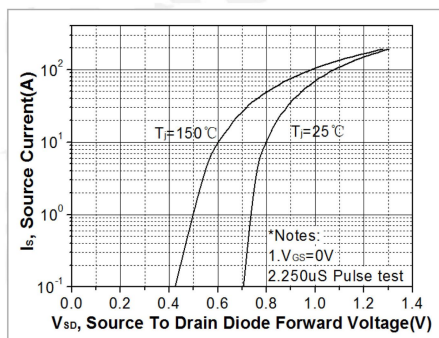


Fig 5. Breakdown voltage variation vs. junction temperature

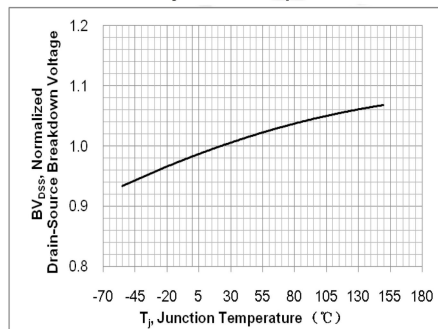


Fig. 6. On-resistance variation vs. junction temperature

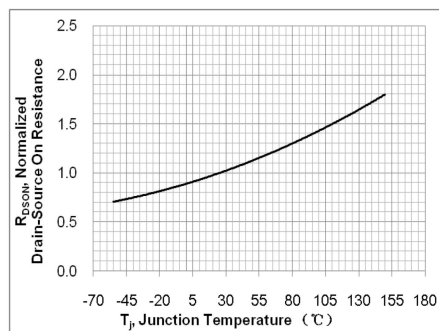


Fig. 7. Gate charge characteristics

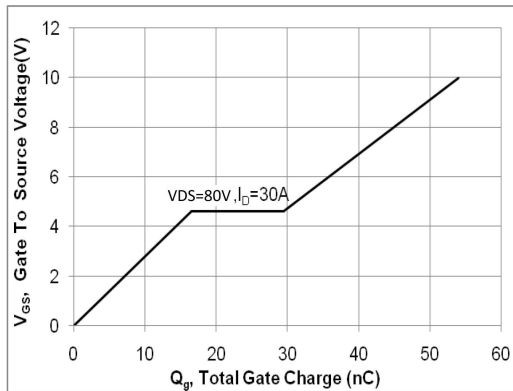


Fig. 8. Capacitance Characteristics

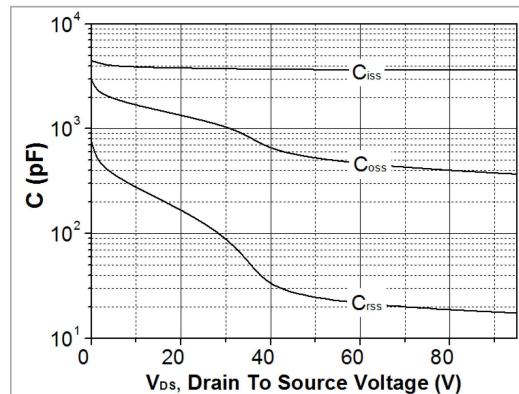


Fig. 9. Maximum safe operating area

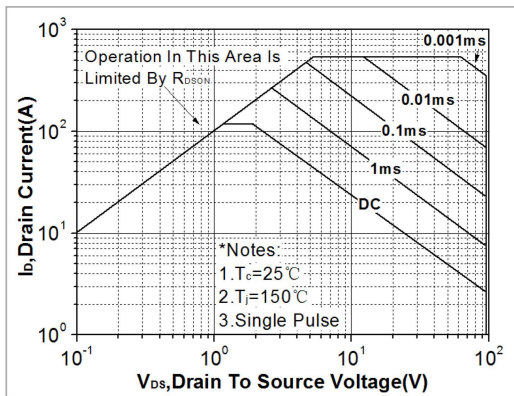


Fig. 10. Maximum drain current vs. case temperature

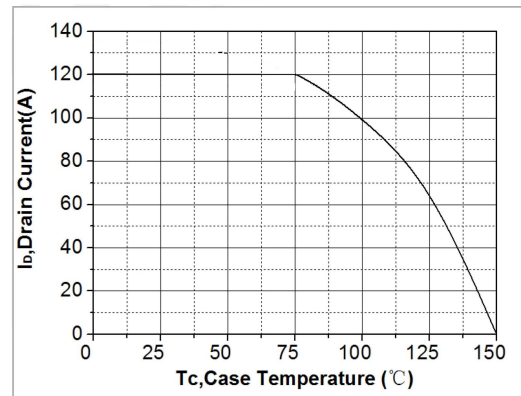


Fig. 11. Transient thermal response curve

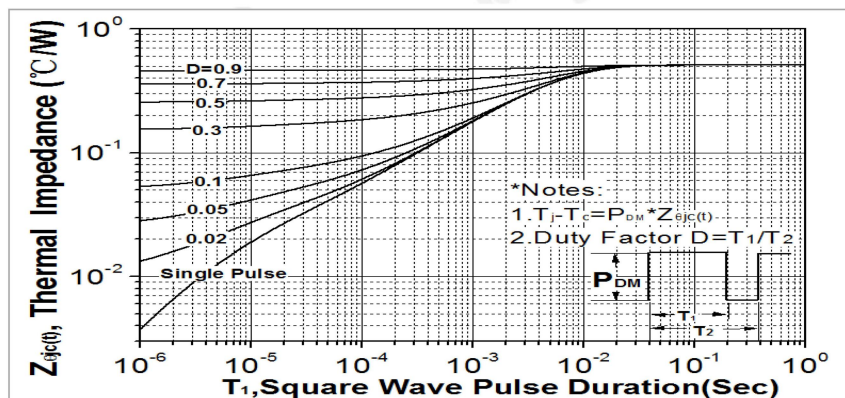


Fig. 12. Gate charge test circuit & waveform

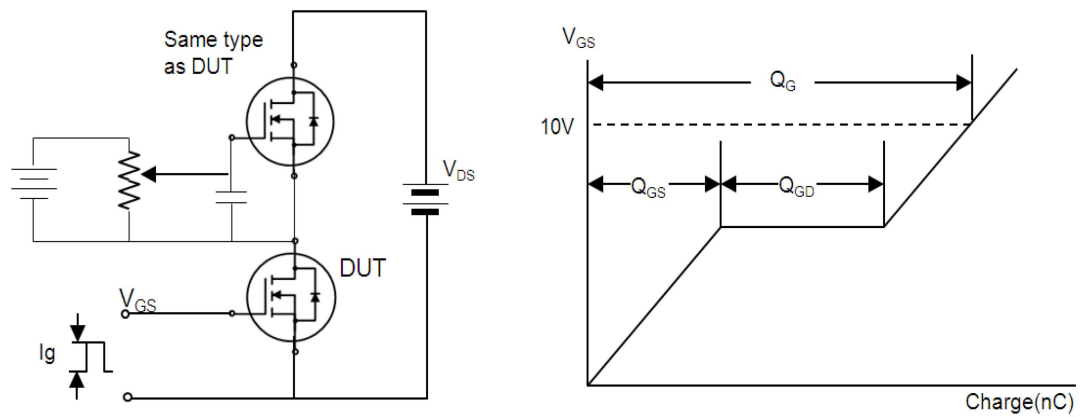


Fig. 13. Switching time test circuit & waveform

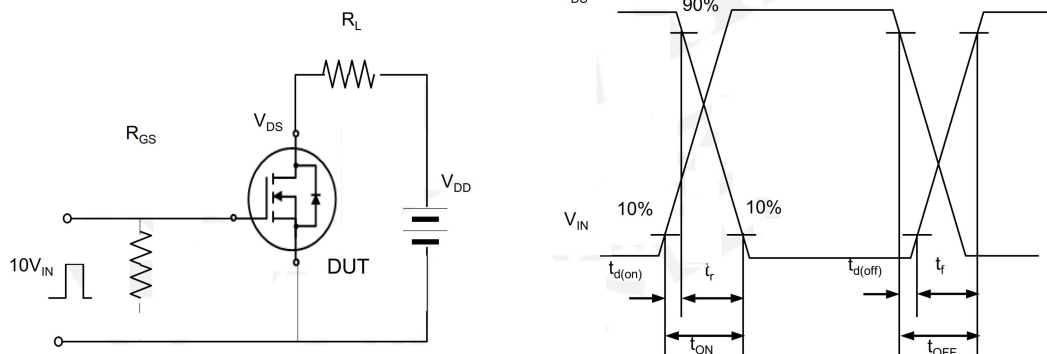


Fig. 14. Unclamped Inductive switching test circuit & waveform

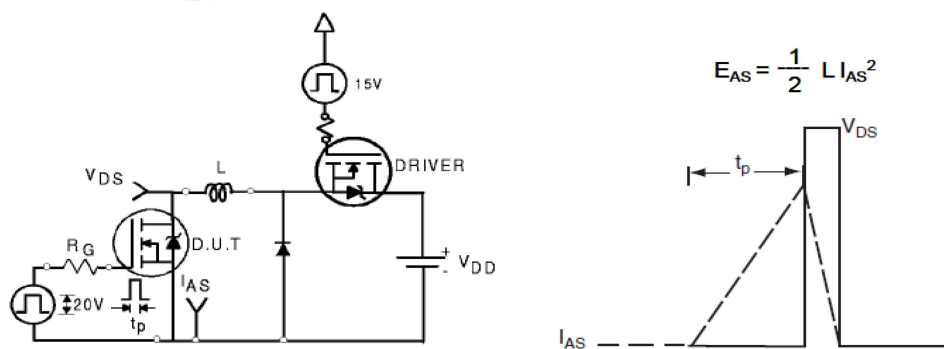
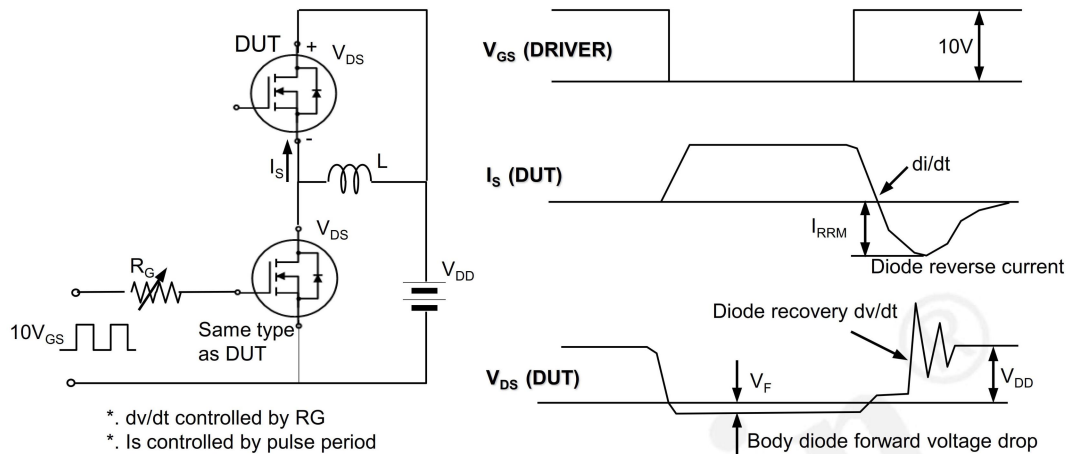


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



Package Mechanical DATA

