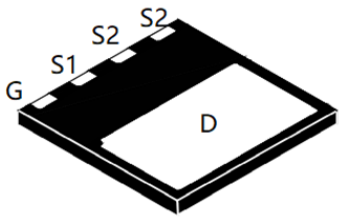
WCR250N65DV

Single N-Channel，650V，10A，Super Junction MOSFET

https://www.omnivision-group.com

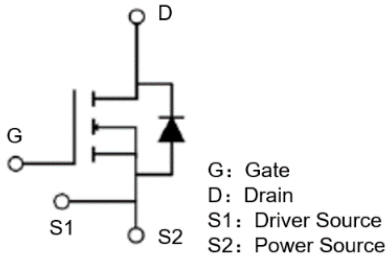
V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
650	255 @ V_{GS}=10V



DFN8X8-4L

Description

The WCR250N65DV is new generation of high voltage MOSFET that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance. This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. This device is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.



Internal schematic diagram

Features

- Extremely low gate charge
- 100% avalanche tested
- 100% Rg tested

DV = Special Code
Y = Year
W = Week(A~z)

Marking

Applications

- Switching applications

Order information

Device	Package	Shipping
WCR250N65DV	DFN8X8-4L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C=25°C	I_D	10	A
	T_C=100°C		6	A
Pulsed Drain Current [c]		I_{DM}	37	A
Avalanche Energy L=60mH		E_{AS}	270	mJ
Power Dissipation [b]	T_C=25°C	P_D	56	W
	T_C=100°C		22	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	19	24	°C/W
	Steady State		46	55	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	1.8	2.3	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area).

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

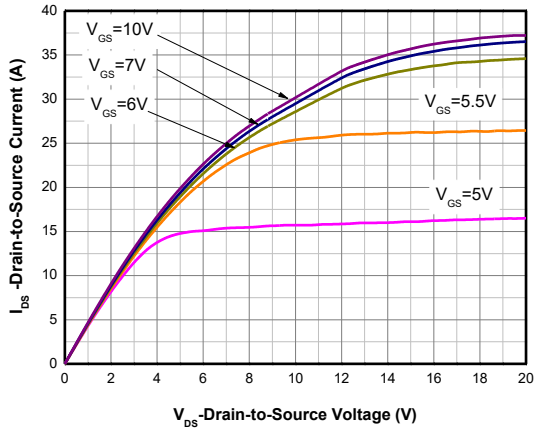
c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

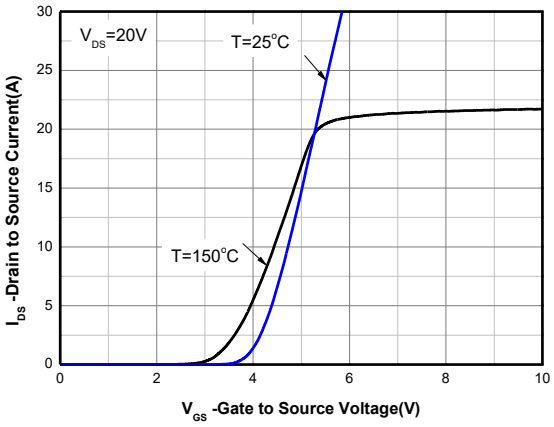
Electronics Characteristics (Ta=25ºC, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =650V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	2	3	4	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D =4.0A		220	255	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} =0 V, f = 1.0MHz, V_{DS} = 400 V		1202		pF
Output Capacitance	C_{OSS}			27		
Reverse Transfer Capacitance	C_{RSS}			1.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}=10V,V_{DD} = 400V, I_D = 13.8A		31		nC
Gate-to-Source Charge	Q_{GS}			7		
Gate-to-Drain Charge	Q_{GD}			11		
Gate Resistance	R_g	f=1MHz		5.8		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 10 V, V_{DD} = 400V, ID = 13.8A , R_G=10Ω		13		ns
Rise Time	tr			10		
Turn-Off Delay Time	td(OFF)			64		
Fall Time	tf			35		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S =4.0 A			1.5	V
Body-Diode Continuous Current	I_{SD}				8	A
Body-Diode Pulsed Current	I_{SDM}				37	A
Body Diode Reverse Recovery Time	Trr	IF=6.9A, V_{DS}=400V di/dt=100A/us		310		nS
Body Diode Reverse Recovery Charge	Qrr			2.8		uC
Peak reverse recovery Current	Irrm			17.9		A

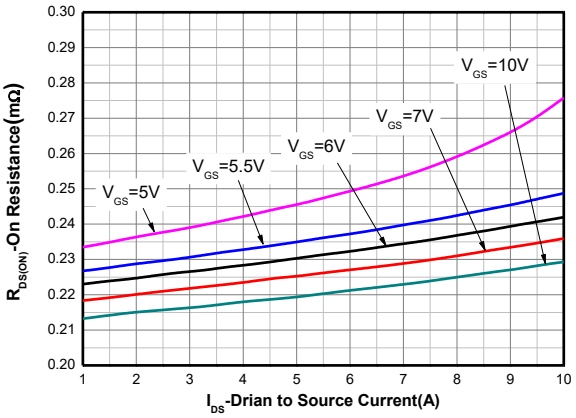
Typical Characteristics (Ta=25°C, unless otherwise noted)



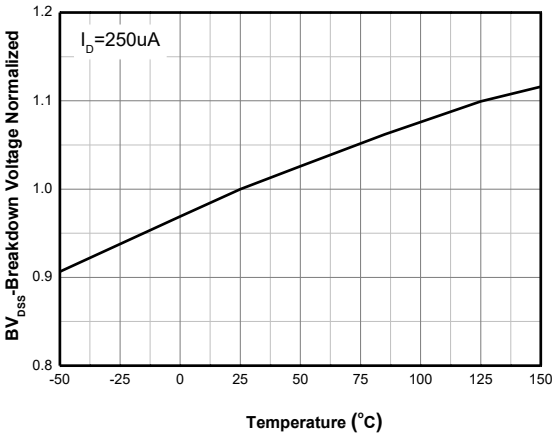
Output Characteristics [d]



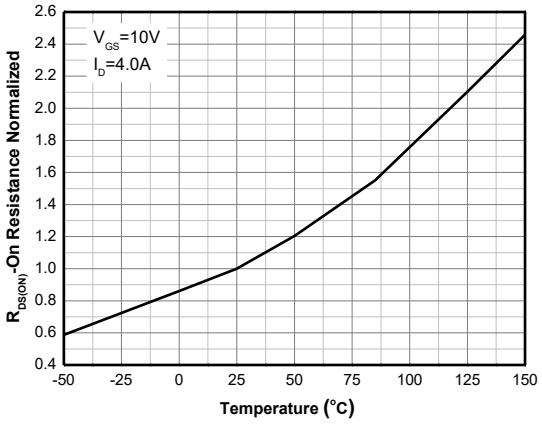
Transfer Characteristics [d]



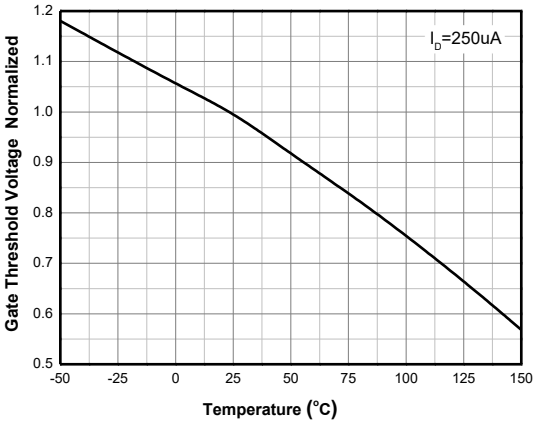
On-Resistance vs. Drain Current [d]



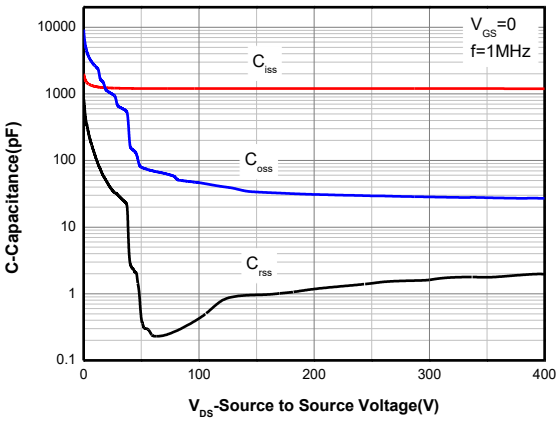
BVdss vs. Temperature [d]



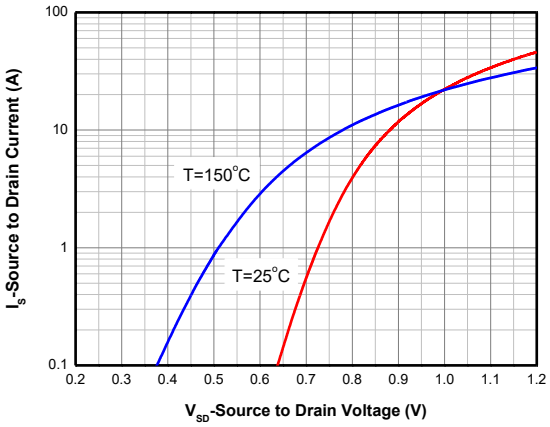
On-Resistance vs. Junction Temperature [d]



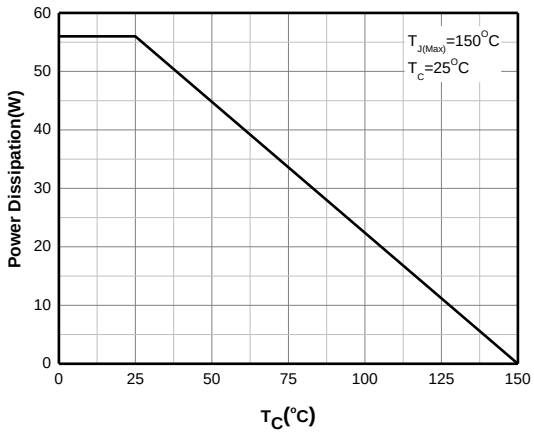
Threshold Voltage vs. Temperature



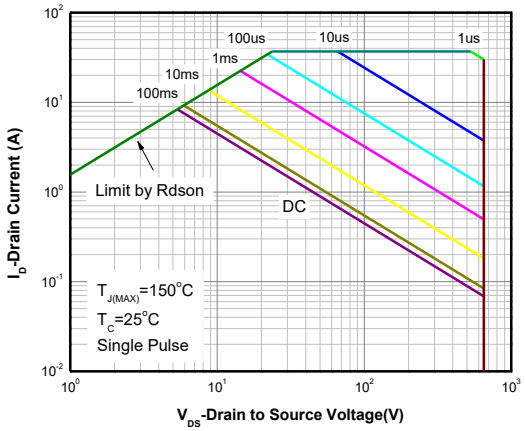
Capacitance



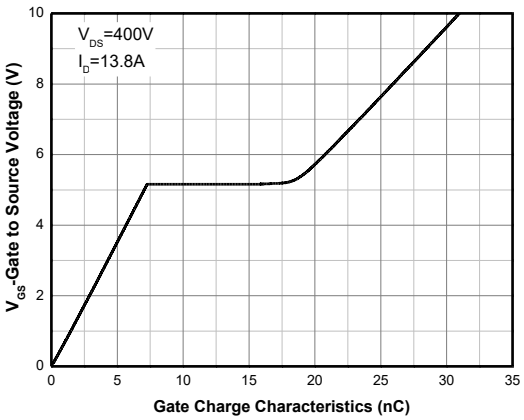
Body Diode Forward Voltage [d]



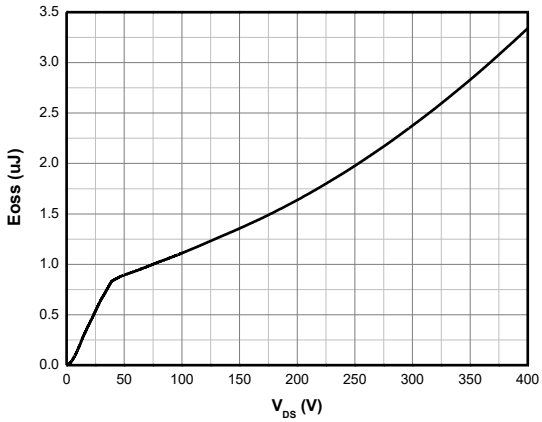
Power Dissipation



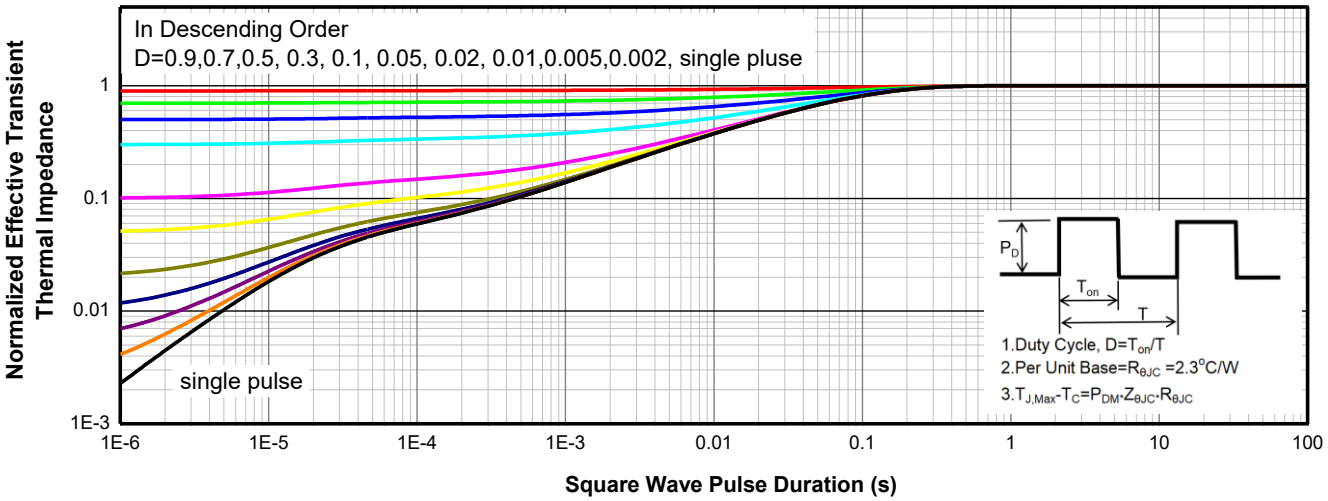
Safe Operating Area



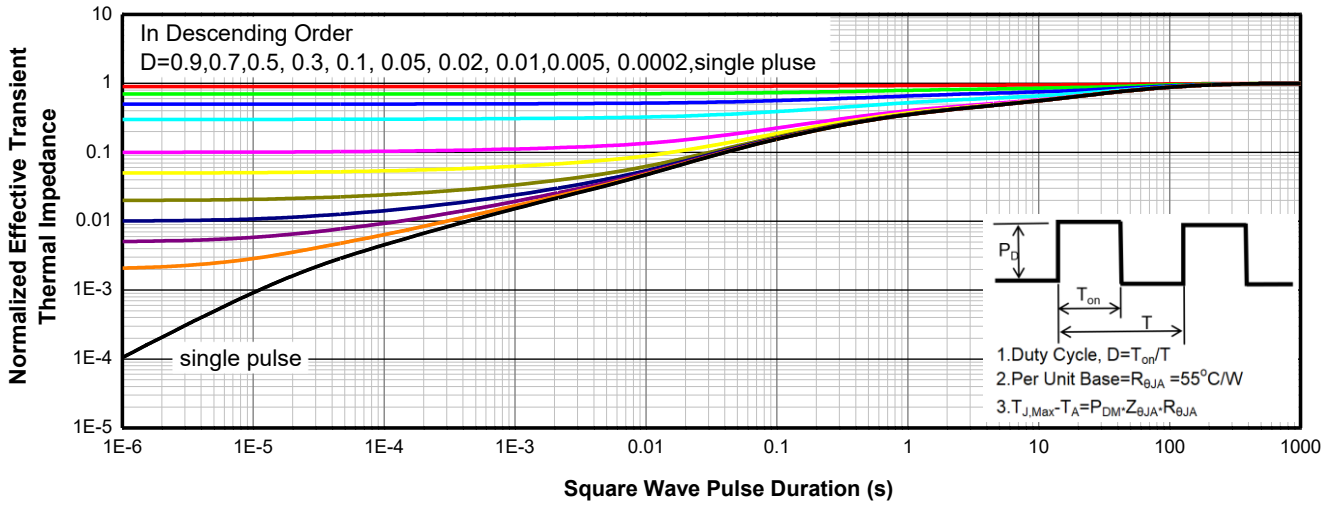
Gate Charge Characteristics



EOSS



Transient Thermal Response (Junction-to-Case)



Transient Thermal Response (Junction -to-Ambient)

PACKAGE OUTLINE DIMENSIONS

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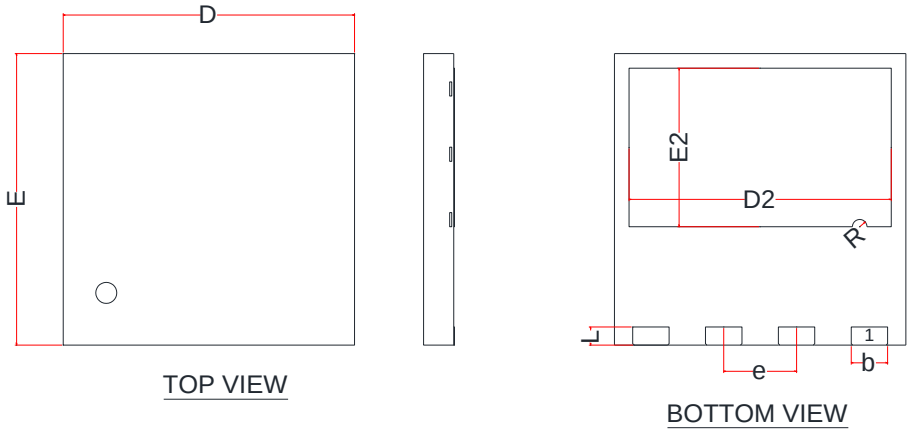

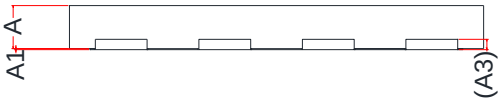

SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20Ref.	
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E2	4.25	4.35	4.45
e	1.90	2.00	2.10
K	2.65	2.75	2.85
L	0.40	0.50	0.60
R	0.20REF	-	-

RECOMMENDED LAND PATTERN (Unit: mm)

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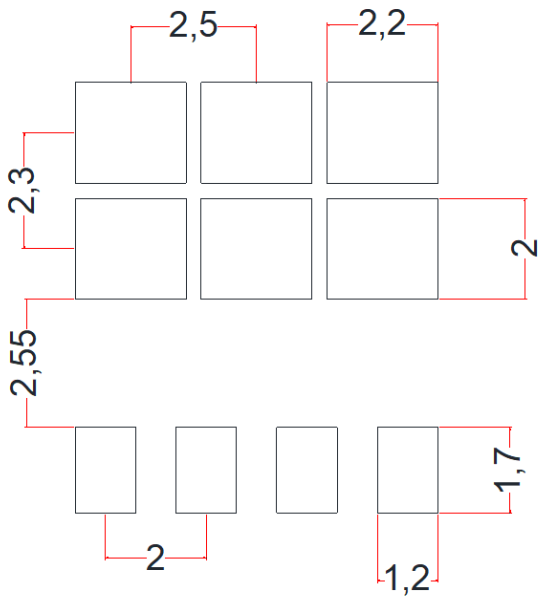
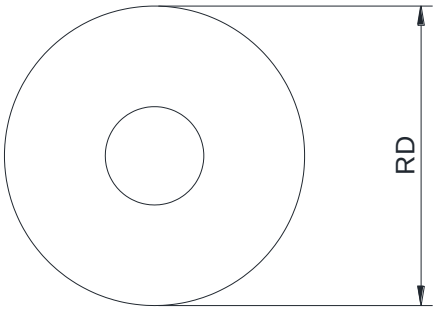


Notes:

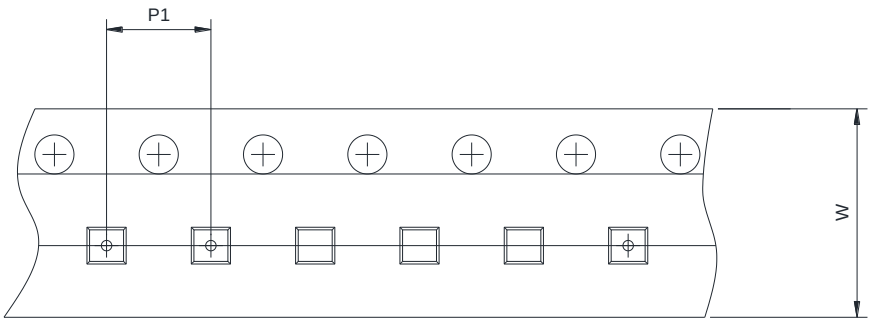
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

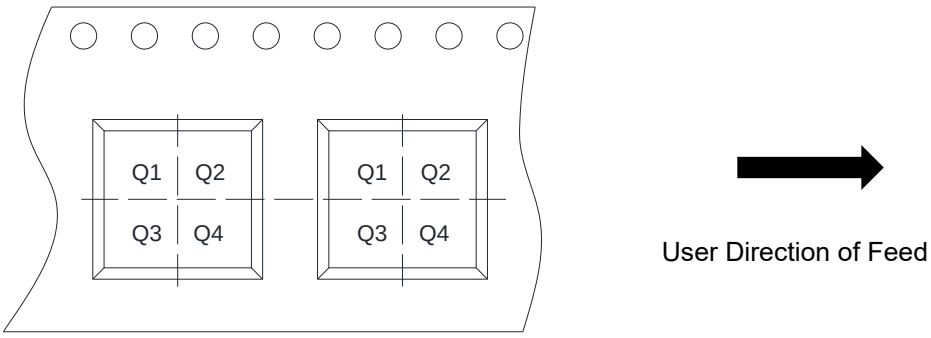
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☐ 12mm ☑ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☐ 8mm ☑ 12mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4