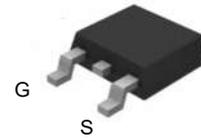


# WNM6010

## Single N-Channel, 60V, 76A, Power MOSFET

[Http://www.omnivision-group.com](http://www.omnivision-group.com)

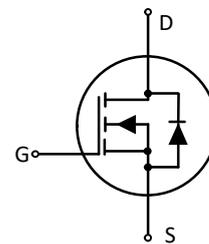
V <sub>DS</sub> (V)	Max. R <sub>DS(on)</sub> (mΩ)
60	5.4 @ V <sub>GS</sub> =10V
	8.8 @ V <sub>GS</sub> =6V



**TO-252E-2L**

### Description

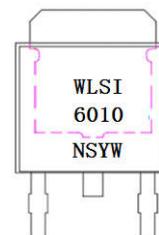
The WNM6010 is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent R<sub>DS(ON)</sub> with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNM6010 is in compliance with RoHS.



**Pin configuration (Top view)**

### Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Package TO-252E-2L



WLSI = Company Code  
 6010 = Device Code  
 NS = Special Code  
 Y = Year  
 W = Week(A~z)

### Marking

### Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

### Order information

Device	Package	Shipping
WNM6010-3/TR	TO-252E-2L	2500/Tape&Reel

### Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>d</sup>	$I_D$	$T_C=25^\circ\text{C}$	76
		$T_C=100^\circ\text{C}$	48
Pulsed Drain Current <sup>c</sup>	$I_{DM}$	310	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	32
		$T_A=70^\circ\text{C}$	26
Avalanche Energy $L=0.3\text{mH}$	$E_{AS}$	200	mJ
Power Dissipation <sup>b</sup>	$P_D$	$T_C=25^\circ\text{C}$	53
		$T_C=100^\circ\text{C}$	21
Power Dissipation <sup>a</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	9.6
		$T_A=70^\circ\text{C}$	6.2
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal resistance ratings

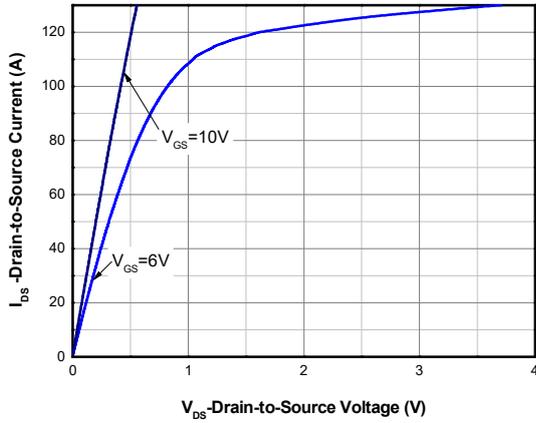
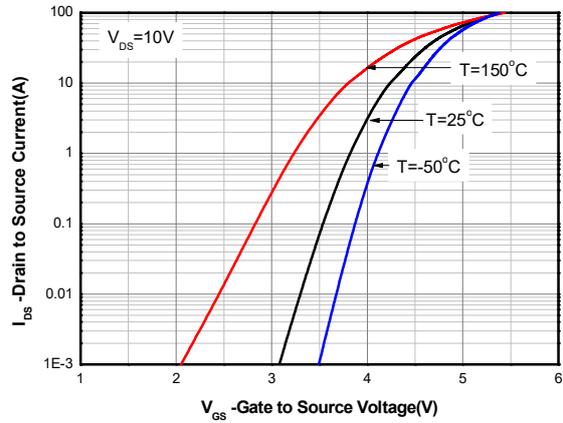
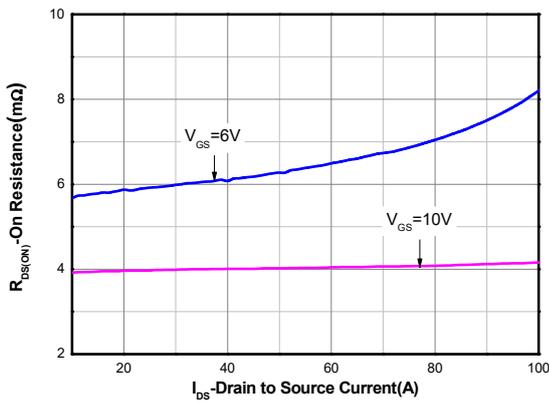
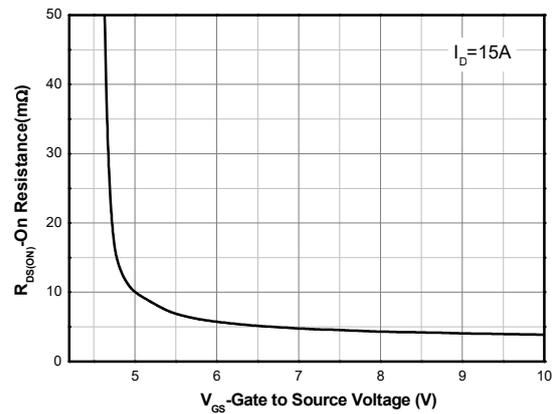
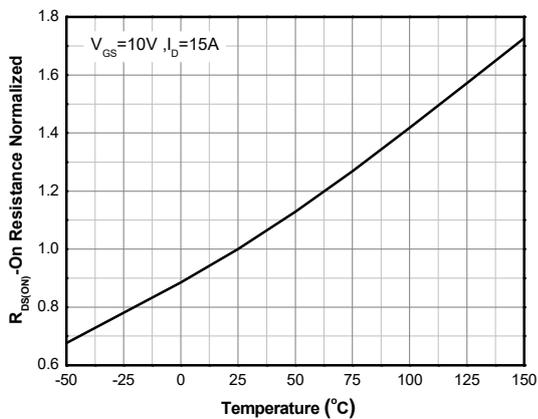
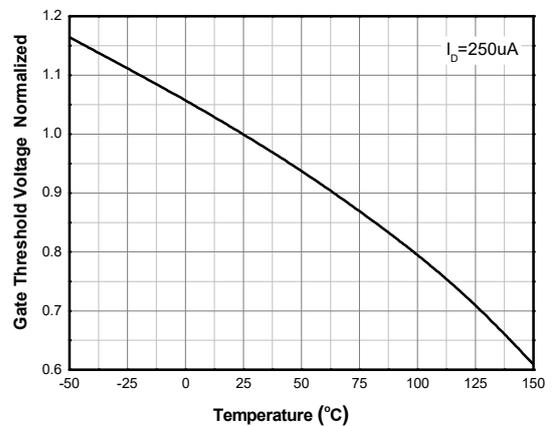
Single Operation					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient Thermal Resistance <sup>a</sup>	$R_{\theta JA}$	$t \leq 10\text{ s}$	11	13	$^\circ\text{C/W}$
		Steady State	35	42	
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	2.3	2.7		

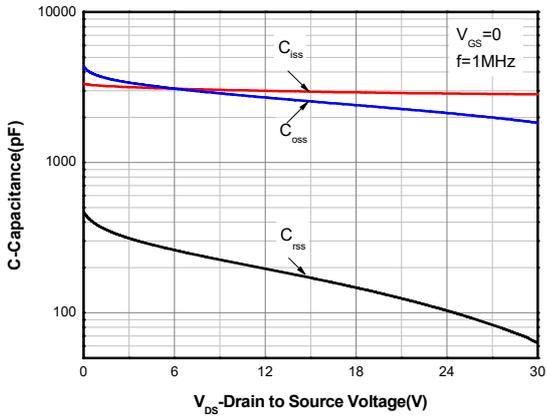
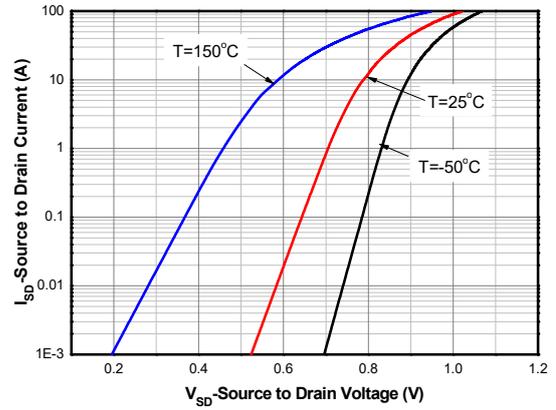
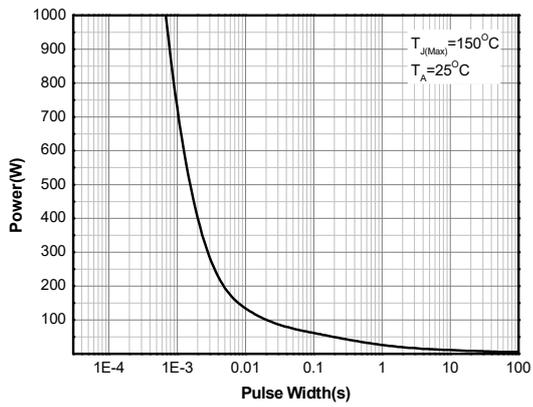
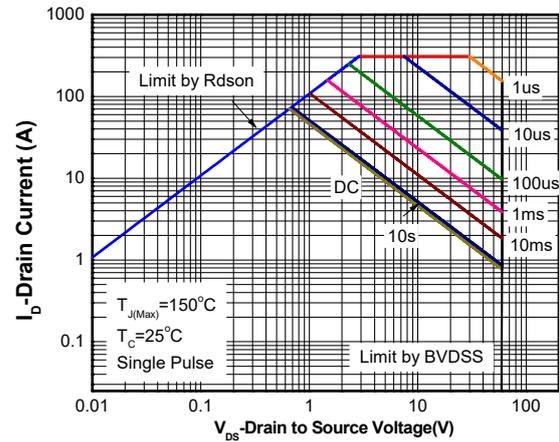
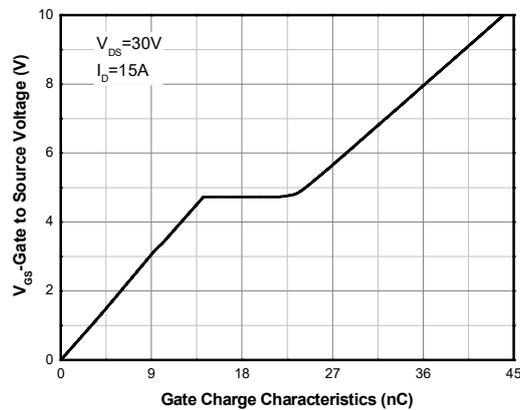
**Note:**

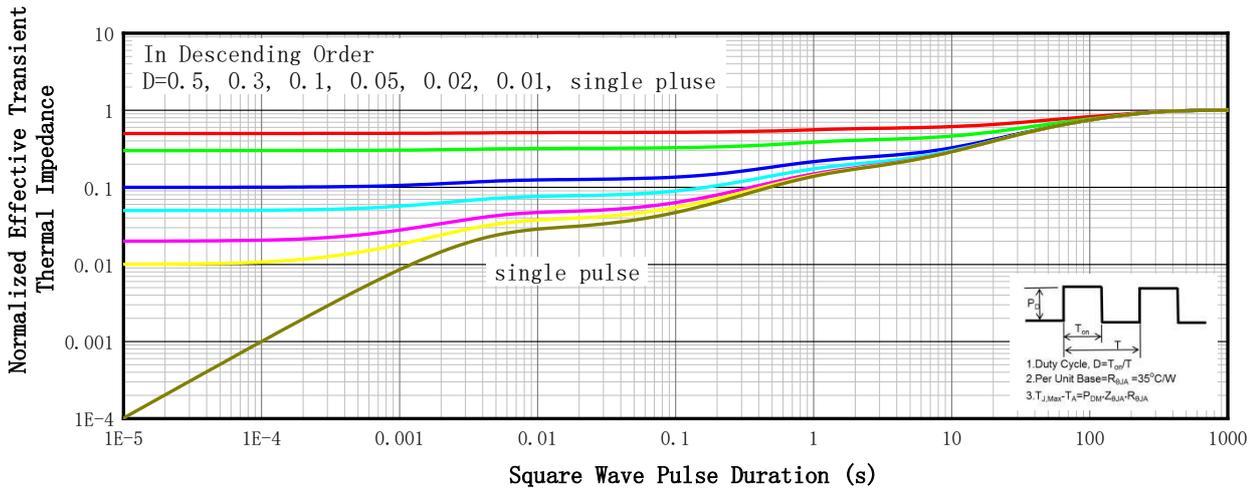
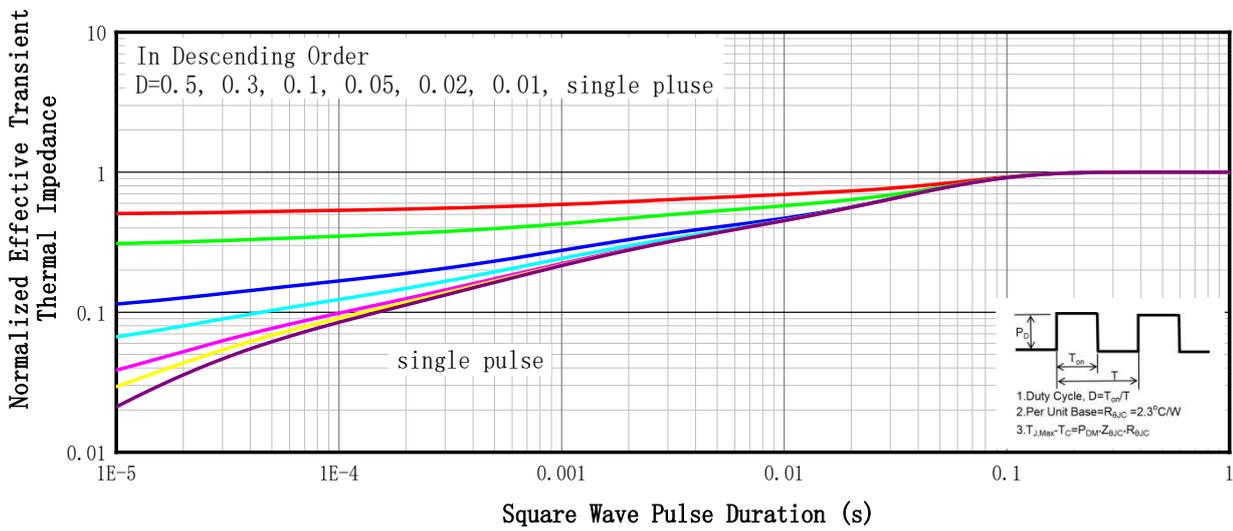
- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm<sup>2</sup> area).
- b The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial  $T_J = 25^\circ\text{C}$ , the maximum allowed junction temperature of  $150^\circ\text{C}$ .
- d The power dissipation  $P_{DSM}$  is based on Junction-to-Ambient thermal resistance  $R_{\theta JA}$   $t \leq 10\text{s}$  value and the  $T_{J(MAX)}=150^\circ\text{C}$ .
- e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

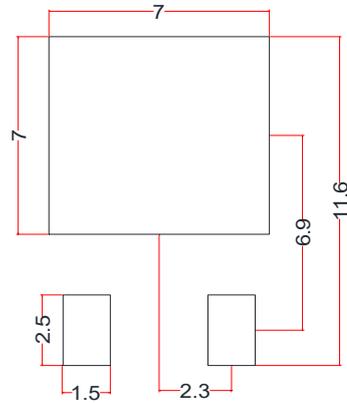
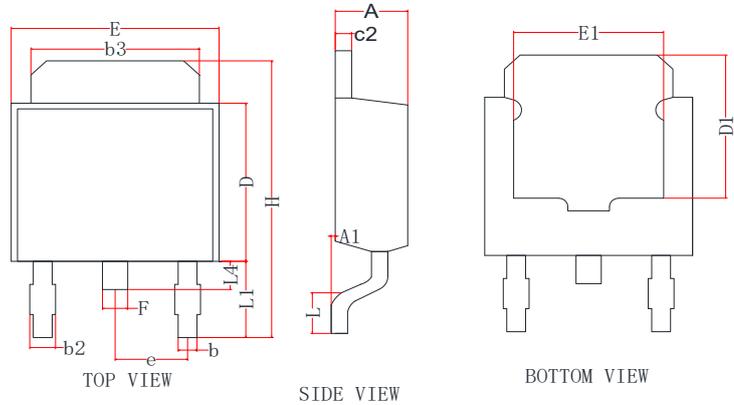
**Electronics Characteristics (Ta=25°C, unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250uA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V			1	uA
Gate-to-source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20V			±100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250uA	2.0	3.0	4.0	V
Drain-to-source On-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 15A		4.1	5.4	mΩ
		V <sub>GS</sub> = 6V, I <sub>D</sub> = 10A		6.0	8.8	
<b>CHARGES, CAPACITANCES AND GATE RESISTANCE</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0 V, f = 1.0MHz, V <sub>DS</sub> = 30V		2844		pF
Output Capacitance	C <sub>OSS</sub>			1835		
Reverse Transfer Capacitance	C <sub>RSS</sub>			63		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 15 A		44		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			8.8		
Gate-to-Source Charge	Q <sub>GS</sub>			14.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			7.9		
Gate Resistance	R <sub>g</sub>	f=1MHz		1.2		Ω
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	td(ON)	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =15A, R <sub>G</sub> =25Ω		41		ns
Rise Time	tr			52		
Turn-Off Delay Time	td(OFF)			100		
Fall Time	tf			68		
<b>BODY DIODE CHARACTERISTICS</b>						
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15A		0.8	1.2	V

**Typical Characteristics (Ta=25°C, unless otherwise noted)**

**Output Characteristics <sup>e</sup>**

**Transfer Characteristics <sup>e</sup>**

**On-Resistance vs. Drain Current <sup>e</sup>**

**On-Resistance vs. Gate-to-Source Voltage <sup>e</sup>**

**On-Resistance vs. Junction Temperature <sup>e</sup>**

**Threshold Voltage vs. Temperature**

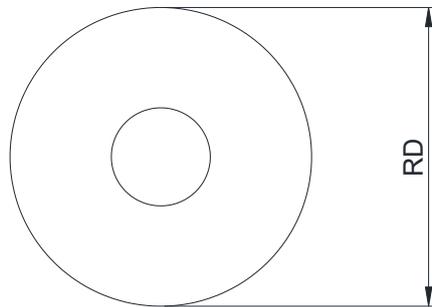
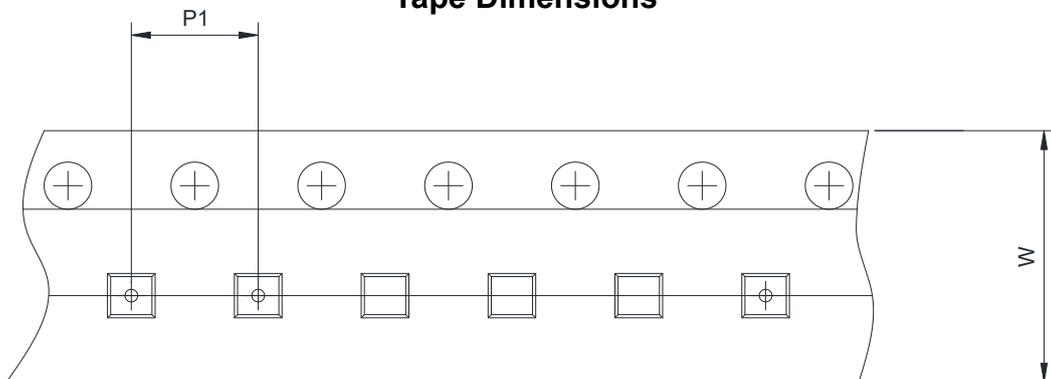
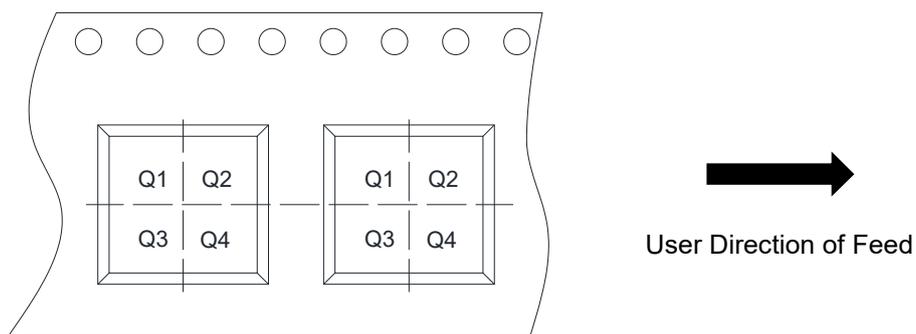

**Capacitance**

**Body Diode Forward Voltage<sup>e</sup>**

**Single Pulse power**

**Safe Operating Power**

**Gate Charge Characteristics**


**Transient Thermal Response (Junction-to-Case)**

**Transient Thermal Response (Junction-to-Ambient)**

**PACKAGE OUTLINE DIMENSIONS**
**TO-252E-2L**


RECOMMENDED LAND PATTERN (Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0	0.08	0.15
b	0.50	0.60	0.70
b 2	0.60	0.75	0.90
b 3	5.20	5.35	5.50
c 2	0.45	0.50	0.55
D	5.40	5.60	5.80
D1	4.57	--	--
E	6.40	6.60	6.80
E1	3.81	--	--
e	2.30 Ref.		
F	0.70	0.80	0.90
H	9.40	9.80	10.20
L	1.40	1.59	1.77
L1	2.40	2.70	3.00
L4	0.80	1.00	1.20

**TAPE AND REEL INFORMATION**
**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments For PIN1 Orientation In Tape**


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input checked="" type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input checked="" type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input type="checkbox"/> Q1	<input checked="" type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4