SGM2072
1.2A, Ultra-High PSRR, Fast Load Transient, Bias Rail CMOS Voltage Regulator

GENERAL DESCRIPTION

The SGM2072 is an ultra-high PSRR, fast transient response, low noise and low dropout voltage linear regulator which is designed using CMOS technology. It provides 1.2A output current capability. The operating input voltage range is from 0.5V to 5.5V and bias supply voltage range is from 2.5V to 5.5V. The adjustable output voltage range is from 0.5V to 3.3V.

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2072 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2072 is available in a Green WLCSP-0.8×1.2-6B-A package. It operates over an operating temperature range of -40℃ to +125℃.

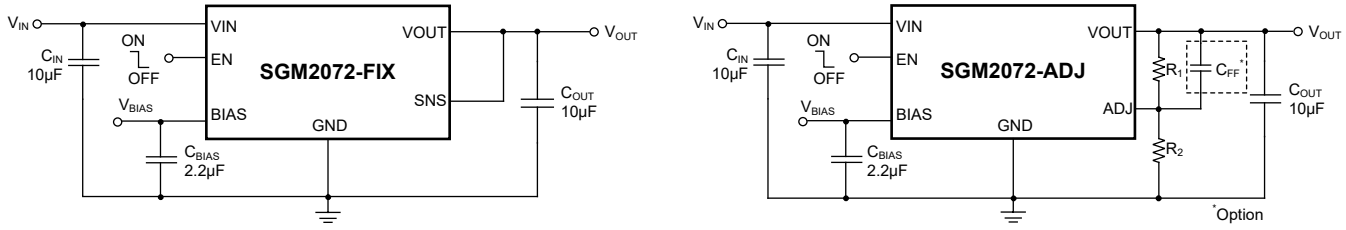
FEATURES

- **Input Supply Voltage Range: 0.5V to 5.5V**
- **Bias Supply Voltage Range: 2.5V to 5.5V**
- **Fixed Output of 1.05V**
- **Adjustable Output from 0.5V to 3.3V**
- **Output Voltage Accuracy: ±1.5% at +25℃**
- **Low Bias Input Current: 80μA (TYP)**
- **Low Dropout Voltage: 58mV (TYP) at 1.2A**
- **Low Noise: 34μV_{RMS} (TYP)**
- **High PSRR: 75dB (TYP) at 1kHz**
- **Very Low Bias Input Current in Shutdown: < 1μA**
- **Current Limiting and Thermal Protection**
- **With Output Automatic Discharge**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green WLCSP-0.8×1.2-6B-A Package**

APPLICATIONS

Portable Equipment
Smartphone
Industrial and medical Equipment

TYPICAL APPLICATION



Fixed Voltage Typical Application Circuit

Adjustable Voltage Typical Application Circuit

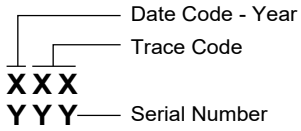
Figure 1. Typical Application Circuits

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2072-1.05	WLCSP-0.8×1.2-6B-A	-40℃ to +125℃	SGM2072-1.05XG/TR	XXX 021	Tape and Reel, 3000
SGM2072-ADJ	WLCSP-0.8×1.2-6B-A	-40℃ to +125℃	SGM2072-ADJXG/TR	XXX GJQ	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, BIAS, EN to GND ..... -0.3V to 6V
OUT, SNS, ADJ to GND ..... -0.3V to MIN(V_{IN} + 0.3V, 6V)
Package Thermal Resistance
WLCSP-0.8×1.2-6B-A, θ_{JA} ..... 177℃/W
WLCSP-0.8×1.2-6B-A, θ_{JB} ..... 32℃/W
WLCSP-0.8×1.2-6B-A, θ_{JC} ..... 48℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{IN} ..... 0.5V to 5.5V
Bias Supply Voltage Range, V_{BIAS} ..... 2.5V to 5.5V
Bias Effective Capacitance, C_{BIAS} ..... 0.1μF (MIN)
Input Effective Capacitance, C_{IN} ..... 4.7μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 4.7μF to 22μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

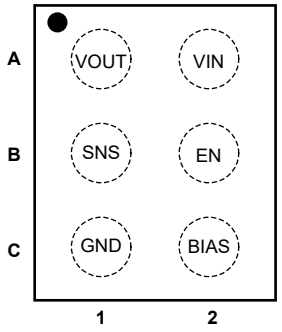
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

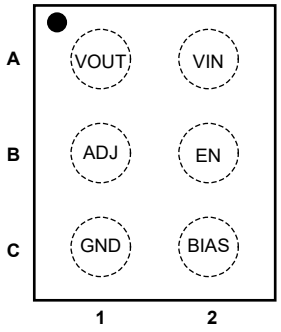
PIN CONFIGURATION

SGM2072-Fixed Output
(TOP VIEW)



WLCSP-0.8×1.2-6B-A

SGM2072-ADJ
(TOP VIEW)



WLCSP-0.8×1.2-6B-A

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	VOUT	Regulator Output Pin. It is recommended to use an output capacitor with effective capacitance in the range of 4.7μF to 22μF.
A2	VIN	Input Voltage Supply Pin.
B1	SNS	Output Voltage Sense Input Pin (fixed voltage version only). Connect this pin to the load side of the output trace only in the fixed voltage version.
	ADJ	Feedback Input Pin (adjustable voltage version only). Connect this pin to the external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
B2	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
C1	GND	Ground.
C2	BIAS	Bias Supply Voltage Pin for Internal Control Circuits. This pin is monitored by internal under-voltage lockout circuit.

FUNCTIONAL BLOCK DIAGRAMS

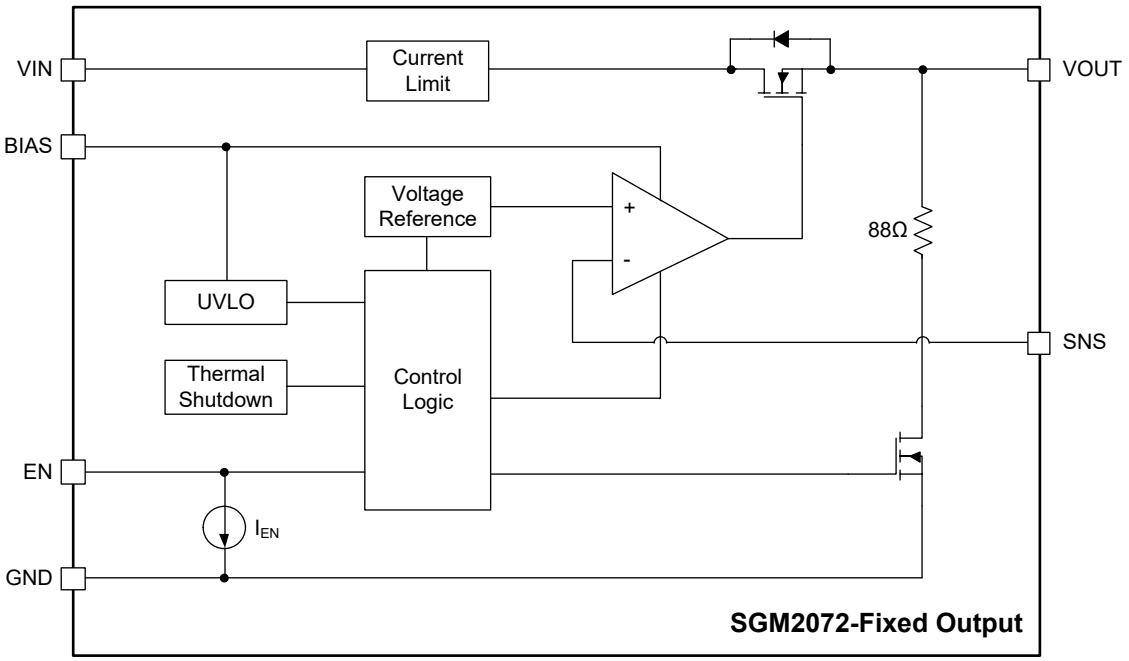


Figure 2. Fixed Output Voltage Internal Block Diagram

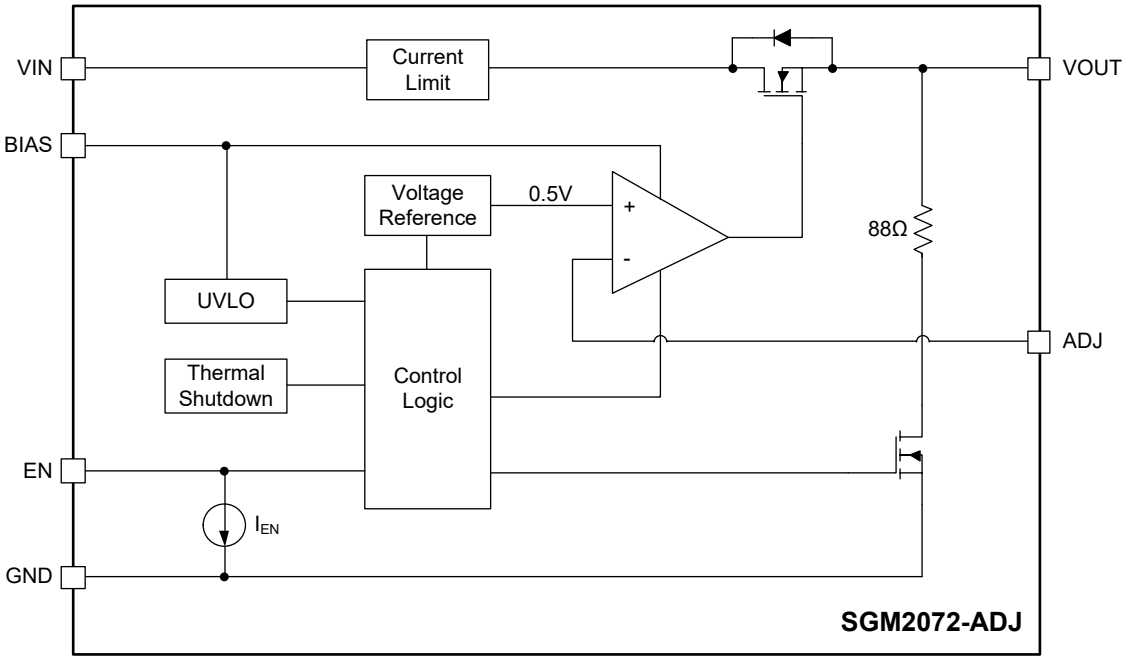


Figure 3. Adjustable Output Voltage Internal Block Diagram

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 2.5V or ($V_{OUT(NOM)}$ + 1.6V) (whichever is greater), $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 10μF and C_{BIAS} = 2.2μF, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{IN}			$V_{OUT(NOM)}$ + V_{DROP_VIN}		5.5	V
Bias Supply Voltage Range	V_{BIAS}			($V_{OUT(NOM)}$ + 1.6) ≥ 2.5		5.5	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 5.5V, V_{BIAS} = 2.5V or ($V_{OUT(NOM)}$ + 1.6V) to 5.5V, I_{OUT} = 1mA to 1.2A	T_J = +25℃	-1.5		1.5	%
			T_J = -40℃ to +125℃	-3		3	
Adjustable Reference Voltage	V_{ADJ}	SGM2072-ADJ	T_J = +25℃	0.4925	0.5	0.5075	V
			T_J = -40℃ to +125℃	0.485		0.515	
ADJ Pin Operating Current	I_{ADJ}	V_{ADJ} = 0.6V		-10		10	nA
Under-Voltage Lockout	V_{UVLO}	V_{BIAS} rising			1.6	2	V
		Hysteresis			0.2		V
V_{IN} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 5.5V			0.002	0.05	%/V
V_{BIAS} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{BIAS} \times V_{OUT}}$	V_{BIAS} = 2.5V or ($V_{OUT(NOM)}$ + 1.6V) to 5.5V			0.02	0.2	%/V
Load Regulation	ΔV_{OUT}	I_{OUT} = 1mA to 1.2A			1	6	mV
V_{IN} Dropout Voltage (1)	V_{DROP_VIN}	I_{OUT} = 1.2A			58	100	mV
V_{BIAS} Dropout Voltage (2) (3)	V_{DROP_BIAS}	I_{OUT} = 1.2A, V_{IN} = V_{BIAS}			1.2	1.5	V
Output Current Limit	I_{LIMIT}	V_{OUT} = 90% × $V_{OUT(NOM)}$, T_J = -40℃ to +85℃		1.2	2.7		A
Short Current Limit	I_{SHORT}	V_{OUT} = 0V			0.9		A
BIAS Pin Quiescent Current	I_{BIAS}	V_{BIAS} = 5.5V			80	130	μA
VIN Pin Quiescent Current	I_{IN}	V_{IN} = 5.5V, I_{OUT} = 0mA			35	100	μA
BIAS Pin Shutdown Current	$I_{BIAS(DIS)}$	V_{EN} = 0V			0.001	1	μA
VIN Pin Shutdown Current	$I_{VIN(DIS)}$	V_{EN} = 0V	T_J = +25℃			0.5	μA
			T_J = -40℃ to +125℃			2	
EN Input Voltage	V_{IH}	Logic high		1			V
	V_{IL}	Logic low				0.4	V
EN Pull-Down Current	I_{EN}	V_{EN} = 5.5V, V_{BIAS} = 5.5V			0.27	1	μA
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 98% × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 1.1V			110		μs
V_{IN} Power Supply Rejection Ratio	PSRR	V_{IN} to V_{OUT}, $V_{OUT(NOM)}$ = 1.1V, V_{IN} ≥ 1.6V, I_{OUT} = 150mA, f = 1kHz			75		dB
V_{BIAS} Power Supply Rejection Ratio		V_{BIAS} to V_{OUT}, $V_{OUT(NOM)}$ = 1.1V, V_{IN} ≥ 1.6V, I_{OUT} = 150mA, f = 1kHz			80		dB
Output Voltage Noise	e_n	$V_{OUT(NOM)}$ = 1.1V, V_{IN} = 1.6V, f = 10Hz to 100kHz			34		μV_{RMS}
Output Discharge Resistance	R_{DIS}	V_{EN} = 0V, V_{OUT} = 0.5V		50	88	130	Ω
Thermal Shutdown Temperature	T_{SHDN}				165		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				30		℃

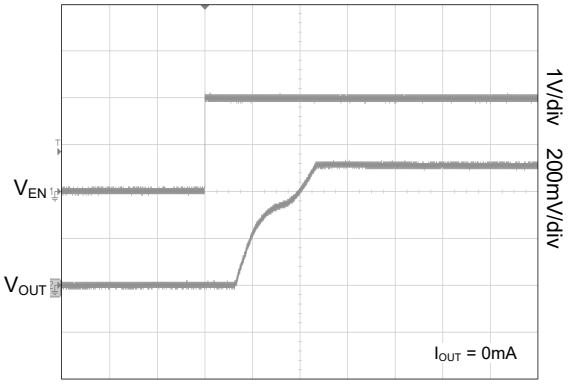
NOTES:

1. V_{IN} dropout voltage is defined as the difference between V_{IN} and V_{OUT} when V_{OUT} falls to 95% × $V_{OUT(NOM)}$.
2. V_{BIAS} dropout voltage refers to V_{BIAS} - V_{OUT} when the VIN and BIAS pins are connected together and V_{OUT} falls to 95% × $V_{OUT(NOM)}$.
3. For output voltages lower than 1.6V, V_{BIAS} dropout voltage is not applicable because the minimum bias supply voltage is 2.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

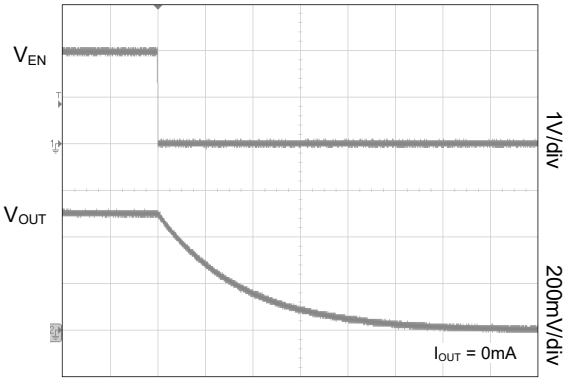
T_J = +25℃, V_{IN} = 0.8V, V_{EN} = V_{BIAS} = 2.5V, $V_{OUT(NOM)}$ = 0.5V, C_{IN} = C_{OUT} = 10μF, C_{BIAS} = 2.2μF, unless otherwise noted.

Turn-On Speed with EN Pin



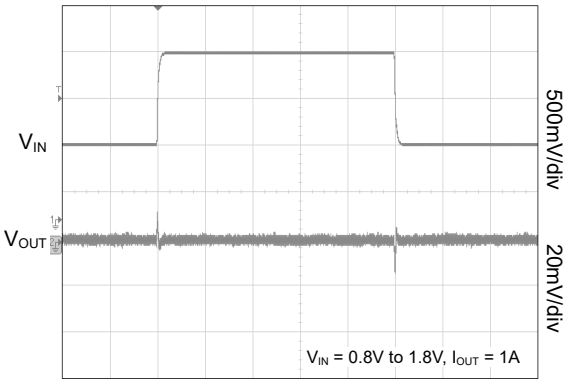
Time (50μs/div)

Turn-Off Speed with EN Pin



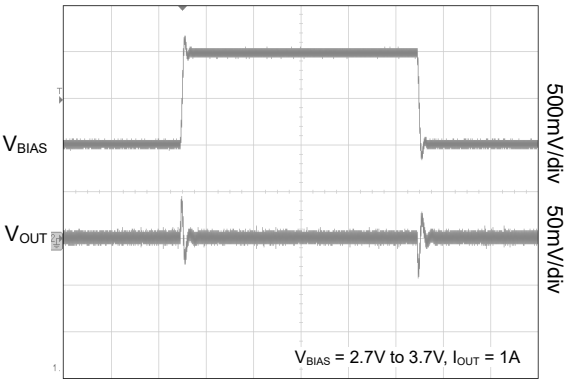
Time (500μs/div)

V_{IN} Line Transient Response



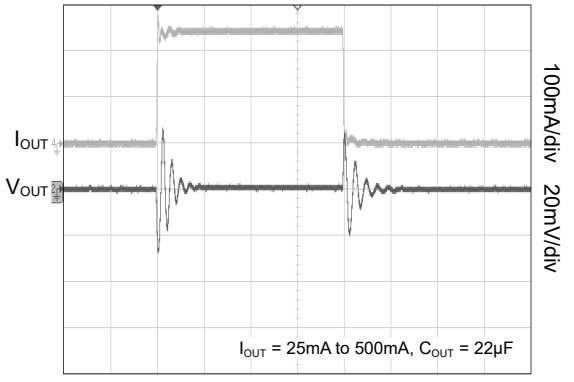
Time (100μs/div)

V_{BIAS} Line Transient Response



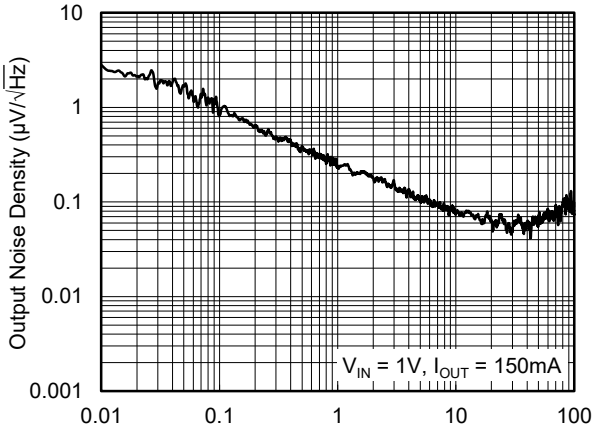
Time (100μs/div)

Load Transient Response



Time (50μs/div)

Output Noise Density vs. Frequency

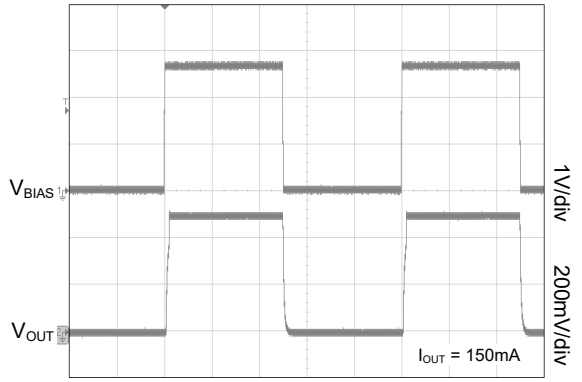


Frequency (kHz)

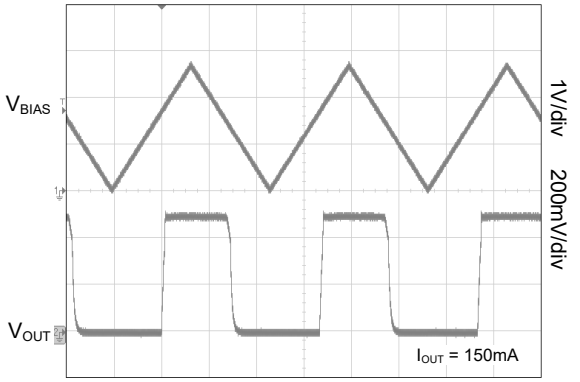
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 0.8V, V_{EN} = V_{BIAS} = 2.5V, $V_{OUT(NOM)}$ = 0.5V, C_{IN} = C_{OUT} = 10μF, C_{BIAS} = 2.2μF, unless otherwise noted.

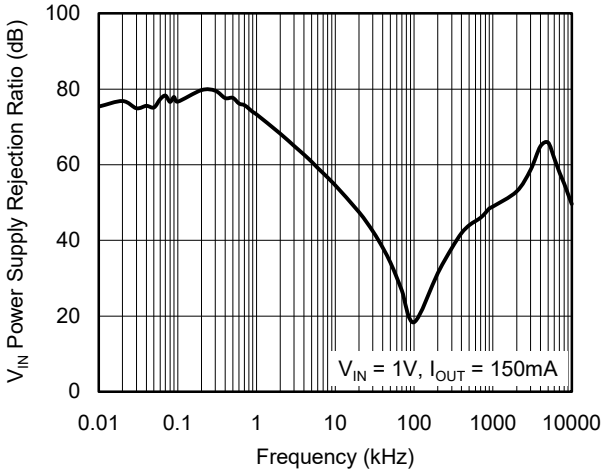
V_{BIAS} Power-Up/Power-Down Output Waveform



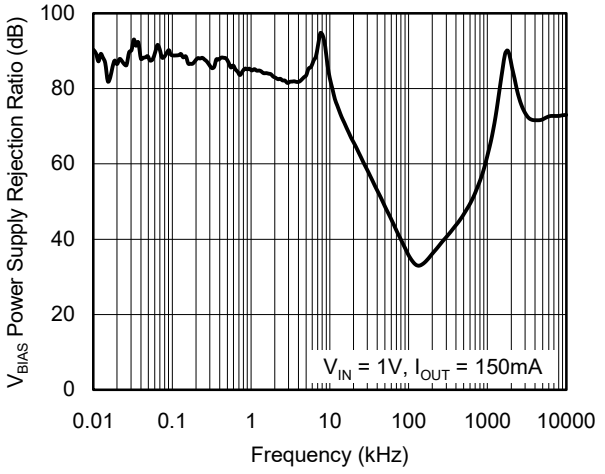
V_{BIAS} Power Ramp-Up/Ramp-Down Output Waveform



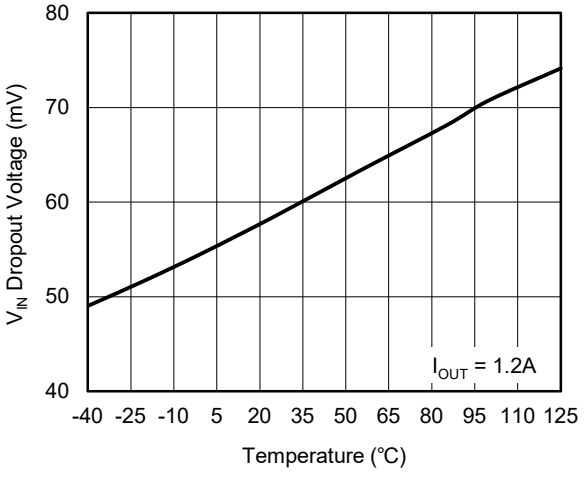
V_{IN} Power Supply Rejection Ratio vs. Frequency



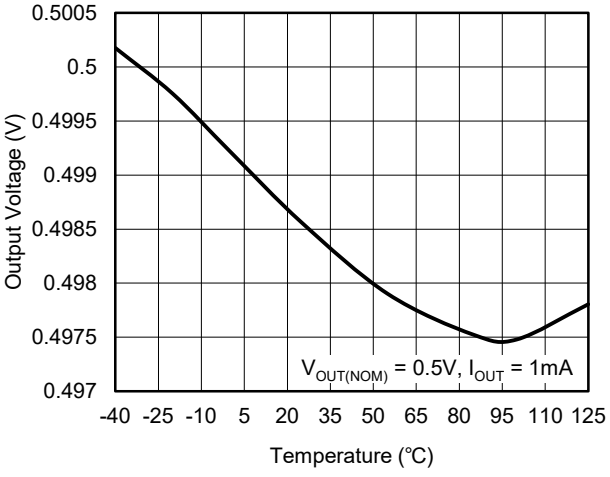
V_{BIAS} Power Supply Rejection Ratio vs. Frequency



V_{IN} Dropout Voltage vs. Temperature



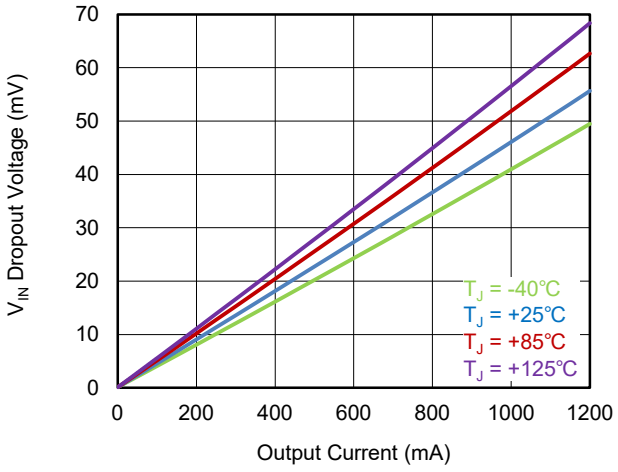
Output Voltage vs. Temperature



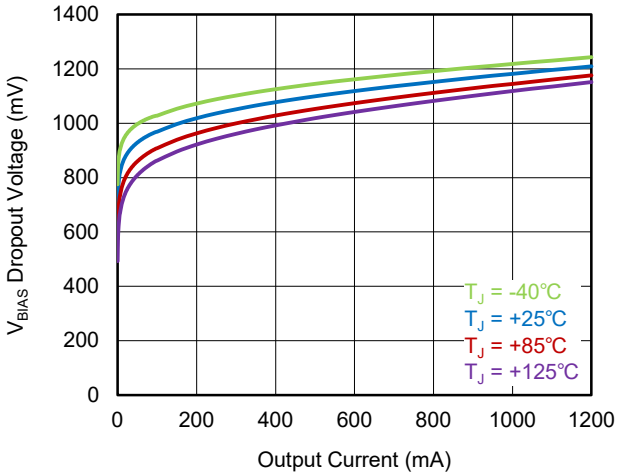
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 0.8V, V_{EN} = V_{BIAS} = 2.5V, $V_{OUT(NOM)}$ = 0.5V, C_{IN} = C_{OUT} = 10μF, C_{BIAS} = 2.2μF, unless otherwise noted.

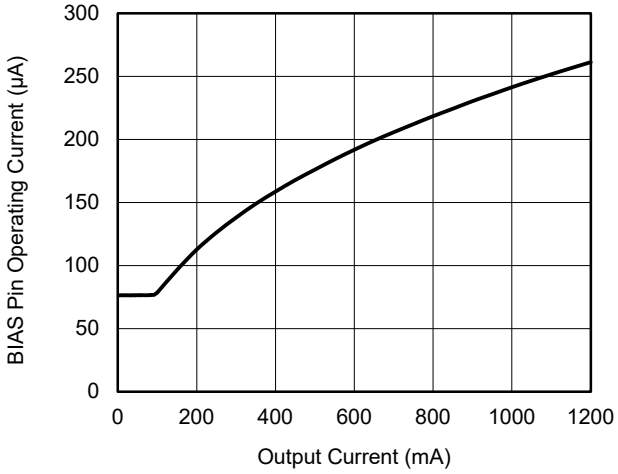
V_{IN} Dropout Voltage vs. Output Current



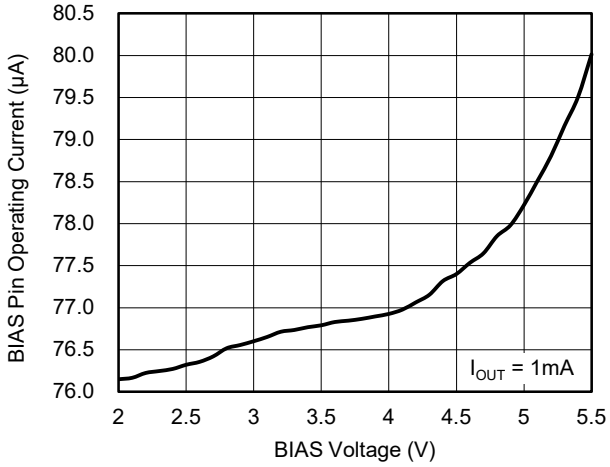
V_{BIAS} Dropout Voltage vs. Output Current



BIAS Pin Operating Current vs. Output Current



BIAS Pin Operating Current vs. BIAS Voltage



APPLICATION INFORMATION

The SGM2072 is a low noise, fast transient response high performance LDO. It consumes only 80μA (TYP) quiescent current and provides 1.2A output current. The SGM2072 provides the protection functions for output overload, output short-circuit condition and overheating.

The SGM2072 is suitable for application which has noise sensitive circuit such as battery-powered equipment and smartphones.

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the VIN pin to ensure the device stability. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

The output capacitor should be placed as close as possible to the VOUT pin. A 10μF or greater X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of C_{OUT} that SGM2072 can remain stable is 4.7μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Dropout Voltage

The SGM2072 specifies two dropout voltages because there are two power supplies V_{IN} and V_{BIAS} and one V_{OUT} regulator output. V_{IN} dropout voltage is defined as the difference between V_{IN} and V_{OUT} when V_{OUT} falls 5% below $V_{OUT(NOM)}$. When the output voltage is lower than 1.6V, V_{BIAS} dropout voltage is not applicable because the minimum bias supply voltage is 2.5V.

When V_{OUT} begins to decrease and V_{BIAS} is high enough, the V_{IN} dropout voltage equals to V_{IN} - V_{OUT}. V_{BIAS} dropout voltage refers to V_{BIAS} - V_{OUT} when the VIN and BIAS pins are connected together and V_{OUT} begins to decrease.

Adjustable Regulator

The output voltage of the SGM2072-ADJ can be adjusted from 0.5V to 3.3V. The ADJ pin will be connected to two external resistors as shown in Figure 4. The output voltage is determined by the following equation:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

V_{OUT} is output voltage and V_{ADJ} is the adjustable reference voltage, V_{ADJ} = 0.5V.

One parallel capacitor (C_{FF}) with R_1 can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the output noise. Use $R_2 \leq 10k\Omega$ with C_{FF} in the range of 1nF to 100nF (effective capacitance).

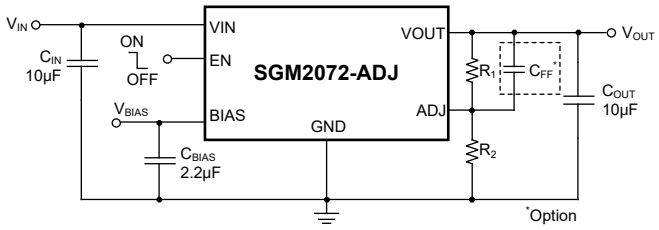


Figure 4. Adjustable Output Voltage Application

Enable Operation

The EN pin of the SGM2072 is used to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.4V, the device is in shutdown state. There is no current flowing from VIN to VOUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through an 88Ω (TYP) resistor.

When the EN pin voltage is higher than 1V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

The EN pin is pulled down by internal 0.27μA (TYP) current source when the EN pin is floated. This current source will ensure the SGM2072 in shutdown state and reduce the power dissipation in system.

APPLICATION INFORMATION (continued)

Reverse Current Protection

The NMOS power transistor has an inherent body diode, this body diode will be forward biased when V_{OUT} > V_{IN}. When V_{OUT} > V_{IN}, the reverse current flowing from the VOUT pin to the VIN pin will damage the SGM2072. If V_{OUT} > (V_{IN} + 0.3V) is expected in the application, one external Schottky diode will be added between the VOUT pin and VIN pin to protect the SGM2072.

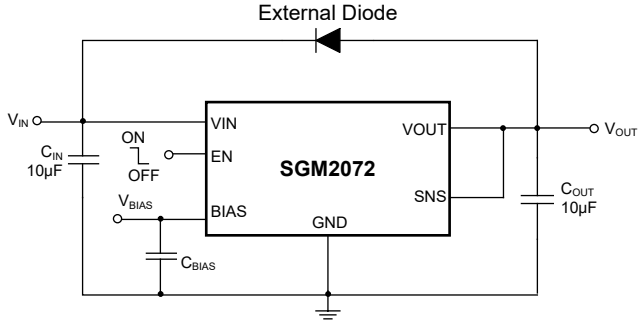


Figure 5. Reverse Protection Reference Design

Negatively Biased Output

When the output voltage is negative, the chip may not start up due to parasitic effects. Ensure that the output is greater than -0.3V under all conditions. If negatively biased output is excessive and expected in the application, a Schottky diode can be added between the VOUT pin and GND pin.

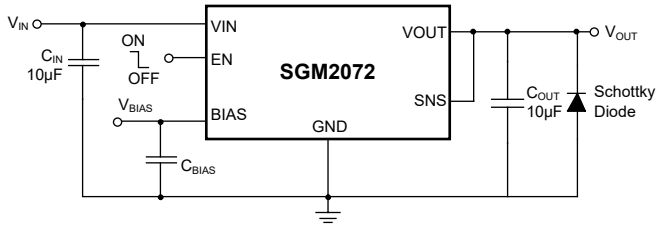


Figure 6. Negatively Biased Output Application

Output Current Limit and Short-Circuit Protection

When overload events happen, the output current is internally limited to 2.7A (TYP). When the VOUT pin is shorted to ground, the short-circuit protection will limit the output current to 0.9A (TYP).

Thermal Shutdown Protection

The SGM2072 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2072 will be in shutdown state and it will remain in this state until the die temperature decreases to +135℃.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2072 can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2072 is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (2)$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN/BIAS pin and OUT pin separately.

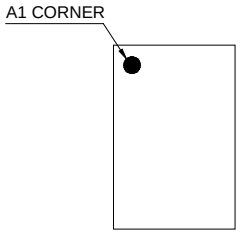
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

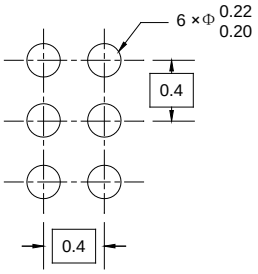
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

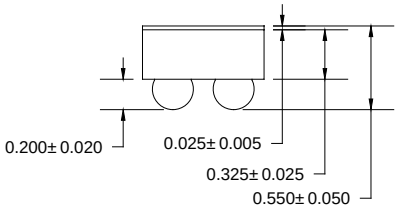
WLCSP-0.8×1.2-6B-A



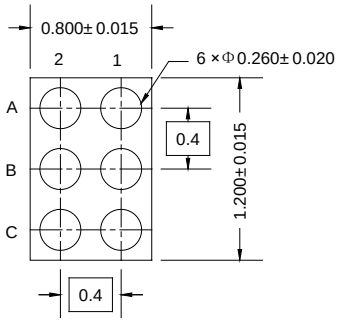
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

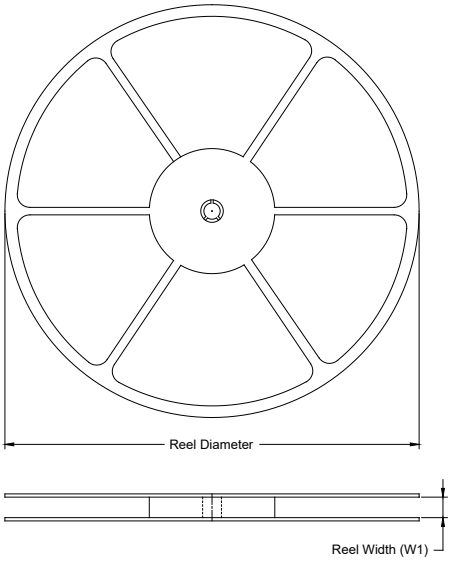


BOTTOM VIEW

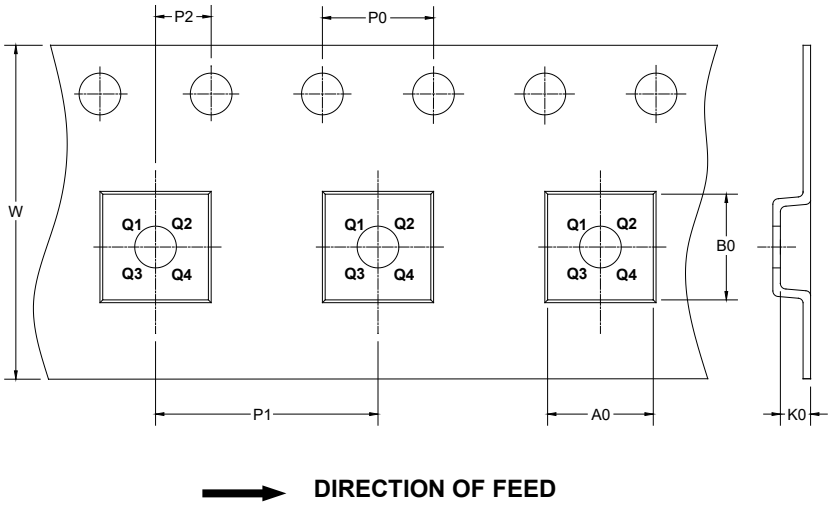
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



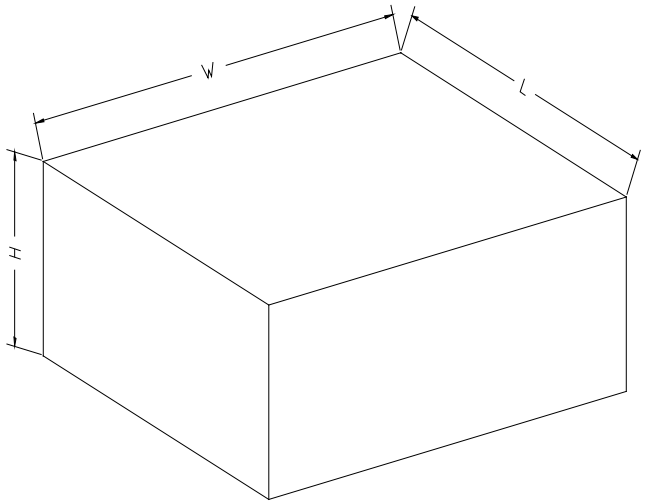
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.8×1.2-6B-A	7″	9.0	0.90	1.32	0.68	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002