SK2301AVP

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} -20V
- I_D -3.4A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜64 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜80 mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜95 mohm

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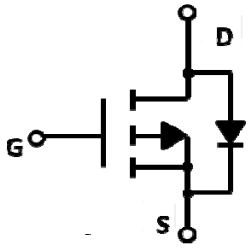

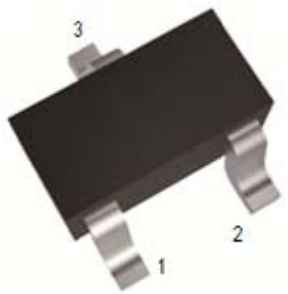

1 : Gate 2 : Source 3 : Drain

General Description

- Trench Power LV MOSFET technology
- High Power and Current handing capability
- Low Gate Charge
- Marking：A1SHB

Applications

- PWM applications
- Power management
- Load switch

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃	I_D	-3.4	A
	T_A=70℃		-2.7	
Pulsed Drain Current [A]		I_{DM}	-14	A
Total Power Dissipation @ T_A=25℃		P_D	1	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	125	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-3.4A		49	64	mΩ
		V_{GS}= -2.5V, I_D=-3A		59	80	
		V_{GS}= -1.8V, I_D=-2.5A		79	95	
Diode Forward Voltage	V_{SD}	I_S=-3.4A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-3.4	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHz		550		pF
Output Capacitance	C_{oss}			89		
Reverse Transfer Capacitance	C_{rss}			65		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-3.4A		4.3		nC
Gate Source Charge	Q_{gs}			0.8		
Gate Drain Charge	Q_{gd}			1.1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, I_D=-1A, R_{GEN}=2.5Ω		12		ns
Turn-on Rise Time	t_r			54		
Turn-off Delay Time	$t_{D(off)}$			15		
Turn-off Fall Time	t_f			9		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

Typical Performance Characteristics

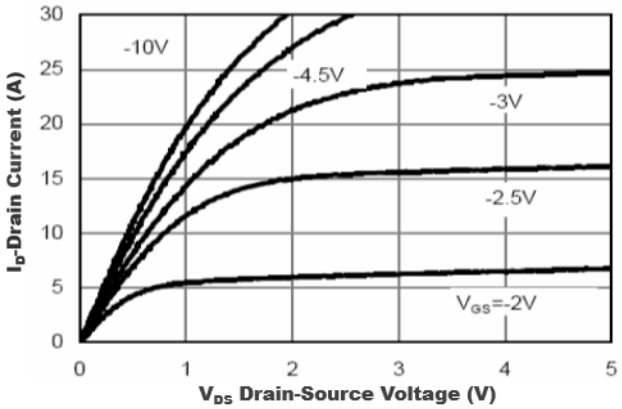

Figure1. Output Characteristics

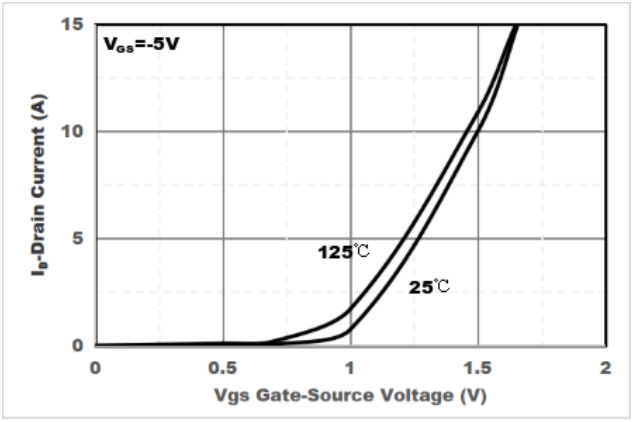

Figure2. Transfer Characteristics

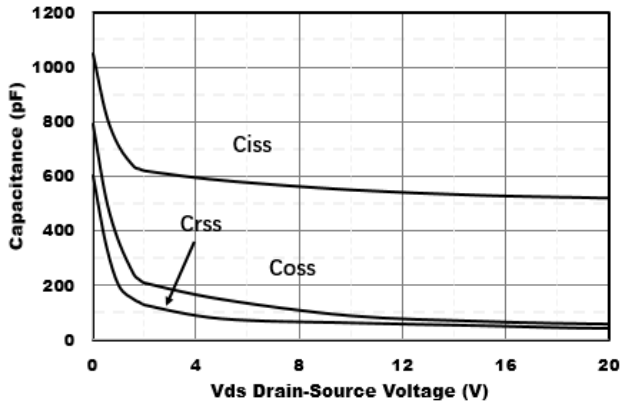

Figure3. Capacitance Characteristics

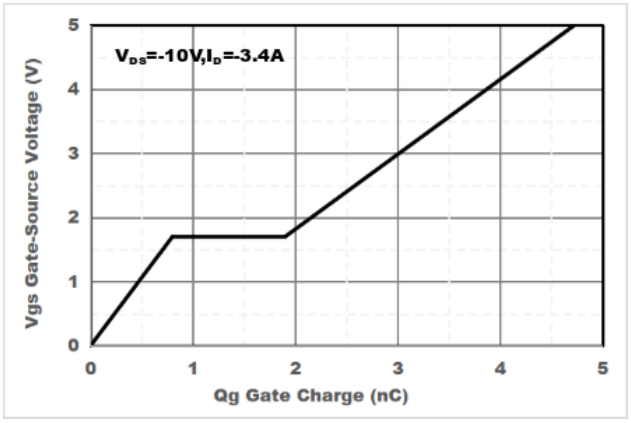

Figure4. Gate Charge

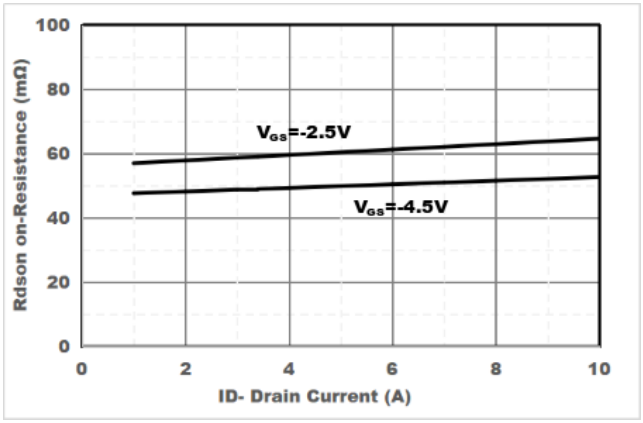

Figure5. Drain-Source on Resistance

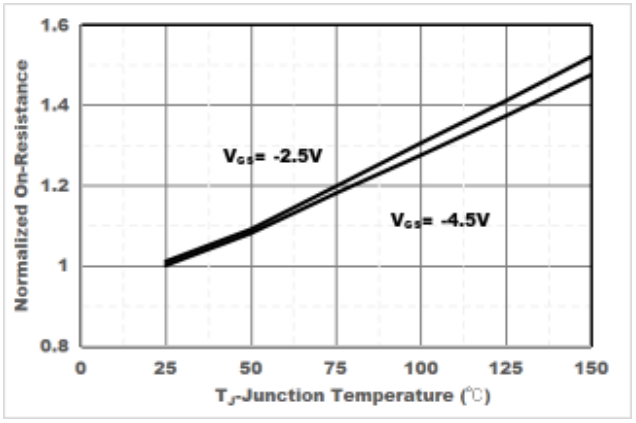

Figure6. Drain-Source on Resistance

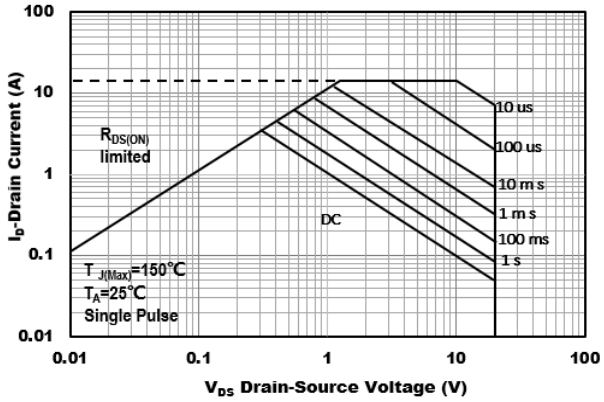

Figure7. Safe Operation Area

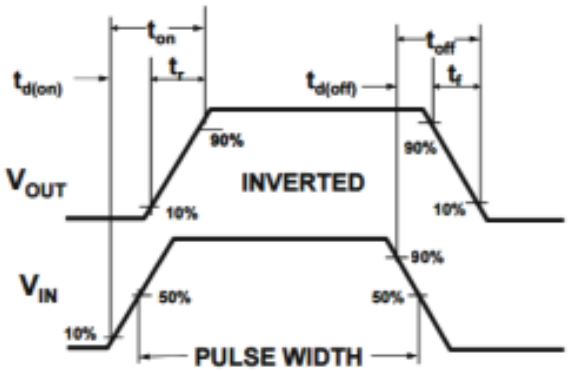

Figure8. Switching wave

Package Outline Dimensions (UNIT: mm)

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