XR829 Datasheet

Single-Chip IEEE 802.11 b/g/n WLAN, Bluetooth 2.1/4.0/4.2

Revision 1.4.1

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Revision History

Version	Data	Summary of Changes
1.0	2018-5-5	Initial Version
1.1	2018-11-30	Add Package Thermal Characteristics
1.2	2019-7-11	Update silkscreen
1.3	2019-8-2	Update declaration
1.4	2020-3-9	Update XR829 marking information
1.4.1	2020-6-12	Update the voltage range of ESD in section 5.1

Contents

Tables

Figures

1 System Overview

1.1 General Description

This scope of document is to provide a specification of XR829 Wireless LAN SoC, it will be used by the system/design/development teams to detail the design requirements.

XR829 is a fully integrated SoC to support 2.4G WLAN 802.11 b/g/n and Bluetooth 2.1+EDR/4.2. It is optimized for mobile applications such as PDAs and portable media players. High sensitivity and transmitting power ensure long distance and robust connection. Highest level of integration allows very compact and cost effective reference designs delivering fast time-to-market for new WLAN and Bluetooth enabled products. And small 5mmx5mm QFN package is suitable for very compact design.

1.2 Features

WLAN Features

- Compatible with IEEE 802.11 b/g/n standard
- 802.11n supports for 20/40MHz bandwidth
- Supports for Short Guard Interval
- Supports for 802.11n MCS0~MCS7
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Supports frame aggregation using A-MSDU, A-MPDU
- Supports MAC enhancements including
  - 802.11d - Regulatory domain operation
  - 802.11e - QoS including WMM
  - 802.11h - Transmit power control dynamic and frequency selection
  - 802.11i - Security including WPA2 and WAPI compliance
  - 802.11r - Roaming
  - 802.11w - Management frame protection
- Supports for Station, SoftAP and P2P mode
- Supports for Wi-Fi Direct

Bluetooth Features

- Bluetooth Dual Mode support with 2.1/4.0/4.2
- Class 1, Class 2 and Class 3 transmitter operation
- Host Controller Interface using a high-speed UART, maximum baud rate of 4 Mbps

- Adaptive Frequency Hopping
- SCO and eSCO support
- 1, 3 and 5 slots all packet types support
- Audio interfaces: PCM, I2S
- Transcoders for A-law, μ-law and CVSD voice over air
- Piconet and scatternet support
- Secure simple pairing
- Sniff/Sniff Subrating low power mode support

1.3Applications

Tablet PC

Smart internet TV box

Portable media player (PMP)

Portable gaming device (PGD)

Internet of Thing (IOT)

1.4Block Diagram

Top level block diagram of XR829 is shown in Figure 1-1.

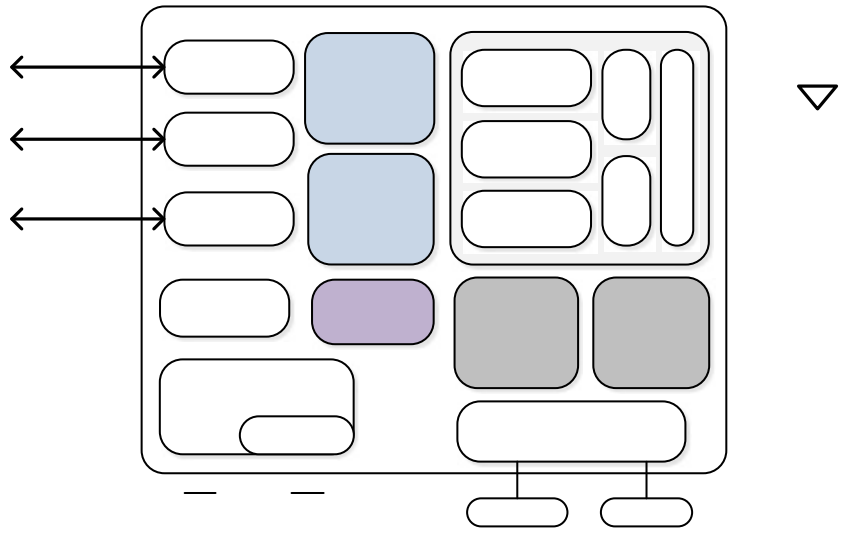


Figure 1-1 XR829 Block Diagram

The XR829 includes a single-band 2.4G RF transceiver (integration with PA, LNA and TR switch), PMU, WLAN modem, WLAN MAC, Bluetooth modem and Bluetooth protocol stack. The WLAN subsystem keeps data communications with the host using SDIO 2.0, while the Bluetooth subsystem uses HCI UART and PCM for audio data. The XR829 core provides an industry leading price competitive solution with a high level of system integration. In turn this reduces the

overall BOM cost while also shortening the mass production cycle.

2 Pin Description

2.1 Pin Assignment

Figure 2-1 Pin Assignment

2.2 Pin List

The following signal type codes are used in the table:

I: Input

O: Output

I/O: Input/Output

P: Power pin

Table 2-1 Pin List

Name	Pin	Type	Description
Analog			
XTAL1	4	I	Reference clock input or XTAL inputs
XTAL2	3	I	
ANT	40	I/O	2.4 GHz RF input/output
Power			
VDD14_TX	36	P	Supply for RF TX
VDD14_RX	1	P	Supply for RF RX
VDD14_DIG	22	P	Supply for digital LDO
VDD12_CLK	2	P	Supply for Clock
VDD12_DIG	21	P	Supply for digital LDO
VDD_IO	11	P	Supply for IO
VDD_SENSE	28	P	DCDC feedback
VDD_VLX	29	P	DCDC output
VDD_RTC	26	P	Supply for RTC
VDD25_EF	27	P	Supply for EFUSE
VDD33_PA	38	P	Supply for PA
VBAT	30,37	P	Supply for on-chip-PMU
Digital			
LDO_SEL	25	I	DCDC/LDO select 0: Internal switching regulator select 1: Internal LDO select
LPCLK	20	I	Low power clock input, 32kHz or 32.768 kHz
BT_WKUP_HOST	6	O	Bluetooth subsystem wakes up host
BT_HOST_WKUP	5	I	Host wakes up Bluetooth subsystem
PCM_CLK	31	I/O	Bluetooth PCM clock
PCM_IN	33	I	Bluetooth PCM data input
PCM_OUT	32	O	Bluetooth PCM data output
PCM_SYNC	34	I/O	Bluetooth PCM synchronization control
UART_TX	10	O	Bluetooth UART transmit
UART_RX	9	I	Bluetooth UART receive
UART_CTS	8	I	Bluetooth UART CTS
UART_RTS	7	O	Bluetooth UART RTS
BT_RSTN	23	I	Bluetooth reset, active low
WL_RSTN	24	I	WLAN reset, active low
CLKREQO	18	O	Clock request
WIRQ	35	O	WLAN interrupt request

SDIO_CMD	12	I/O	SDIO command
SDIO_D0	13	I/O	SDIO data
SDIO_D1	14	I/O	SDIO data
SDIO_D2	17	I/O	SDIO data
SDIO_D3	15	I/O	SDIO data
SDIO_CLK	16	I	SDIO clock
TEN	19	I	Test enable select, active high

3 Power Supply

3.1 Power Up and Power Down

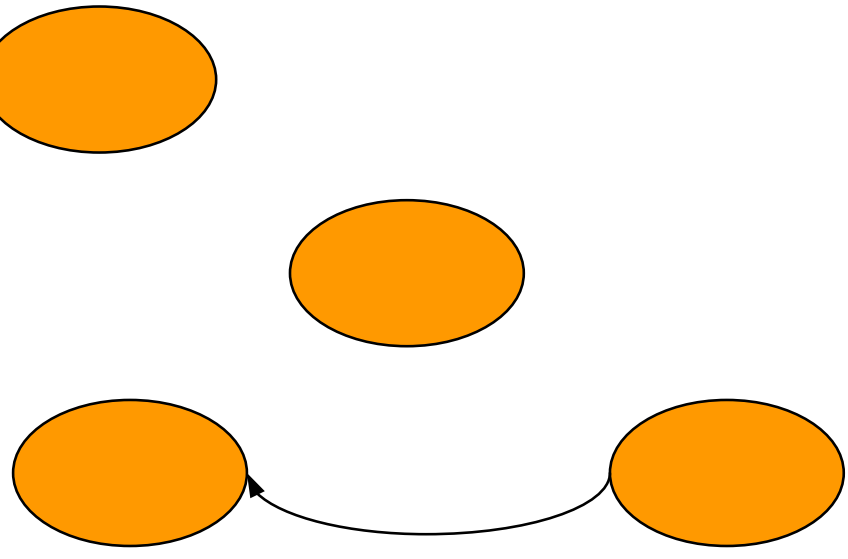


Figure 3-1 WLAN Subsystem Power Up and Power Down

There is no constraint on the WLAN subsystem power supplies (VBAT and VDD_IO) activation sequence. The WLAN subsystem can start up without the reference clock being present. The platform is then expected to provide a stable clock within T_{stable}ms (see reference value in chapter 4) unless the built-in XTAL oscillator is used. A typical startup for the WLAN subsystem is as follows:

(1)VBAT, VDD_IO is applied.

(2)Release WL_RSTN pin from low to high.

(3)The host should wait 30ms after the WL_RSTN release for the on-chip PMU to stabilize.

(4)WLAN subsystem is now in the Sleep state.

(5)The host wake up the WLAN subsystem by writing WUP bit through the SDIO interface.

(6)Within T_{stable}ms, the reference clock should be stable and the system can start using it.

(7)The host can download the firmware and release the CPU reset by further SDIO write.

(8)WLAN subsystem will begin to initialize.

(9)Once initialized, which includes a series of messages passing between the host and the WLAN subsystem, the WLAN subsystem may not have anything further to do and will enter the sleep state if Host set WLAN_RDY to 0.

To power down the WLAN subsystem, WL_RSTN has to be set to 0. There are no constraints on other input pins. VDD_IO is allowed to go down 20ms after all input signals have been set to 0 (avoid the influent current).

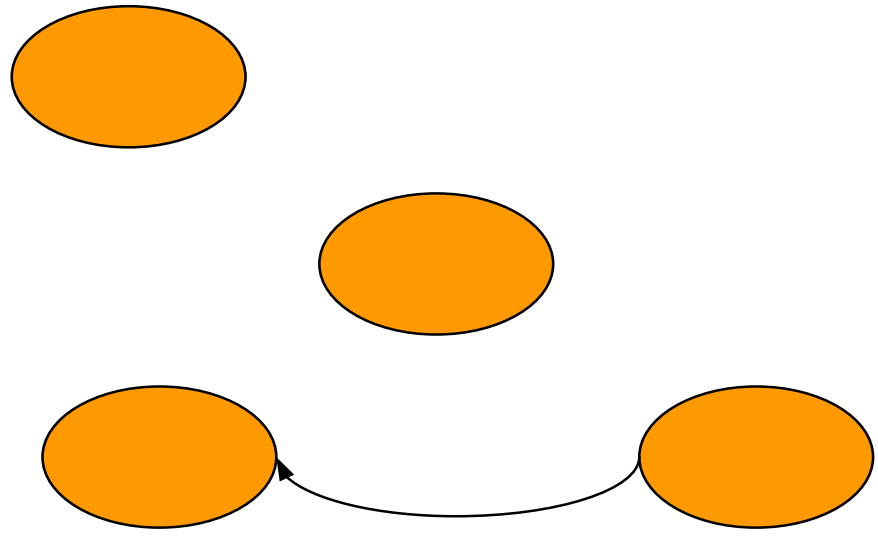


Figure 3-2 Bluetooth Subsystem Power Up and Power Down

The Bluetooth subsystem power up and power down is similar to the WLAN subsystem. A typical startup for the Bluetooth subsystem is as follows:

(1)VBAT, VDD_IO is applied.

(2)Release BT_RSTN pin from low to high.

(3)The host should wait 30ms after the BT_RSTN release for the on-chip PMU to stabilize.

(4)Bluetooth subsystem is now in the Sleep state.

(5)The host should now wake the Bluetooth subsystem by pull up BT_HOST_WKUP pin.

(6)Within T_{stable}ms, the reference clock should be stable and the system can start using it.

(7)The host and Bluetooth subsystem will synchronous baud rate through the UART interface.

(8)The host can download firmware by further UART write.

(9)Bluetooth subsystem will begin to initialize.

(10)Once initialized, which includes a series of messages passing between the host and the Bluetooth subsystem, the Bluetooth subsystem may not have anything further to do and will enter the sleep state if Host pull down BT_HOST_WKUP pin.

To power down the Bluetooth subsystem, BT_RSTN has to be set to 0. There are no constraints on other input pins. VDD_IO is allowed to go down 20ms after all input signals have been set to 0 (avoid the influent current).

3.2Analog Power Supply

Table 3-1 Analog Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	Power supply	3.0	3.6	5.5	V
VDD33_PA	TX PA 3.3V power supply	3.0	3.3	3.6	V

VDD14_RX	RX LDO power supply	1.4	1.5	2	V
VDD14_TX	TX LDO power supply	1.4	1.5	2	V
VDD_SENSE	DCDC feedback	1.4	1.5	2	V
VDD12_CLK	Clock LDO power supply	1.14	1.2	1.26	V

3.3Digital Power Supply

Table 3-2 Digital Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD_IO	IO power supply	1.62	3.3	3.6	V
VDD25_EF	EFUSE power supply	2.3	2.5	2.7	V
VDD14_DIG	Digital LDO power supply	1.4	1.5	2	V
VDD12_DIG	Digital power supply	1	1.1	1.2	V
VDD_RTC	RTC power supply	1	1.1	1.2	V

3.4Power Consumption

Conditions： VBAT=3.6V; VDDIO=3.3V; Temp:25°C

Table 3-3 Power Consumption

WLAN State	Bluetooth State	DCDC Mode (mA)	LDO Mode (mA)
Standby	Standby	0.00078	0.00078
Sleep	Sleep	0.12	0.21
20M Mode RX DSSS/CCK 1M	Standby	29	62
20M Mode RX OFDM MCS7	Standby	35	75
40M Mode RX OFDM MCS7	Standby	41	88
20M Mode TX @16dBm, DSSS/CCK 11M	Standby	145	192
20M Mode TX @14dBm, OFDM MCS7	Standby	128	179
40M Mode TX @15dBm, OFDM MCS0	Standby	137	190
40M Mode TX @14dBm, OFDM MCS7	Standby	126	180
Standby	RX active DH1/2DH3/3DH5	19	41
Standby	TX active @5dbm DH1/2DH3/3DH5	42	90

4 Clocks

XR829 uses a reference clock and a low power clock.

For the reference clock, XR829 can either use an external reference clock source or generate its own reference using a XTAL and a built-in oscillator.

For the low power clock, XR829 can use an external 32KHz or 32.768 KHz clock. The low power clock is used during power save modes and used only for power controller module.

4.1 Reference Clock

Table 4-1 External Reference Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequency list using an external clock source	13	24	52	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	19.2	24	52	MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	uA

Clock frequency detection

An integrated automatic detection algorithm detects the reference clock frequency using the low power clock after a hardware reset.

Clock source detection

An integrated automatic detection mechanism detects the clock source from the connections of the XTAL1 and XTAL2 pins:

• When an external reference clock source is used, the clock input pin is XTAL2. The XR829 supports both an analog and digital source. An analog source shall be AC coupled to XTAL2 while a digital source shall be DC coupled to XTAL2. In both cases, XTAL1 shall be DC grounded.

• When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to XTAL1 and XTAL2.

External Clock Source

• Requirements

Table 4-2 External Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
AC coupled signal					
F_{IN}	Frequency	13	24	52	MHz
V_{APP}	Peak-to-peak voltage range of the AC coupled analog input	0.4	0.5	1.2	Vpp
N_H	Total harmonic content of the input signal	-	-	-25	dBc
DC coupled signal					
V_{IL}	input low voltage on XTAL2	0	-	0.3*V18	V
V_{IH}	input high voltage on XTAL2	0.7*V18	-	V18	V
T_r/T_f	10%-90% rise and fall time	-	-	5	ns
Duty cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					
Z_{INRE}	Real part of parallel AC input impedance at the pin	30	-	-	kΩ
Z_{INIM}	Imaginary part of parallel AC input impedance at the pin	-	3.5	5	pF
Z_{DC}	DC input impedance	1	-	-	MΩ
Phase noise	Ref clock @ 24 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -123 -133 -138 -138	dBc/Hz

External XTAL and Built-in Oscillator

Table 4-3 External Crystal Characteristics Requirements

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range		13	24	52	MHz
ESR		-	-	60	Ω
C_{in_xtal}(1)	Single-ended	0	3	15	pF
C_{shunt}(1)		-	2	-	pF
Load capacitance(1)		0	16	27	pF
Crystal frequency accuracy at nominal temperature	25 °C	-10	-	+10	ppm
Crystal drift due to temperature	-20 °C to +85 °C	-10	-	+10	ppm
Crystal pull ability		10	-	150	ppm/pF

(1)The load capacitance value (C_{load}) and shunt capacitance (C_{shunt}) depends on XTAL model, XTAL1 and XTAL2 pin have inside capacitance (C_{in_xtal}), so external added load capacitance value(PCB Welding Capacitance) $C_{load\_ext} = C_{load} * 2 - C_{in\_xtal} - C_{pcb} - C_{shunt} * 2$, C_{pcb} is PCB parasitic capacitance(Single ended). C_{in_xtal} has tuning range about 15pF, which is

controlled by software, for details please go to software user manual.

4.2Low Power Clock

Table 4-4 Low Power Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Frequency	-	32/32.768	-	kHz
F/F_{IN}	Frequency accuracy	-250	-	+250	ppm
Duty cycle		30	-	70	%
Jitter	Cycle-to-cycle	-40	-	+40	ns
R_{in}	Input resistance	1	-	-	MΩ
C_{in}	Input capacitance	-	-	5	pF
V_{IL}	Input low voltage on LPCLK	0	-	0.4	V
V_{IH}	Input high voltage on LPCLK	VDD_IO- 0.4	-	VDD_IO	V

5 Electrical Characteristics

5.1Absolute Maximum Rating

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 5-1 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VBAT	3.0~5.5V power supply	-0.3	5.8	V
VDD_IO	IO power supply	-0.3	4.0	V
Vin	Input voltage on any digital pin	-0.3	3.6	V
T_{stg}	Storage temperature	-40	150	°C
T_a	Ambient operating temperature	-40	85	°C
Humidity	Storage Operation	5 10	95 93	% %
VESD	HBM	-4000	+4000	V
VESD	CDM	-800	+800	V

5.2Digital IO Pin DC Characteristics

Table 5-2 IO DC Characteristics (VDD_IO=3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input high voltage	2.06	-	3.6	V
V_{IL}	Input low voltage	-0.3	-	1.32	V
V_{OH}	Output high voltage	2.4	-	3.6	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
R_{PU}	Input pull-up resistance	40	66	110	kΩ
R_{PD}	Input pull-down resistance	40	66	110	kΩ

Table 5-3 IO DC Characteristics (VDD_IO=1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input high voltage	1.18	-	2	V
V_{IL}	Input low voltage	-0.3	-	0.65	V
V_{OH}	Output high voltage	1.44	-	2	V
V_{OL}	Output low voltage	-0.3	-	0.4	V

R_{PU}	Input pull-up resistance	80	135	210	kΩ
R_{PD}	Input pull-down resistance	80	135	210	kΩ

6 Transceiver/Receiver Performance

6.1WLAN Performance

Conditions： VBAT=3.6V; VDDIO=3.3V; Temp:25 °C

Table 6-1 WLAN Transceiver/Receiver Performance

Parameter	Description	Performance			Unit
		Min	Typ	Max	
Frequency range	Center channel frequency	2412	-	2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS	-	-97	-	dBm
	2Mbps DSSS	-	-95	-	dBm
	5.5Mbps CCK	-	-93	-	dBm
	11Mbps CCK	-	-90	-	dBm
RX Sensitivity (802.11g)	6Mbps OFDM	-	-92	-	dBm
	9Mbps OFDM	-	-92	-	dBm
	12Mbps OFDM	-	-91	-	dBm
	18Mbps OFDM	-	-88	-	dBm
	24Mbps OFDM	-	-86	-	dBm
	36Mbps OFDM	-	-82	-	dBm
	48Mbps OFDM	-	-78	-	dBm
	54Mbps OFDM	-	-76	-	dBm
RX Sensitivity (802.11n, 20MHz)	MCS0	-	-91	-	dBm
	MCS1	-	-87	-	dBm
	MCS2	-	-85	-	dBm
	MCS3	-	-83	-	dBm
	MCS4	-	-79	-	dBm
	MCS5	-	-75	-	dBm
	MCS6	-	-74	-	dBm
	MCS7	-	-72	-	dBm
RX Sensitivity (802.11n, 40MHz)	MCS0	-	-89	-	dBm
	MCS1	-	-87.5	-	dBm
	MCS2	-	-84.5	-	dBm

	MCS3	-	-81.5	-	dBm
	MCS4	-	-78	-	dBm
	MCS5	-	-74	-	dBm
	MCS6	-	-72	-	dBm
	MCS7	-	-71	-	dBm
Maximum Input Level	11b@11Mbps CCK	-	-10	-	dBm
	11g@54Mbps OFDM	-	-20	-	dBm
	11n@ HT20, MCS 7	-	-20	-	dBm
	11n@ HT40, MCS 7	-	-20	-	dBm
TX Power	1Mbps DSSS	-	20	-	dBm
	11Mbps CCK	-	20	-	dBm
	6Mbps OFDM	-	20	-	dBm
	54Mbps OFDM	-	19	-	dBm
	HT20, MCS 0	-	17.5	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	HT40, MCS 0	-	16	-	dBm
	HT40, MCS 7	-	17	-	dBm

6.2Bluetooth Performance

Conditions： VBAT=3.6V; VDDIO=3.3V; Temp:25 °C

Table 6-2 Bluetooth Transceiver/Receiver Performance

Parameter	**Description**	**Performance**			**Unit**
		Min	**Typ**	**Max**	
Frequency range	Center channel frequency	2402	-	2480	MHz
RX Sensitivity (BR)	1Mbps GFSK	-	-91	-	dBm
RX Sensitivity (EDR)	2Mbps π/4-DQPSK	-	-93	-	dBm
	3Mbps 8DPSK	-	-85	-	dBm
RX Sensitivity (BLE)	1Mbps GFSK	-	-93	-	dBm
Maximum Input Level	1Mbps GFSK	-	-20	-	dBm
	2Mbps π/4-DQPSK	-	-20	-	dBm
	3Mbps 8DPSK	-	-10	-	dBm
TX Out Power	Class1, Class2, Class3	-17	7	-	dBm

	@BR, EDR				
	BLE	-	7	-	dBm

7 Package Outline & PCB Layout Design

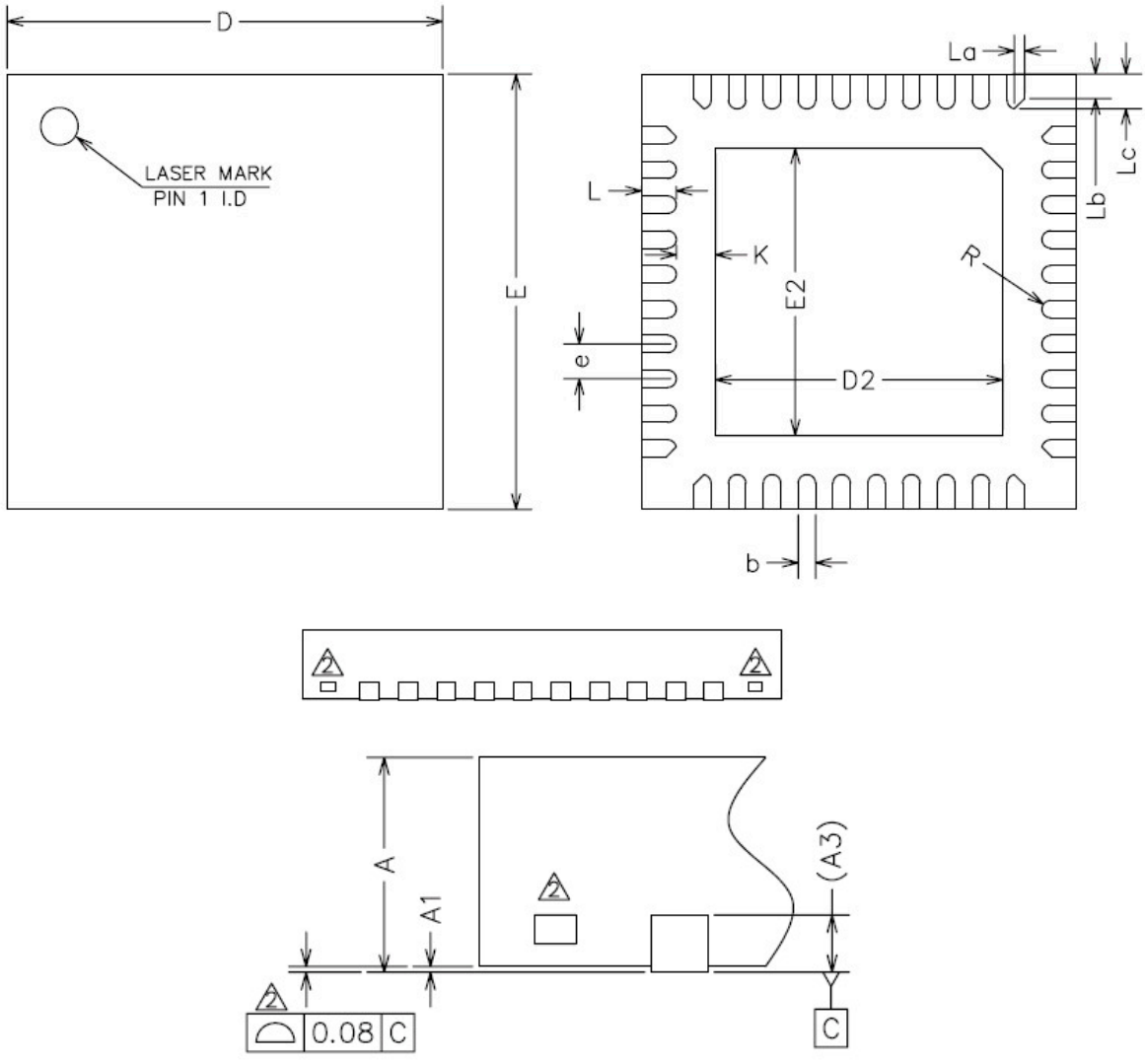


Figure 7-1 Package Dimensions

Table 7-1 Package Dimensions

Symbol	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0	0.02	0.05	mm
A3	0.20REF			mm
b	0.15	0.20	0.25	mm
D	4.90	5.00	5.10	mm
E	4.90	5.00	5.10	mm
D2	3.15	3.30	3.45	mm
E2	3.15	3.30	3.45	mm
e	0.30	0.40	0.50	mm

K	0.20	-	-	mm
L	0.30	0.40	0.50	mm
R	0.09	-	-	mm
La	0.12	0.15	0.18	mm
Lb	0.23	0.26	0.29	mm
Lc	0.30	0.39	0.50	mm

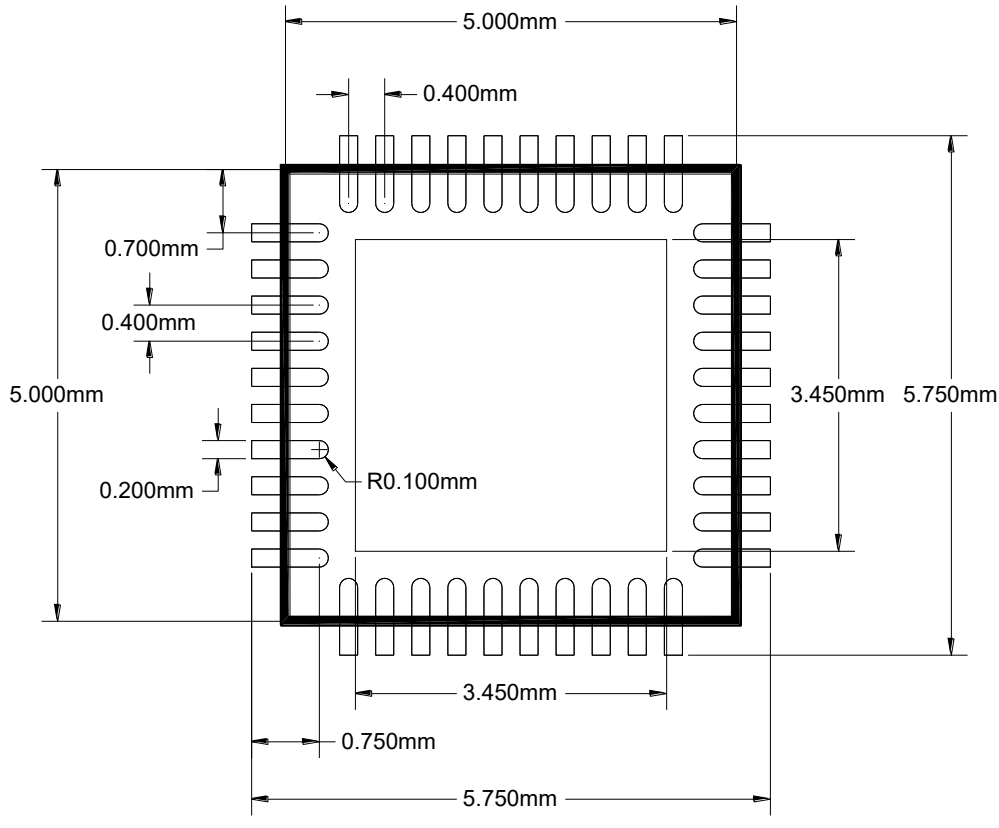


Figure 7-2 Example for PCB Layout Design

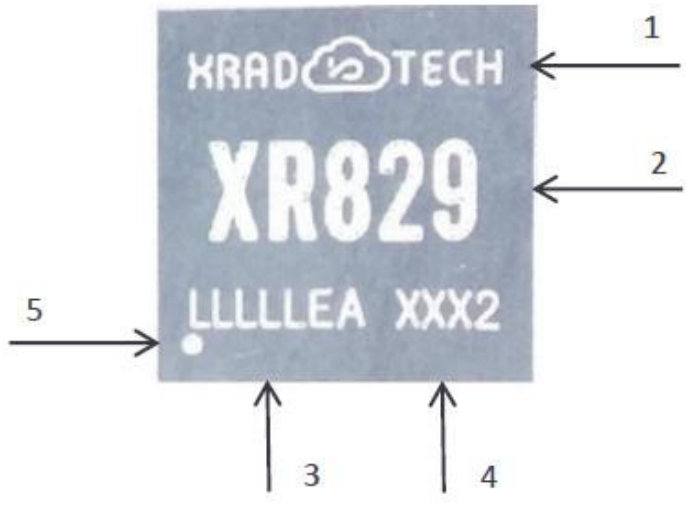


Figure 7-3 XR829 Marking (Top View)

Table 7-2. XR829 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1		Xradio logo or name	Fixed
2	XR829	Product name	Fixed
3	LLLLLEA	Lot number	Dynamic
4	XXX2	Date code	Dynamic
5		Package pin 1 identifier (the white dot in the bottom left corner)	Fixed

8 Package Thermal Characteristics

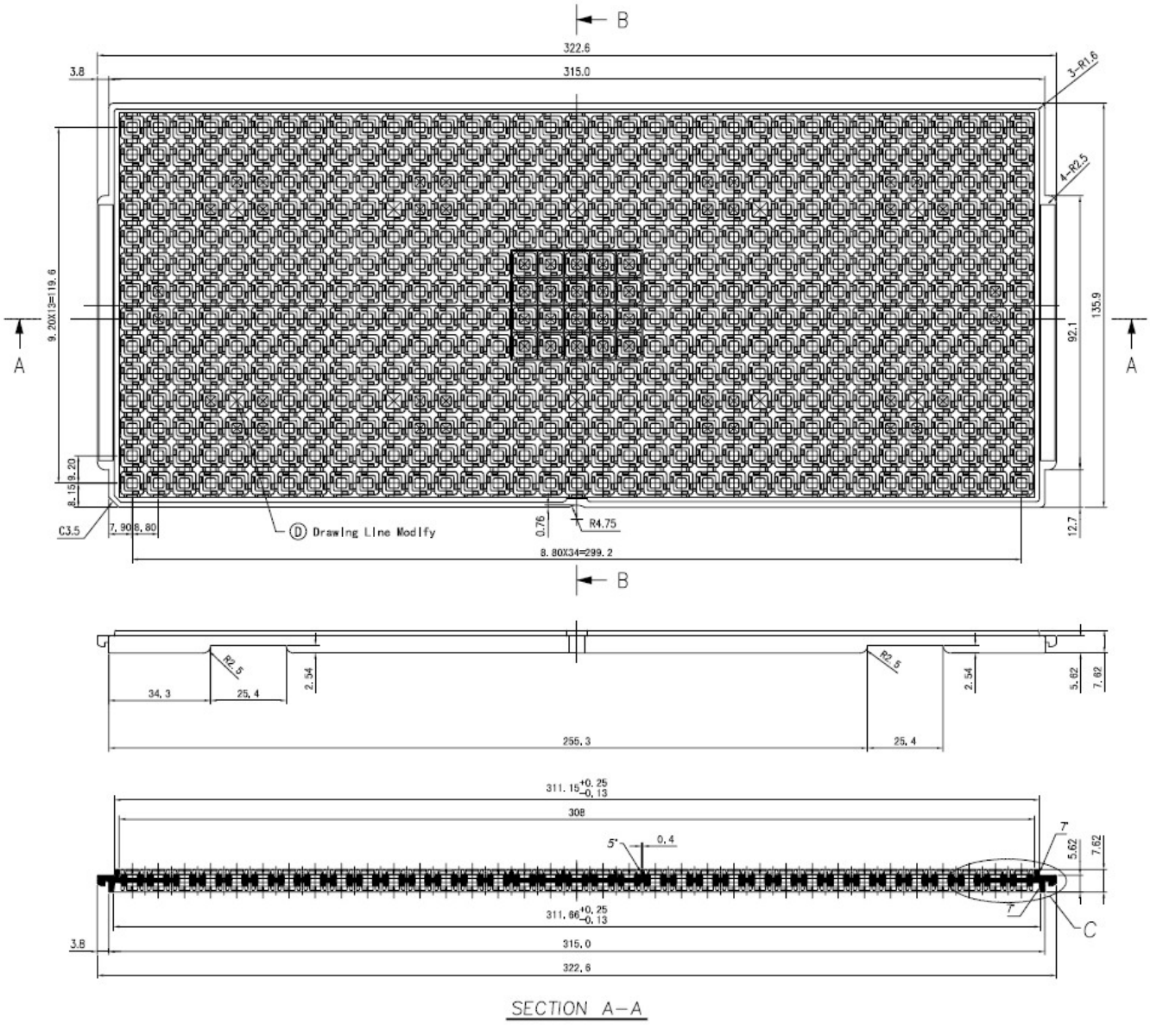
Table 8-1 Thermal Resistance Characteristics

Symbol	Parameter	Conditions	Type	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	28	^{o}C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	8.5	^{o}C /W
Θ_{JC}	Junction-to-Case	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	9.2	^{o}C /W

9 Carrier Information

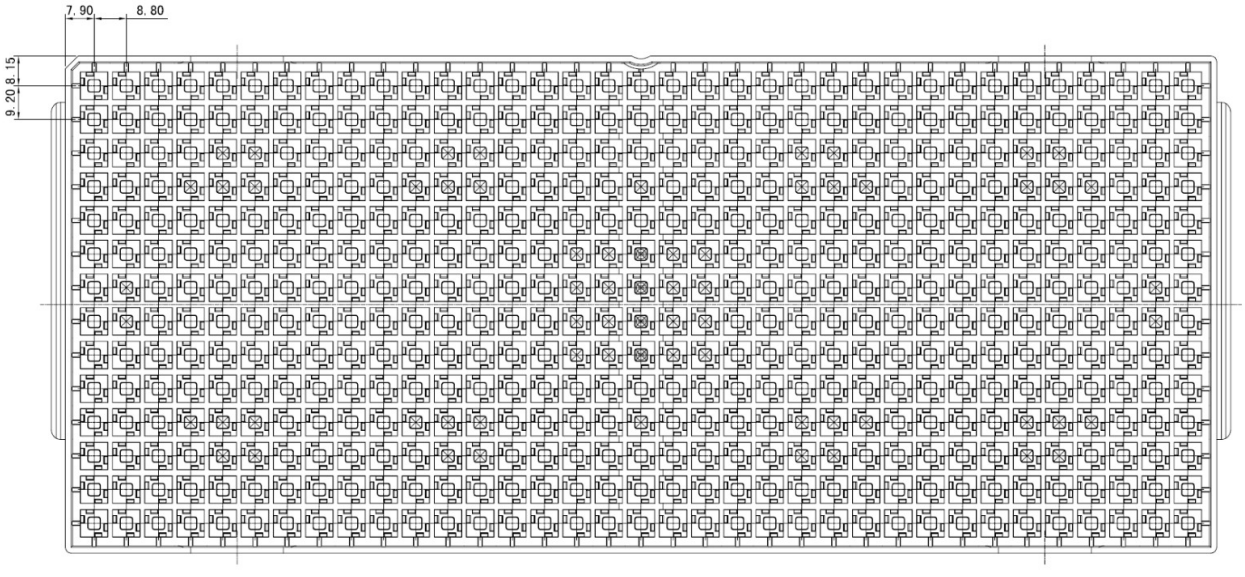
XR829 use two kinds of carriers for customer delivery and production, which are tray carrier and tape reel carrier. Each tray has 490ps of chips, while each tape reel provides 4900ps samples.

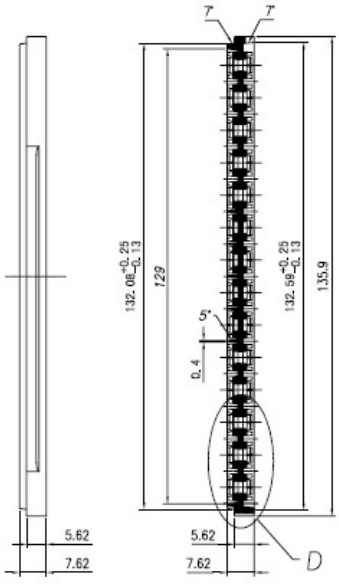
9.1Tray Carrier

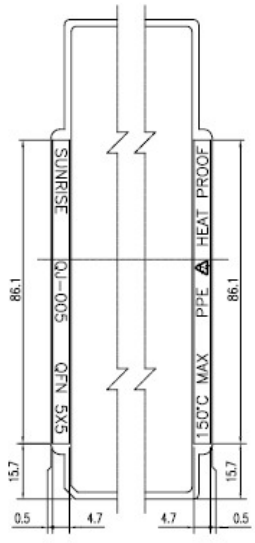


NOTE :

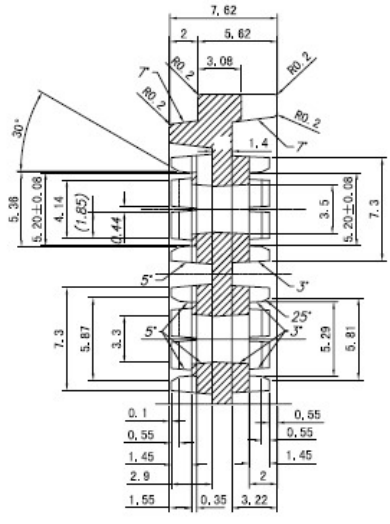
1. HEAT RESISTANCE UP TO 24 HOURS 150°C.
2. SURFACE ELECTRIC RESISTIVITY LESS THAN $10^{12}\Omega$ /sq.
3. WARPAGE IS WITHIN 0.76mm.
4. TOLERANCE : X=±0.5mm
   X.X=±0.25mm
   X.XX=±0.13mm
5. Material : PPE+Carbon Fiber.



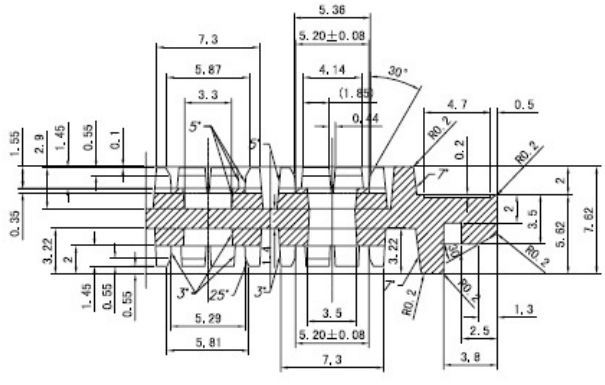




SECTION B–B

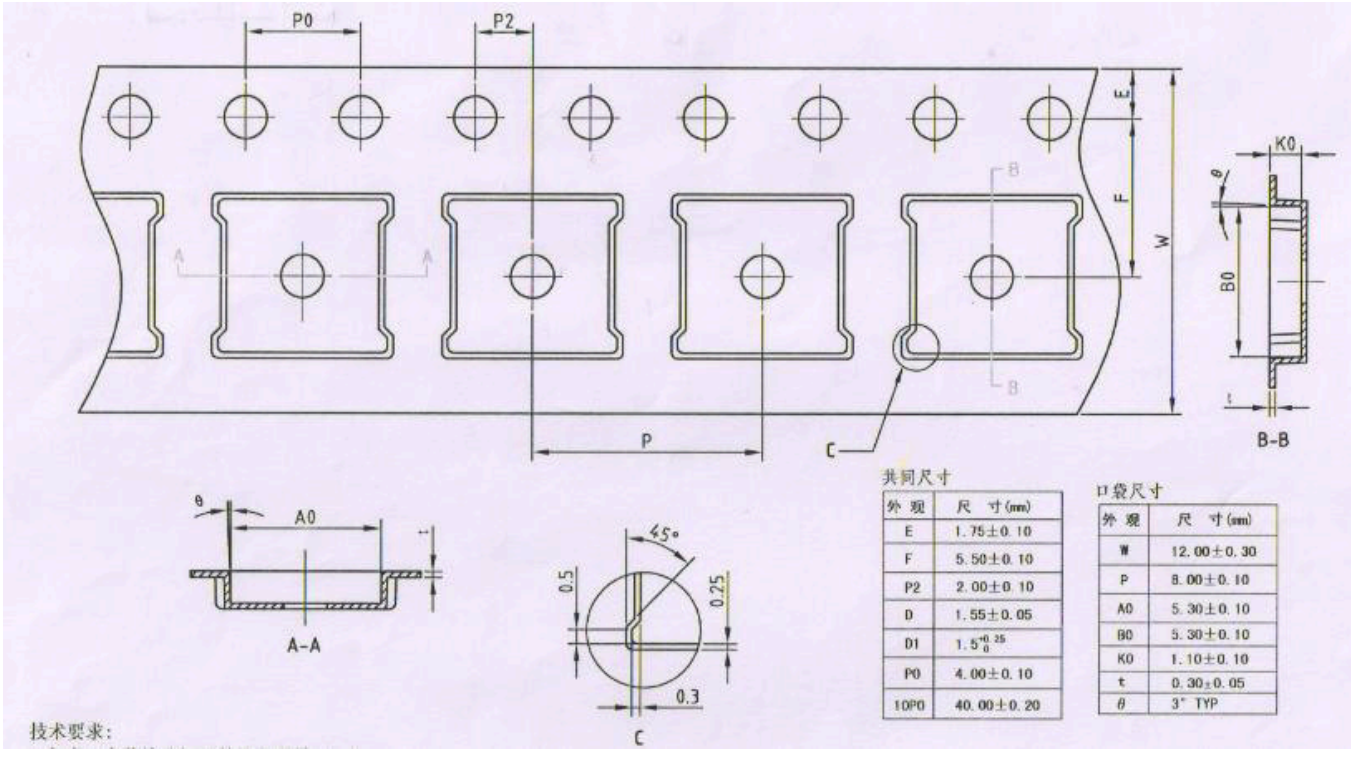


DETAIL D
SCALE: 4/1



DETAIL C
SCALE: 4/1

9.2Tape Reel Carrier



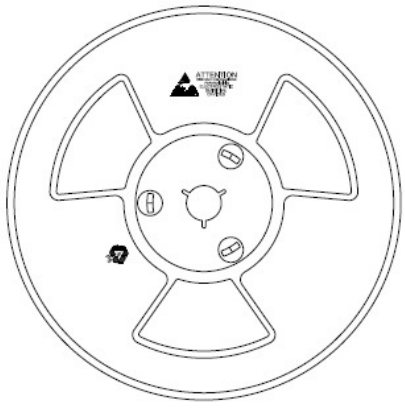
共同尺寸

外 观	尺 寸(mm)
E	1.75±0.10
F	5.50±0.10
P2	2.00±0.10
D	1.55±0.05
D1	$1.5^{+0.25}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

口袋尺寸

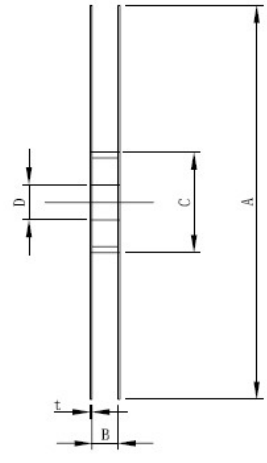
外 观	尺 寸(mm)
W	12.00±0.30
P	8.00±0.10
A0	5.30±0.10
B0	5.30±0.10
K0	1.10±0.10
t	0.30±0.05
θ	3° TYP

技术要求：

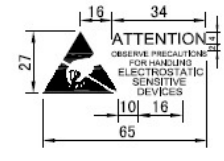


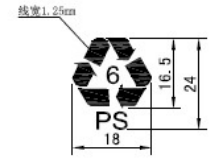
⚠

SCALE: 1 : 1



SECTION A-A





⚠ 技术要求：

1. 颜色：蓝色。
2. 未注公差为±0.20mm；
3. 盘面光洁，无翘曲变形、杂质等缺陷；
4. 外包装良好，无破损；
5. 表面电阻率：10^5~10^{10} Ω/□。
6. 卷盘表面除指定的标识外，其余依供应商而定。

圆盘基本尺寸 (mm)					
载带宽度	A	B	C	D	t
12	⌀329±1	12.8±1	⌀100±1	⌀13.3±0.3	2.0±0.3