

### General Description

The CMSC1653 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. This device is well suited for use in compact DC/DC converter applications.

### Features

- 30V,30A, RDS(ON) =7mΩ @VGS = 10V
- Low Gate Charge
- High Current Capability
- RoHS Compliant

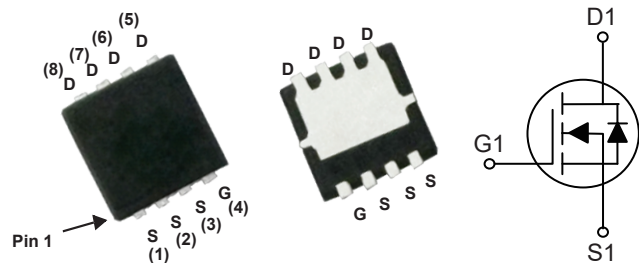
### Product Summary

BVDSS	RDS(ON)	ID
30V	7mΩ	30A

### Applications

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

### DFN-8 3.3x3.3 Pin Configuration



Type	Package	Marking
CMSC1653	DFN-8 3.3*3.3	1653

### Maximum Ratings and Thermal Characteristics (T<sub>A</sub> = 25 °C unless otherwise noted)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25 °C	Continuous Drain Current	30	A
I <sub>D</sub> @T <sub>C</sub> =100 °C		22	A
I <sub>DM</sub>	Pulsed Drain Current	60	A
EAS	Single Pulse Avalanche Energy <sup>1</sup>	65	mJ
P <sub>D</sub> @T <sub>C</sub> =25 °C	Total Power Dissipation	25	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-ambient(Steady-State)	---	90	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction -Case(Steady-State)	---	5.4	°C/W

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250μA	30	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =20A	---	---	7	mΩ
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =20A	---	---	12	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	1	---	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =30V , V <sub>GS</sub> =0V	---	---	1	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =5A	---	18	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz	---	1.3	---	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V , V <sub>GS</sub> =10V , I <sub>D</sub> =13A	---	8	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =15V , V <sub>GS</sub> =10V , R <sub>L</sub> =1.2Ω R <sub>GEN</sub> =3Ω	---	3.5	---	ns
T <sub>r</sub>	Rise Time		---	2.8	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	16.5	---	
T <sub>f</sub>	Fall Time		---	3	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz	---	1400	---	pF
C <sub>oss</sub>	Output Capacitance		---	230	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	28	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	30	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V , I <sub>S</sub> =20A	---	---	1	V

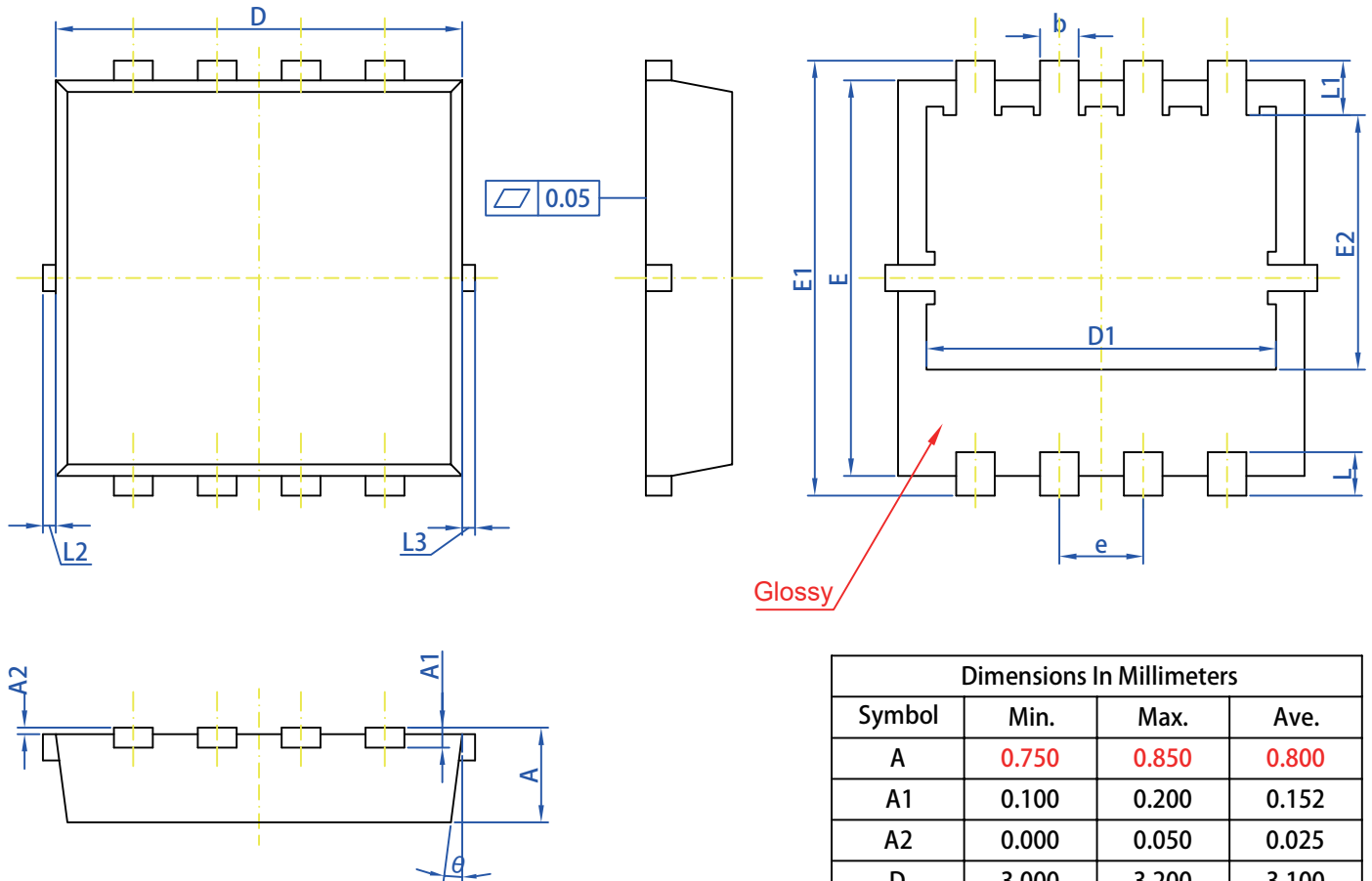
Notes:

1. L=1.3mH , I<sub>AS</sub>=10A , V<sub>D</sub>=15V , Starting T<sub>J</sub>=25 C .

This product has been designed and qualified for the consumer market.  
Cmos assumes no liability for customers' product design or applications.  
Cmos reserves the right to improve product design ,functions and reliability without notice.

Package Dimensions

DFN-8 3.3\*3.3 Package Outline Drawing



Dimensions In Millimeters			
Symbol	Min.	Max.	Ave.
A	0.750	0.850	0.800
A1	0.100	0.200	0.152
A2	0.000	0.050	0.025
D	3.000	3.200	3.100
D1	2.610	2.810	2.710
E	3.000	3.200	3.100
E1	3.300	3.500	3.400
E2	1.830	2.030	1.930
b	0.200	0.400	0.300
e	0.550	0.750	0.650
L	0.350	0.550	0.450
L1	0.365	0.565	0.455
L2	0~0.100		
L3	0~0.100		
$\theta$	6°	12°	9°

Note:

1. Smooth surface Ra=0.1; unmarked surface is matte surface Ra=1.0~1.2
2. Unmarked tolerance  $\pm 0.05$ , unmarked fillet, R max=0.25
3. The plastic package has no defects such as defects, shrinkage holes, cracks, bubbles, etc.
4. Marking unit mm
5. Misalignment between the center of the plastic package and the center of the lead frame  $\leq 0.05$