Revision 0.0 Customer Acceptance Specification May 08

# DF39079LIDFZV

## Customer Specification

RENESAS

Everywhere you imagine.

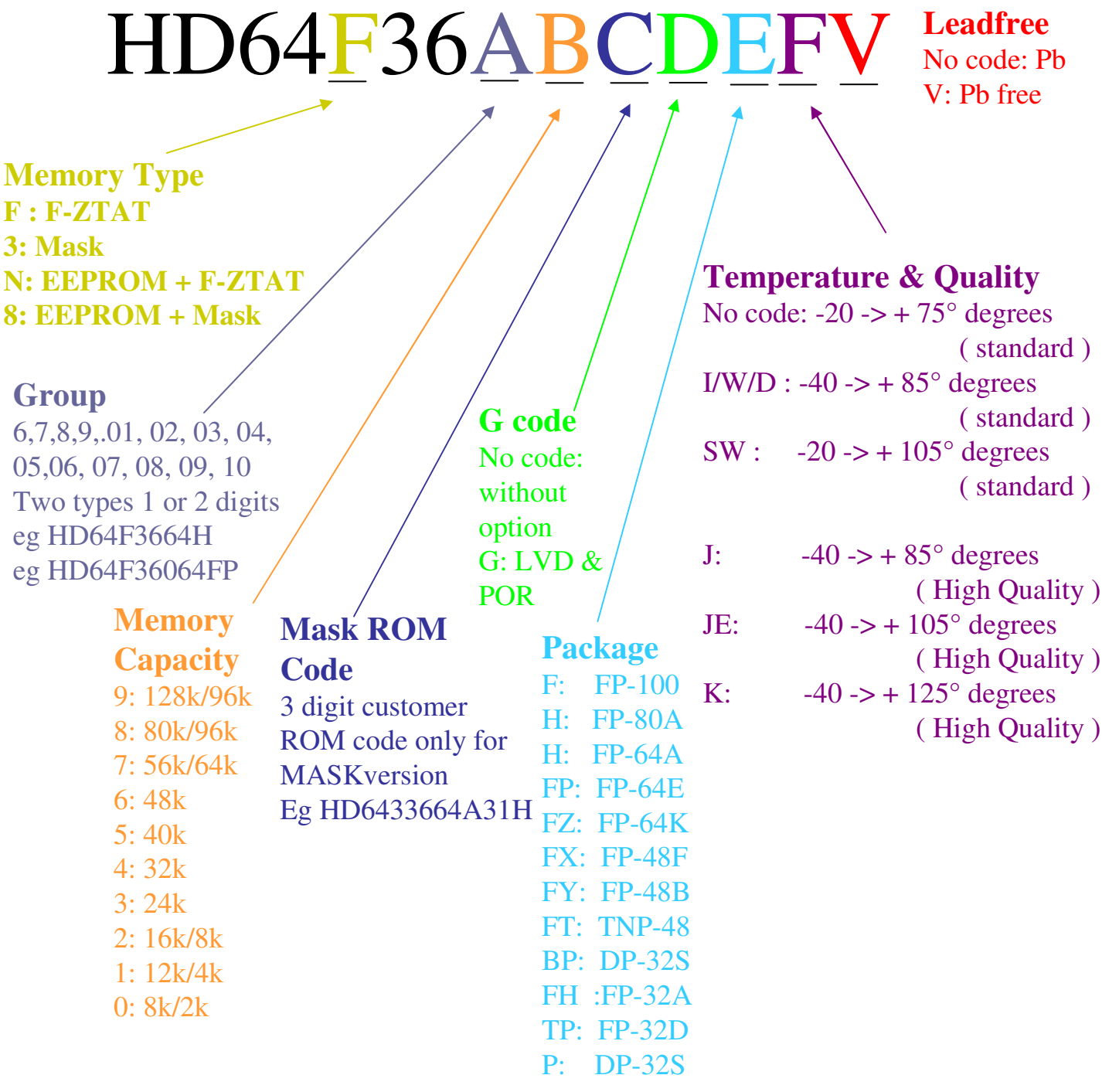
# H8/36079 Series Part Number System

## H8/36079 Series

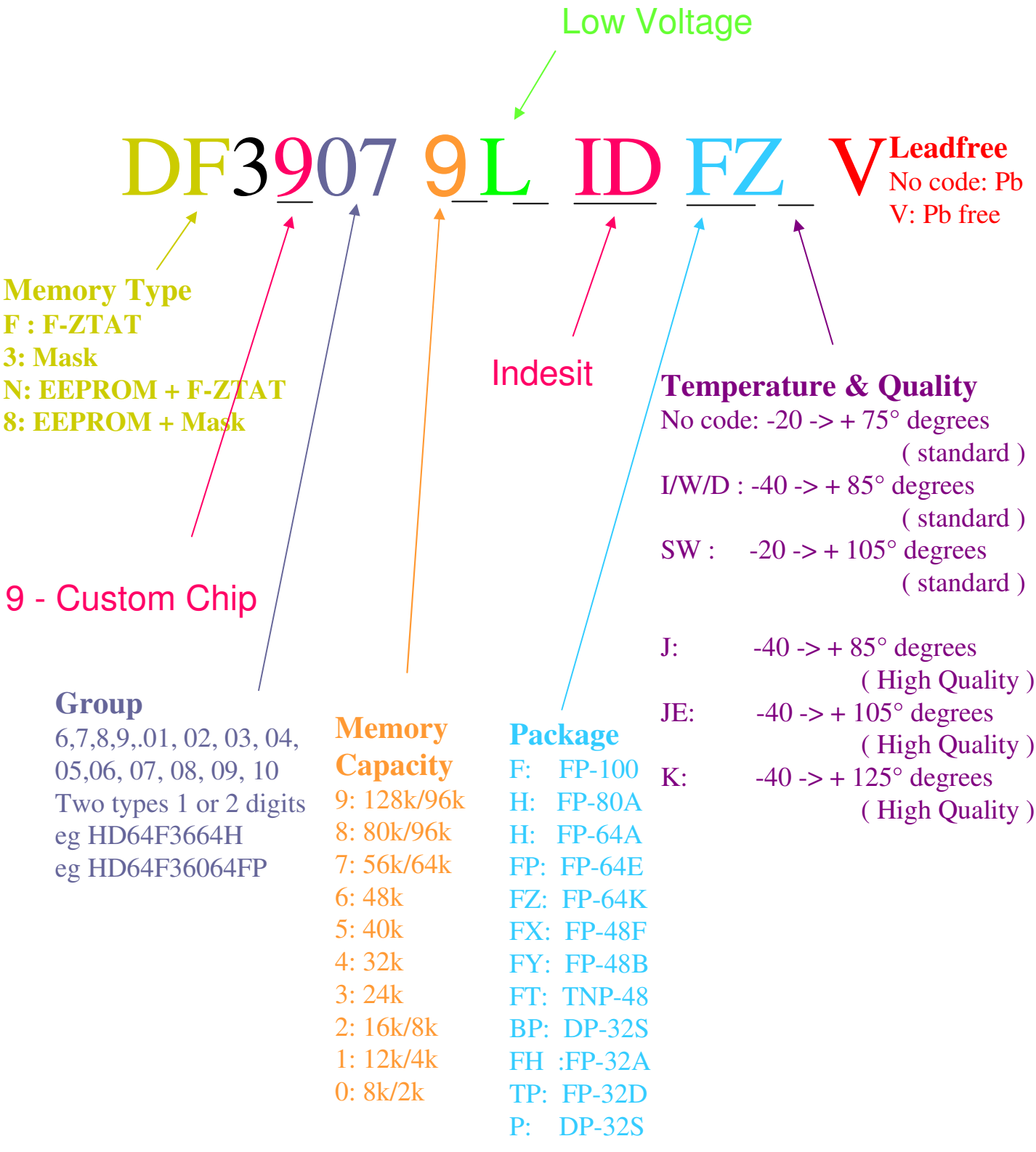
**Oct-08**

| Device | Type | Operating Temperature | Operating Voltage/ Maximum Clock Rate | POR | LVD | Package | Product Name | Renesas Order Code |
|---|---|---|---|---|---|---|---|---|
| H8/36079(128K/6K) | F-ZTAT (128K/6K) | Regular | Vcc=4.0 to 5.5V f=20MHz | Yes | Yes | FP-64A | HD64F36079GHV | DF36079GHV |
| | | | | | | FP-64K | HD64F36079GFZV | DF36079GFZV |
| | | I version | | | | FP-64A | HD64F36079GHWV | DF36079GHWV |
| | | | | | | FP-64K | HD64F36079GFZWV | DF36079GFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36079GHSWV | DF36079GHSWV |
| | | | | | | FP-64K | HD64F36079GFZSW\ | DF36079GFZSWV |
| | | Regular | Vcc=3.0 to 3.6V f=16MHz | Yes | Yes | FP-64A | HD64F36079LHV | DF36079LHV |
| | | | | | | FP-64K | HD64F36079LFZV | DF36079LFZV |
| | | I version | | | | FP-64A | HD64F36079LHWV | DF36079LHWV |
| | | | | | | FP-64K | HD64F36079LFZWV | DF36079LFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36079LHSWV | DF36079LHSWV |
| | | | | | | FP-64K | HD64F36079LFZSWV | DF36079LFZSWV |
| H8/36078(96K/6K) | F-ZTAT (96K/6K) | Regular | Vcc=4.0 to 5.5V f=20MHz | Yes | Yes | FP-64A | HD64F36078GHV | DF36078GHV |
| | | | | | | FP-64K | HD64F36078GFZV | DF36078GFZV |
| | | I version | | | | FP-64A | HD64F36078GHWV | DF36078GHWV |
| | | | | | | FP-64K | HD64F36078GFZWV | DF36078GFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36078GHSWV | DF36078GHSWV |
| | | | | | | FP-64K | HD64F36078GFZSW\ | DF36078GFZSWV |
| | | Regular | Vcc=3.0 to 3.6V f=16MHz | Yes | Yes | FP-64A | HD64F36078LHV | DF36078LHV |
| | | | | | | FP-64K | HD64F36078LFZV | DF36078LFZV |
| | | I version | | | | FP-64A | HD64F36078LHWV | DF36078LHWV |
| | | | | | | FP-64K | HD64F36078LFZWV | DF36078LFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36078LHSWV | DF36078LHSWV |
| | | | | | | FP-64K | HD64F36078LFZSWV | DF36078LFZSWV |
| H8/36077(56K/4K) | F-ZTAT (56K/54K) | Regular | Vcc=4.0 to 5.5V f=20MHz | Yes | Yes | FP-64A | HD64F36077GHV | HD64F36077GHV |
| | | | | | | FP-64K | HD64F36077GFZV | HD64F36077GFZV |
| | | I version | | | | FP-64A | HD64F36077GHWV | DF36077GHWV |
| | | | | | | FP-64K | HD64F36077GFZWV | DF36077GFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36077GHSWV | DF36077GHSWV |
| | | | | | | FP-64K | HD64F36077GFZSW\ | DF36077GFZSWV |
| | | Regular | Vcc=3.0 to 3.6V f=16MHz | Yes | Yes | FP-64A | HD64F36077LHV | DF36077LHV |
| | | | | | | FP-64K | HD64F36077LFZV | DF36077LFZV |
| | | I version | | | | FP-64A | HD64F36077LHWV | DF36077LHWV |
| | | | | | | FP-64K | HD64F36077LFZWV | DF36077LFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36077LHSWV | DF36077LHSWV |
| | | | | | | FP-64K | HD64F36077LFZSWV | DF36077LFZSWV |
| H8/36074(32K/4K) | F-ZTAT (32K/4K) | Regular | Vcc=4.0 to 5.5V f=20MHz | Yes | Yes | FP-64A | HD64F36074GHV | DF36074GHV |
| | | | | | | FP-64K | HD64F36074GFZV | DF36074GFZV |
| | | I version | | | | FP-64A | HD64F36074GHWV | DF36074GHWV |
| | | | | | | FP-64K | HD64F36074GFZWV | DF36074GFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36074GHWV | DF36074GHWV |
| | | | | | | FP-64K | HD64F36074GFZSW\ | DF36074GFZWV |
| | | Regular | Vcc=3.0 to 3.6V f=16MHz | Yes | Yes | FP-64A | HD64F36074LHV | DF36074LHV |
| | | | | | | FP-64K | HD64F36074LFZV | DF36074LFZV |
| | | I version | | | | FP-64A | HD64F36074LHWV | DF36074LHWV |
| | | | | | | FP-64K | HD64F36074LFZWV | DF36074LFZWV |
| | | S version | Vcc=4.0 to 5.5V f=16MHz | | No | FP-64A | HD64F36074LHSWV | DF36074LHSWV |
| | | | | | | FP-64K | HD64F36074LFZSWV | DF36074LFZSWV |
| H8/39079(128K/6K) | F-ZTAT (128K / 6K) | Regular | Vcc=3.0 to 3.6V f=16MHz | Yes | Yes | FP-64K | HD64F39079LIDFZV | DF39079LIDFZV ( Indesit Custom Version ) |

The H8/300H Tiny Series Product Names are generally constructed according to the rules shown below. There are a limited number of exceptions to these rules.



# The H8/300H Tiny Series Custom part Number for Indesit



## 1. Absolute Maximum Ratings

**Table 1.1 Absolute Maximum Ratings**

| Item | | Symbol | Value | Unit | Note |
|---|---|---|---|---|---|
| Power supply voltage | | $V_{CC}$ | –0.3 to +7.0 | V | *1 |
| Analog power supply voltage | | $AV_{CC}$ | –0.3 to +7.0 | V | |
| Input voltage | Ports other than ports B and X1 | $V_{IN}$ | –0.3 to $V_{CC}$ +0.3 | V | |
| | Port B | | –0.3 to $AV_{CC}$ +0.3 | V | |
| | X1 | | –0.3 to 4.3 | V | |
| Operating temperature | | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C | |

Note: 1. Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

# 2. Electrical Characteristics

## 2.1 DC Characteristics

**Table 2.1.1 DC Characteristics (1)**

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| | | | | Values | | | | |
|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **Applicable Pins** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| Input high voltage | $V_{IH}$ | $\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TMIB1, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, SCK3, SCK3_2, TRGV | | $V_{CC} \times 0.9$ | — | $V_{CC}$ + 0.3 | V | |
| | | RXD, RXD_2, SCL, SDA, P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72 P74 to P76, P85 to P87, PC0, PC1 | | $V_{CC} \times 0.8$ | — | $V_{CC}$ + 0.3 | V | |
| | | PB0 to PB7 | $AV_{CC}$ = 3.0 to 3.6 V | $AV_{CC} \times 0.8$ | — | $AV_{CC}$ + 0.3 | V | |
| | | OSC1 | | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | |
| Input low voltage | $V_{IL}$ | $\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TMIB1, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, SCK3, SCK3_2, TRGV | | –0.3 | — | $V_{CC} \times 0.1$ | V | |

Note: Connect the TEST pin to Vss.

## ■ Electrical Characteristics

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Input low voltage | $V_{IL}$ | RXD, RXD_2, SCL, SDA, P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, PC0, PC1 | | –0.3 | — | $V_{CC} \times 0.2$ | V | |
| | | PB0 to PB7 | $AV_{CC}$ = 3.0 to 3.6 V | –0.3 | — | $AV_{CC} \times 0.2$ | V | |
| | | OSC1 | | –0.3 | — | 0.3 | V | |
| Output high voltage | $V_{OH}$ | P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P55, P60 to P67, P70 to P72, P74 to P76, P85 to P87, PC0, PC1 | $-I_{OH}$ = 1.5 mA | $V_{CC}$ – 1.0 | — | — | V | |
| | | | $-I_{OH}$ = 0.1 mA | $V_{CC}$ – 0.5 | — | — | | |
| | | P56, P57 | $-I_{OH}$ = 0.1 mA | $V_{CC}$ – 2.0 | — | — | V | |
| Output low voltage | $V_{OL}$ | P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P70 to P72, P74 to P76, P85 to P87 PC0, PC1 | $I_{OL}$ = 1.6 mA | — | — | 0.6 | V | |
| | | | $I_{OL}$ = 0.4 mA | — | — | 0.4 | | |
| | | P60 to P67 | $I_{OL}$ = 20.0 mA | — | — | 1.5 | V | |
| | | | $I_{OL}$ = 10.0 mA | — | — | 1.0 | | |
| | | | $I_{OL}$ = 1.6 mA | — | — | 0.4 | | |
| | | | $I_{OL}$ = 0.4 mA | — | — | 0.4 | | |
| | | SCL, SDA | $I_{OL}$ = 6.0 mA | — | — | 0.6 | | |
| | | | $I_{OL}$ = 3.0 mA | — | — | 0.4 | | |

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Input/ output leakage current | $\lvert I_{IL} \rvert$ | OSC1, TMIB1, $\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TRGV, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1 RXD, SCK3, RXD_2, SCK3_2, SCL, SDA | $V_{IN}$ = 0.5 V to ($V_{CC}$ – 0.5 V) | — | — | 1.0 | µA | |
| | | P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, PC0, PC1 | $V_{IN}$ = 0.5 V to ($V_{CC}$ – 0.5 V) | — | — | 1.0 | µA | |
| | | PB0 to PB7 | $V_{IN}$ = 0.5 V to ($AV_{CC}$ – 0.5 V) | — | — | 1.0 | µA | |
| Pull-up MOS current | $-I_p$ | P10 to P12, P14 to P17, P50 to P55 | $V_{CC}$ = 3.3 V, $V_{IN}$ = 0.0 V | — | 60.0 | — | µA | |
| Input capaci-tance | $C_{in}$ | All input pins except power supply pins | f = 4 MHz, $V_{IN}$ = 0.0 V, $T_a$ = 25°C | — | — | 15.0 | pF | |
| Active mode current consump-tion | $I_{OPE1}$ | $V_{CC}$ | Active mode 1 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 16 MHz | — | 15.0 | 22.0 | mA | * |
| | | | Active mode 1 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 10 MHz | — | 11.0 | — | | * Reference value |
| | $I_{OPE2}$ | $V_{CC}$ | Active mode 2 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 16 MHz | — | 2.8 | 4.0 | mA | * |
| | | | Active mode 2 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 10 MHz | — | 2.5 | — | | * Reference value |

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Sleep mode supply current | $I_{SLEEP1}$ | $V_{CC}$ | Sleep mode 1 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 16 MHz | — | 9.0 | 14.0 | mA | * |
| | | | Sleep mode 1 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 10 MHz | — | 6.5 | — | | * Reference value |
| | $I_{SLEEP2}$ | $V_{CC}$ | Sleep mode 2 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 16 MHz | — | 2.2 | 3.5 | mA | * |
| | | | Sleep mode 2 $V_{CC}$ = 3.3 V, $f_{OSC}$ = 10 MHz | — | 2.0 | — | | * Reference value |
| Subactive mode supply current | $I_{SUB}$ | $V_{CC}$ | $V_{CC}$ = 3.3 V 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$) | — | 95.0 | 145.0 | µA | * |
| | | | $V_{CC}$ = 3.3 V 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/8$) | — | 85.0 | — | | * Reference value |
| Subsleep mode supply current | $I_{SUBSP}$ | $V_{CC}$ | $V_{CC}$ = 3.3 V 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$) | — | 85.0 | 140.0 | µA | * |
| Standby mode supply current | $I_{STBY}$ | $V_{CC}$ | 32-kHz crystal resonator not used | — | — | 135.0 | µA | * |
| RAM data retention voltage | $V_{RAM}$ | $V_{CC}$ | | 2.0 | — | — | V | |

Note: * Pin states during supply current measurement are given below (excluding current in the pull-up MOS transistors and output buffers).

| Mode | $\overline{RES}$ Pin | Internal State | Other Pins | Oscillator Pins |
|---|---|---|---|---|
| Active mode 1 | $V_{CC}$ | Operates | $V_{CC}$ | Main clock: ceramic or crystal resonator, and on-chip oscillator |
| Active mode 2 | | Operates ($\phi_{OSC}$/64) | | Subclock: Pin X1 = $V_{SS}$ |
| Sleep mode 1 | $V_{CC}$ | Only timers operate | $V_{CC}$ | |
| Sleep mode 2 | | Only timers operate ($\phi_{OSC}$/64) | | |
| Subactive mode | $V_{CC}$ | Operates | $V_{CC}$ | Main clock: ceramic or crystal resonator, and on-chip oscillator |
| Subsleep mode | $V_{CC}$ | Only timers operate | $V_{CC}$ | Subclock: crystal resonator |
| Standby mode | $V_{CC}$ | CPU and timers both stop | $V_{CC}$ | Main clock: ceramic or crystal resonator, and on-chip oscillator<br>Subclock: Pin X1 = $V_{SS}$ |

**Table 2.2.2 DC Characteristics (2)**

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | Symbol | Applicable Pins | Test Condition | Values Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | $I_{OL}$ | Output pins except port 6, SCL, and SDA | | — | — | 2.0 | mA |
| | | Port 6 | | — | — | 20.0 | |
| Permissible output low current (total) | $\Sigma I_{OL}$ | Output pins except port 6, SCL, and SDA | | — | — | 40.0 | mA |
| | | Port 6, SCL, and SDA | | — | — | 80.0 | |
| Permissible output high current (per pin) | $\lvert -I_{OH} \rvert$ | All output pins | | — | — | 5.0 | mA |
| Permissible output high current (total) | $\lvert -\Sigma I_{OH} \rvert$ | All output pins | | — | — | 50.0 | mA |

## 2.2 AC Characteristics

### Table 2.2.1 AC Characteristics

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| System clock oscillation frequency | $f_{OSC}$ | OSC1, OSC2 | | 4.0 | — | 16.0 | MHz | *1 |
| System clock ($\phi$) cycle time | $t_{cyc}$ | | | 1 | — | 64 | $t_{OSC}$ | *2 |
| | | | | — | — | 12.8 | µs | |
| Subclock oscillation frequency | $f_W$ | X1, X2 | | — | 32.768 | — | kHz | |
| Watch clock ($\phi_W$) cycle time | $t_W$ | X1, X2 | | — | 30.5 | — | µs | |
| Subclock ($\phi_{SUB}$) cycle time | $t_{subcyc}$ | | | 2 | — | 8 | $t_W$ | *2 |
| Instruction cycle time | | | | 2 | — | — | $t_{cyc}$ $t_{subcyc}$ | |
| Oscillation stabilization time (crystal resonator) | $t_{rc}$ | OSC1, OSC2 | | — | — | 10.0 | ms | |
| Oscillation stabilization time (ceramic resonator) | $t_{rc}$ | OSC1, OSC2 | | — | — | 5.0 | ms | |
| Oscillation stabilization time (on-chip oscillator) | $t_{rc}$ | | | — | — | 500 | µs | |
| Oscillation stabilization time | $t_{rcx}$ | X1, X2 | | — | — | 2.0 | s | |
| External clock high width | $t_{CPH}$ | OSC1 | | 23.8 | — | — | ns | Figure 2.3.1 |
| External clock low width | $t_{CPL}$ | OSC1 | | 23.8 | — | — | ns | |
| External clock rise time | $t_{CPr}$ | OSC1 | | — | — | 15.0 | ns | |
| External clock fall time | $t_{CPf}$ | OSC1 | | — | — | 15.0 | ns | |

| Item | Symbol | Applicable Pins | Test Condition | Values Min. | Typ. | Max. | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| $\overline{RES}$ pin low width | $t_{REL}$ | $\overline{RES}$ | At power-on and in modes other than those below | $t_{rc}$ | — | — | ms | Figure 2.3.2 |
| | | | In active mode and sleep mode | 2500 | — | — | ns | |
| Input pin high width | $t_{IH}$ | $\overline{NMI}$, TMIB1, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1 | | 2 | — | — | $t_{cyc}$ $t_{subcyc}$ | Figure 2.3.3 |
| Input pin low width | $t_{IL}$ | $\overline{NMI}$, TMIB1, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1 | | 2 | — | — | $t_{cyc}$ $t_{subcyc}$ | |
| On-chip oscillator oscillation frequency | $f_{RC}$ | | Vcc = 3.3 V, Ta = 25°C, FSEL = 1, VCLSEL = 0 | 19.70 | 20.00 | 20.30 | MHz | |
| | | | FSEL = 1, VCLSEL = 0 | 19.40 | 20.00 | 20.60 | | |
| | | | Vcc = 3.3 V, Ta = 25°C, FSEL = 0, VCLSEL = 0 | 15.84 | 16.00 | 16.16 | | |
| | | | FSEL = 0, VCLSEL = 0 | 15.52 | 16.00 | 16.48 | | |

Notes: 1. When an external clock is input, the minimum frequency of the external clock oscillator is 4.0 MHz.
2. Determined by MA2 to MA0, SA1, and SA0 in system control register 2 (SYSCR2).

### Table 2.2.2 $I^2C$ Bus Interface Timing

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | Symbol | Test Condition | Values | | | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| SCL input cycle time | $t_{SCL}$ | | $12t_{cyc}$ + 600 | — | — | ns | Figure 2.3.4 |
| SCL input high width | $t_{SCLH}$ | | $3t_{cyc}$ + 300 | — | — | ns | |
| SCL input low width | $t_{SCLL}$ | | $5t_{cyc}$ + 300 | — | — | ns | |
| SCL and SDA input fall time | $t_{Sf}$ | | — | — | 300 | ns | |
| SCL and SDA input spike pulse removal time | $t_{SP}$ | | — | — | $1t_{cyc}$ | ns | |
| SDA input bus-free time | $t_{BUF}$ | | $5t_{cyc}$ | — | — | ns | |
| Start condition input hold time | $t_{STAH}$ | | $3t_{cyc}$ | — | — | ns | |
| Repeated start condition input setup time | $t_{STAS}$ | | $3t_{cyc}$ | — | — | ns | |
| Setup time for stop condition input | $t_{STOS}$ | | $3t_{cyc}$ | — | — | ns | |
| Data-input setup time | $t_{SDAS}$ | | $1t_{cyc}$+20 | — | — | ns | |
| Data-input hold time | $t_{SDAH}$ | | 0 | — | — | ns | |
| Capacitive load of SCL and SDA | $c_b$ | | 0 | — | 400 | pF | |
| SCL and SDA output fall time | $t_{Sf}$ | | — | — | 250 | ns | |

### Table 2.2.3 Serial Communication Interface (SCI) Timing

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | | |
| Input clock cycle | Asynchronous | $t_{Scyc}$ | SCK3 | | 4 | — | — | $t_{cyc}$ | Figure 2.3.5 |
| | Clock synchronous | | | | 6 | — | — | | |
| Input clock pulse width | | $t_{SCKW}$ | SCK3 | | 0.4 | — | 0.6 | $t_{Scyc}$ | |
| Transmit data delay time (clock synchronous) | | $t_{TXD}$ | TXD | | — | — | 1 | $t_{cyc}$ | Figure 2.3.6 |
| Receive data setup time (clock synchronous) | | $t_{RXS}$ | RXD | | 50.0 | — | — | ns | |
| Receive data hold time (clock synchronous) | | $t_{RXH}$ | RXD | | 50.0 | — | — | ns | |

## 2.3 Operation Timing

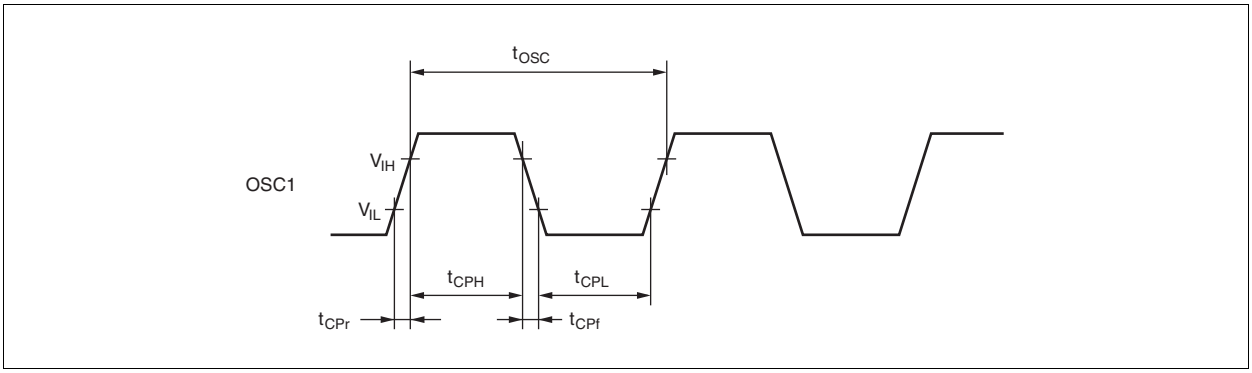



**Figure 2.3.1 System Clock Input Timing**

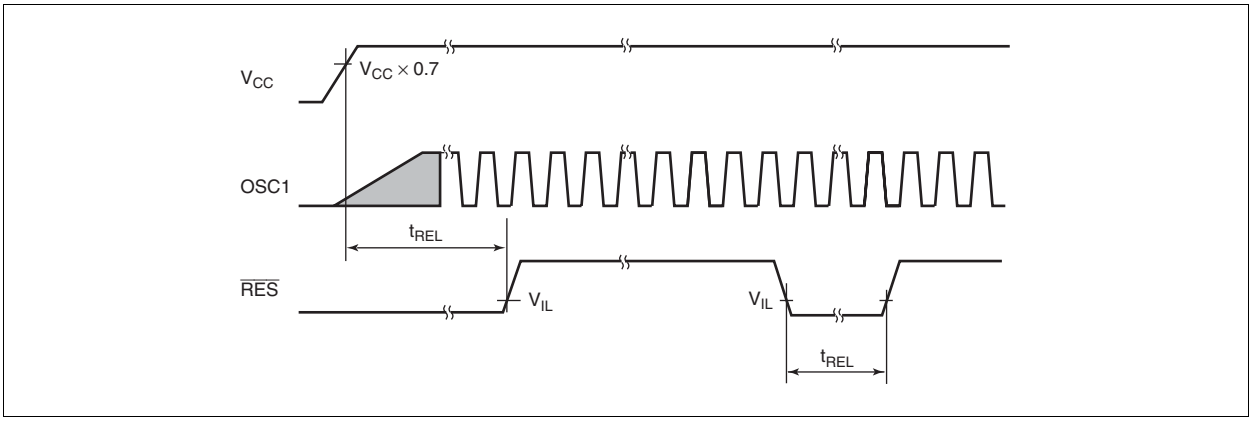



**Figure 2.3.2 $\overline{\text{RES}}$ Low Width Timing**

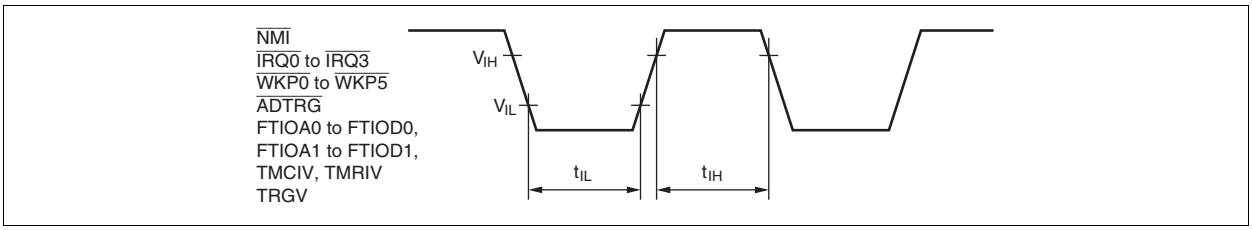



**Figure 2.3.3 Input Timing**

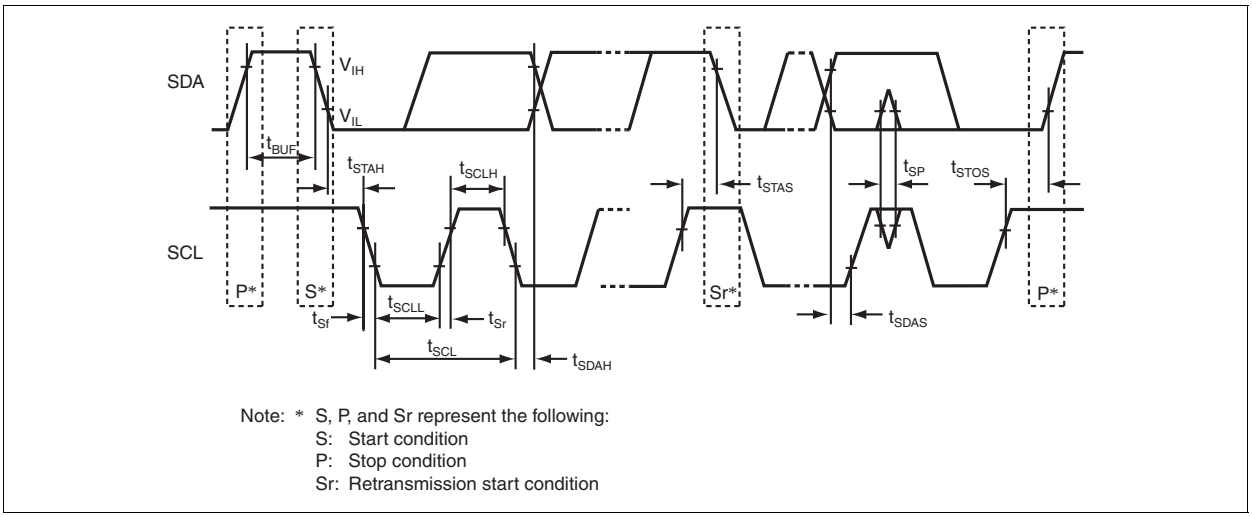



**Figure 2.3.4 $I^2C$ Bus Interface Input/Output Timing**

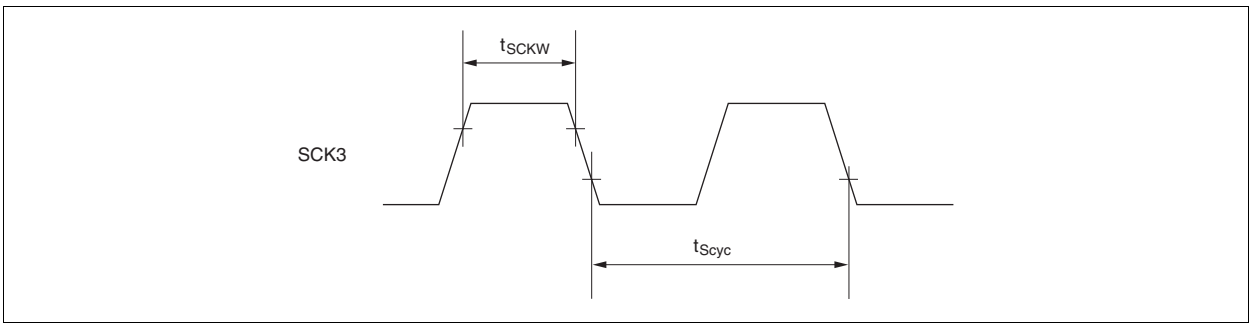
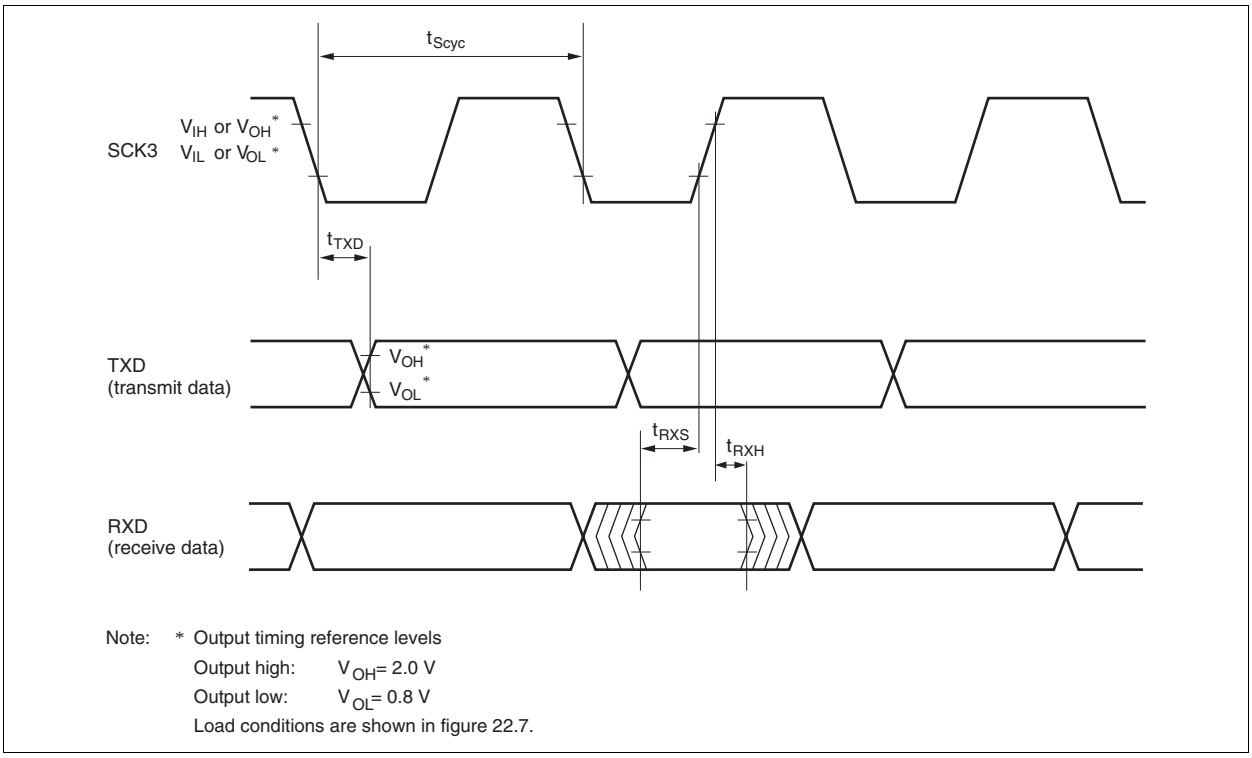



**Figure 2.3.5 SCK3 Input Clock Timing**




Note: * Output timing reference levels
Output high: $V_{OH}$= 2.0 V
Output low: $V_{OL}$= 0.8 V
Load conditions are shown in figure 22.7.

**Figure 2.3.6 SCI Input/Output Timing in Clock Synchronous Mode**

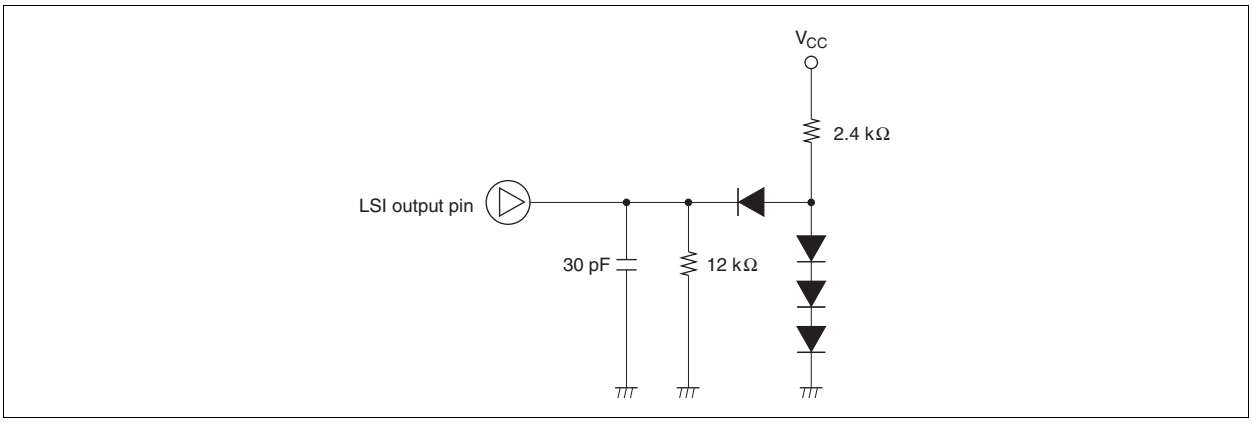



**Figure 2.3.7 Output Load Circuit**

## 2.4 A/D Converter Characteristics

### Table 2.4.1 A/D Converter Characteristics

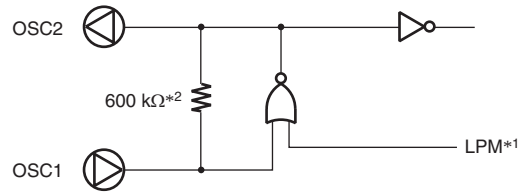
$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Analog power supply voltage | $AV_{CC}$ | $AV_{CC}$ | | 3.0 | $V_{CC}$ | 3.6 | V | *1 |
| Analog input voltage | $AV_{IN}$ | AN0 to AN7 | | $V_{SS}$ – 0.3 | — | $AV_{CC}$ + 0.3 | V | |
| Analog power supply current | $AI_{OPE}$ | $AV_{CC}$ | $AV_{CC}$ = 3.6 V<br>$f_{OSC}$ = 16 MHz | — | — | 2.0 | mA | |
| | $AI_{STOP1}$ | $AV_{CC}$ | | — | 50 | — | µA | *2<br>Reference value |
| | $AI_{STOP2}$ | $AV_{CC}$ | | — | — | 5.0 | µA | *3 |
| Analog input capacitance | $C_{AIN}$ | AN0 to AN7 | | — | — | 30.0 | pF | |
| Permissible signal source impedance | $R_{AIN}$ | AN0 to AN7 | | — | — | 5.0 | kΩ | |
| Resolution (data length) | | | | 10 | 10 | 10 | bit | |
| Conversion time (single mode) | | | $AV_{CC}$ = 3.0 to 3.6 V | 134 | — | — | $t_{cyc}$ | |
| Nonlinearity error | | | | — | — | ±7.5 | LSB | |
| Offset error | | | | — | — | ±7.5 | LSB | |
| Full-scale error | | | | — | — | ±7.5 | LSB | |
| Quantization error | | | | — | — | ±0.5 | LSB | |
| Absolute accuracy | | | | — | — | ±8.0 | LSB | |

Notes: 1. Set $AV_{CC}$ = $V_{CC}$ when the A/D converter is not used.
2. $AI_{STOP1}$ is the current in active and sleep modes while the A/D converter is idle.
3. $AI_{STOP2}$ is the current at reset and in standby, subactive, and subsleep modes while the A/D converter is idle.

## 2.5 External Oscillators

There are two methods to supply external clock pulses into this LSI: connecting a crystal or ceramic resonator, and an external clock. Oscillation pins OSC1 and OSC2 are common with general ports PC0 and PC1, respectively.




Notes: 1. LPM: Power-down mode (standby mode, subactive mode, or subsleep mode)
2. Values here are reference values.

**Figure 2.5.1 Block Diagram of External Clock Oscillator**

### 2.5.1 Connecting Crystal Resonator

Figure 2.5.2 shows an example of connecting a crystal resonator. An AT-cut parallel-resonance crystal resonator should be used. Figure 2.5.3 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 2.5.1 should be used.

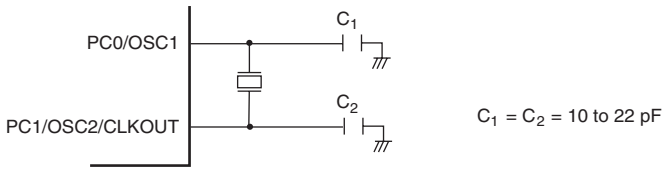



**Figure 2.5.2 Example of Connection to Crystal Resonator**

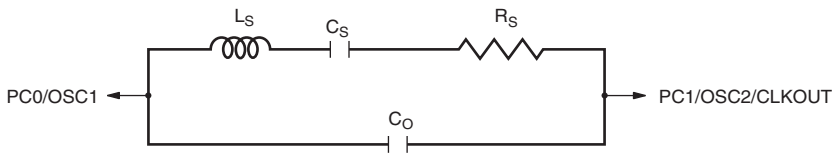



**Figure 2.5.3 Equivalent Circuit of Crystal Resonator**

**Table 2.5.1 Crystal Resonator Parameters**

| Frequency (MHz) | 4 | 8 | 10 | 16 | 20 |
|---|---|---|---|---|---|
| $R_S$ (Max.) | 120 Ω | 80 Ω | 60 Ω | 50 Ω | 40 Ω |
| $C_O$ (Max.) | | | 70 pF | | |

### (1) Connecting Ceramic Resonator

Figure 2.5.4 shows an example of connecting a ceramic resonator.

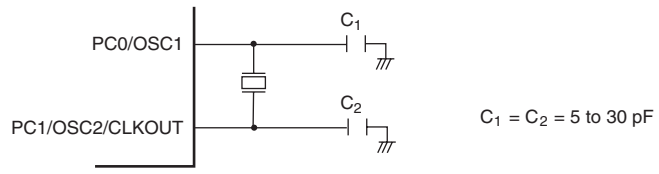



**Figure 2.5.4 Example of Connection to Ceramic Resonator**

### (2) Inputting External Clock

To use the external clock, input the external clock on pin OSC1. Figure 2.5.5 shows an example of connection. The duty cycle of the external clock signal must range from 45 to 55%.

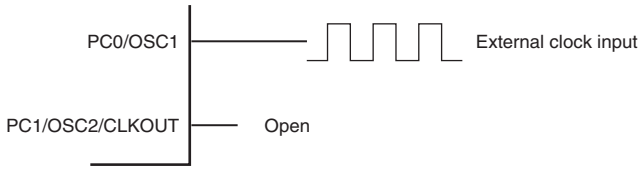



**Figure 2.5.5 Example of External Clock Input**

## 2.5.2 Subclock Oscillator

Figure 2.5.6 shows a block diagram of the subclock oscillator.

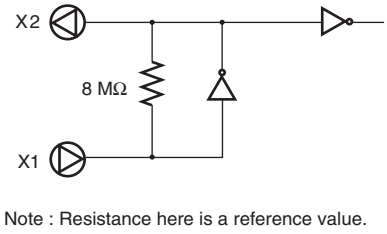



**Figure 2.5.6 Block Diagram of Subclock Oscillator**

### (1) Connecting 32.768-kHz Crystal Resonator

Clock pulses can be supplied to the subclock divider by connecting a 32.768-kHz crystal resonator, as shown in figure 2.5.7. Figure 2.5.8 shows the equivalent circuit of the 32.768-kHz crystal resonator.

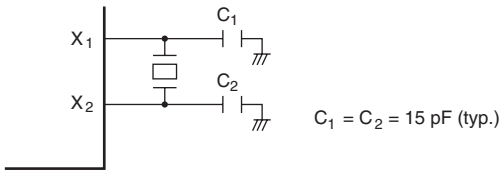
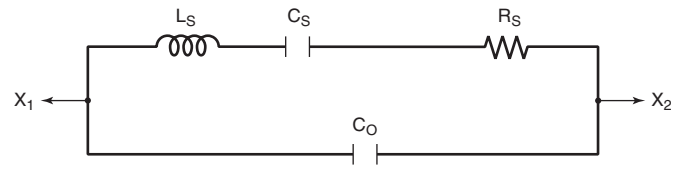



**Figure 2.5.7 Typical Connection to 32.768-kHz Crystal Resonator**




$C_O$ = 1.5 pF (typ.)
$R_S$ = 14 kΩ (typ.)
$f_W$ = 32.768 kHz

Note: Values here are reference values.

**Figure 2.5.8 Equivalent Circuit of 32.768-kHz Crystal Resonator**

### (2) Pin Connection when Not Using Subclock

When the subclock is not used, connect pin X1 to VCL or VSS and leave pin X2 open, as shown in figure 2.5.9.

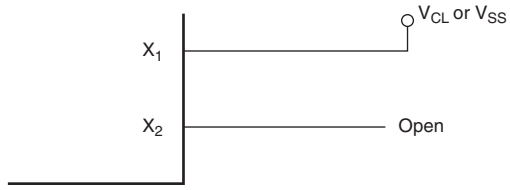



**Figure 2.5.9 Pin Connection when not Using Subclock**

### 2.5.3 Usage Notes

#### (1) Note on Resonators

Resonator characteristics are closely related to board design and should be carefully evaluated by the user, referring to the examples shown in this section. Resonator circuit parameters will differ depending on the resonator element, stray capacitance of the PCB, and other factors. Suitable values should be determined in consultation with the resonator element manufacturer. Design the circuit so that the resonator element never receives voltages exceeding its maximum rating.

#### (2) Notes on Board Design

When using a crystal resonator (ceramic resonator), place the resonator and its load capacitors as close as possible to pins OSC1 and OSC2. Other signal lines should be routed away from the oscillator circuit to prevent induction from interfering with correct oscillation (see figure 2.5.10).

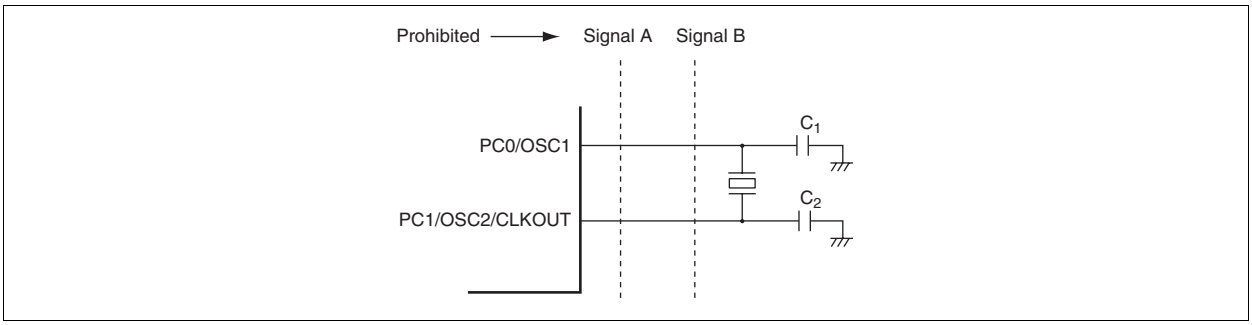



**Figure 2.5.10 Example of Incorrect Board Design**

## 2.6 Watchdog Timer Characteristics

**Table 2.6.1 Watchdog Timer Characteristics**

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| On-chip oscillator overflow time | $t_{OVF}$ | | | 0.2 | 0.4 | — | s | * |

Note: * Time until an internal reset is generated after the counter counts from 0 to 255 when the on-chip oscillator is selected

## 2.7 ROM Characteristics

### 2.7.1 Flash Memory Characteristics

**Table 2.7.1 Flash Memory Characteristics**

$V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| Item | | Symbol | Test Condition | Values Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Programming time (per 128 bytes)*1*2*4 | | $t_P$ | | — | 7.0 | 10.0 | ms |
| Erase time (per block) *1*3*6 | | $t_E$ | | — | 10.0 | 20.0 | ms |
| Reprogramming count | | $N_{WEC}$ | | 1000 | 10000 | — | Times |
| Programming | Wait time after setting SWE bit*1 | x | | 1 | — | — | µs |
| | Wait time after setting PSU bit*1 | y | | 50 | — | — | µs |
| | Wait time after setting P bit *1*4 | z1 | 1 ≤ n ≤ 6 | 28 | 30 | 32 | µs |
| | | z2 | 7 ≤ n ≤ 1000 | 198 | 200 | 202 | µs |
| | | z3 | Additional-programming | 8 | 10 | 12 | µs |
| | Wait time after clearing P bit*1 | α | | 5 | — | — | µs |
| | Wait time after clearing PSU bit*1 | β | | 5 | — | — | µs |
| | Wait time after setting PV bit*1 | γ | | 4 | — | — | µs |
| | Wait time after dummy write*1 | ε | | 2 | — | — | µs |
| | Wait time after clearing PV bit*1 | η | | 2 | — | — | µs |
| | Wait time after clearing SWE bit*1 | θ | | 100 | — | — | µs |
| | Maximum programming count *1*4*5 | N | | — | — | 1000 | Times |

**Data hold time**

| Reprogramming count | Memory address | Data hold time*8 |
|---|---|---|
| 1000 Times | H'000000 ～ H'01FFFF | 10 year |
| 10000 Times | H'000000 ～ H'000FFF | 3 month |

## ■ Electrical Characteristics

| Item | | Symbol | Test Condition | Values Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Erasing | Wait time after setting SWE bit*[1] | x | | 1 | — | — | µs |
| | Wait time after setting ESU bit*[1] | y | | 100 | — | — | µs |
| | Wait time after setting E bit*[1]*[6] | z | | 10 | — | 100 | ms |
| | Wait time after clearing E bit*[1] | α | | 10 | — | — | µs |
| | Wait time after clearing ESU bit*[1] | β | | 10 | — | — | µs |
| | Wait time after setting EV bit*[1] | γ | | 20 | — | — | µs |
| | Wait time after dummy write*[1] | ε | | 2 | — | — | µs |
| | Wait time after clearing EV bit*[1] | η | | 4 | — | — | µs |
| | Wait time after clearing SWE bit*[1] | θ | | 100 | — | — | µs |
| | Maximum erase count *[1]*[6]*[7] | N | | — | — | 120 | Times |

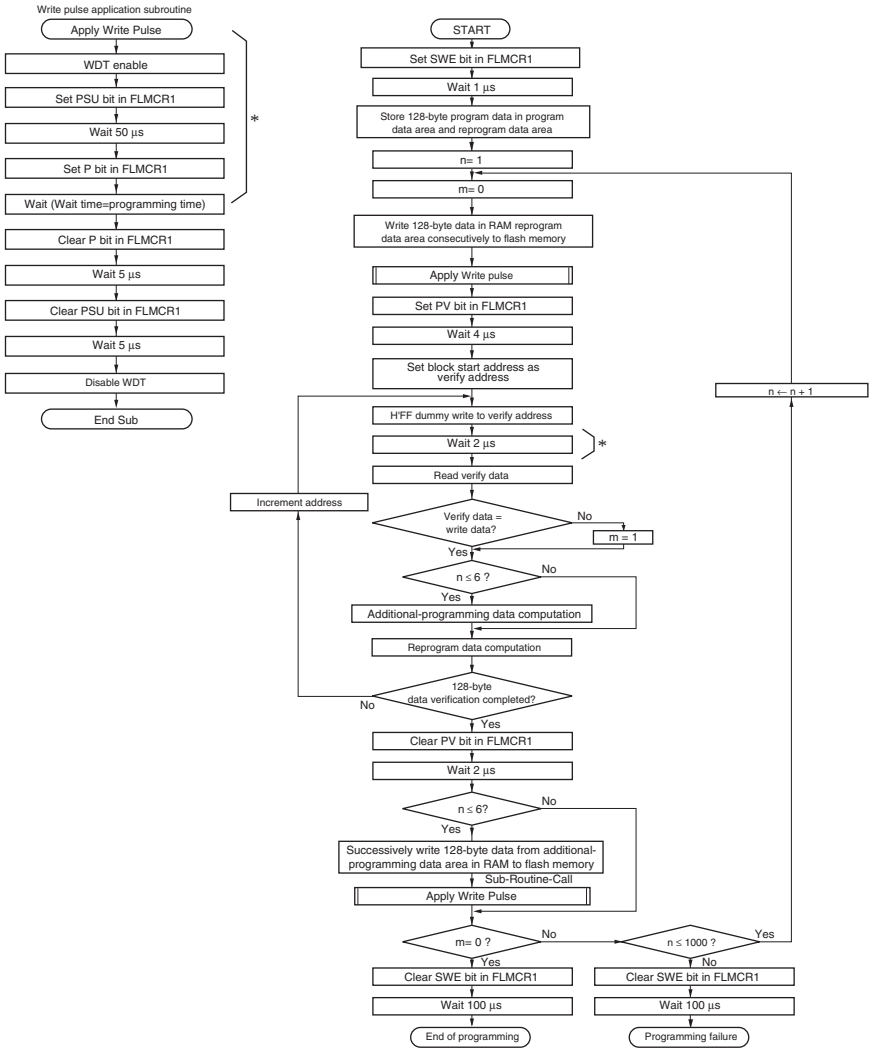
Notes:
1. Make the time settings in accordance with the program/erase algorithms.
2. The programming time for 128 bytes. (Indicates the total time for which the P bit in flash memory control register 1 (FLMCR1) is set. The program-verify time is not included.)
3. The time required to erase one block. (Indicates the time for which the E bit in flash memory control register 1 (FLMCR1) is set. The erase-verify time is not included.)
4. Programming time maximum value ($t_P$(max.)) = wait time after P bit setting (z) × maximum programming count (N)
5. Set the maximum programming count (N) according to the actual set values of z1, z2, and z3 so that it does not exceed the programming time maximum value ($t_P$(max.)). The wait time after setting P bit (z1, z2) should be changed as follows according to the value of the programming count (n).

   Programming count (n)

   $1 \leq n \leq 6$ z1 = 30 µs

   $7 \leq n \leq 1000$ z2 = 200 µs
6. Erase time maximum value ($t_E$(max.)) = wait time after E bit setting (z) × maximum erase count (N)
7. Set the maximum erase count (N) according to the actual set value of (z) so that it does not exceed the erase time maximum value ($t_E$(max.)).
8. The data hold time includes time that the power supply os off or the clock is not supplied.

## 2.7.2 Flash Memory Programming/Erasing




Note: *The RTS instruction must not be used during the following 1. and 2. periods.
1. A period between 128-byte data programming to flash memory and the P bit clearing
2. A period between dummy writing of H'FF to a verify address and verify data reading

**Figure 2.7.1 Program/Program-Verify Flowchart**

**Table 2.7.2 Reprogram Data Computation Table**

| Program Data | Verify Data | Reprogram Data | Comments |
|---|---|---|---|
| 0 | 0 | 1 | Programming completed |
| 0 | 1 | 0 | Reprogram bit |
| 1 | 0 | 1 | — |
| 1 | 1 | 1 | Remains in erased state |

**Table 2.7.3 Additional-Program Data Computation Table**

| Reprogram Data | Verify Data | Additional-Program Data | Comments |
|---|---|---|---|
| 0 | 0 | 0 | Additional-program bit |
| 0 | 1 | 1 | No additional programming |
| 1 | 0 | 1 | No additional programming |
| 1 | 1 | 1 | No additional programming |

**Table 2.7.4 Programming Time**

| n (Number of Writes) | Programming Time | In Additional Programming | Comments |
|---|---|---|---|
| 1 to 6 | 30 | 10 | |
| 7 to 1,000 | 200 | — | |

Note: Time shown in µs.

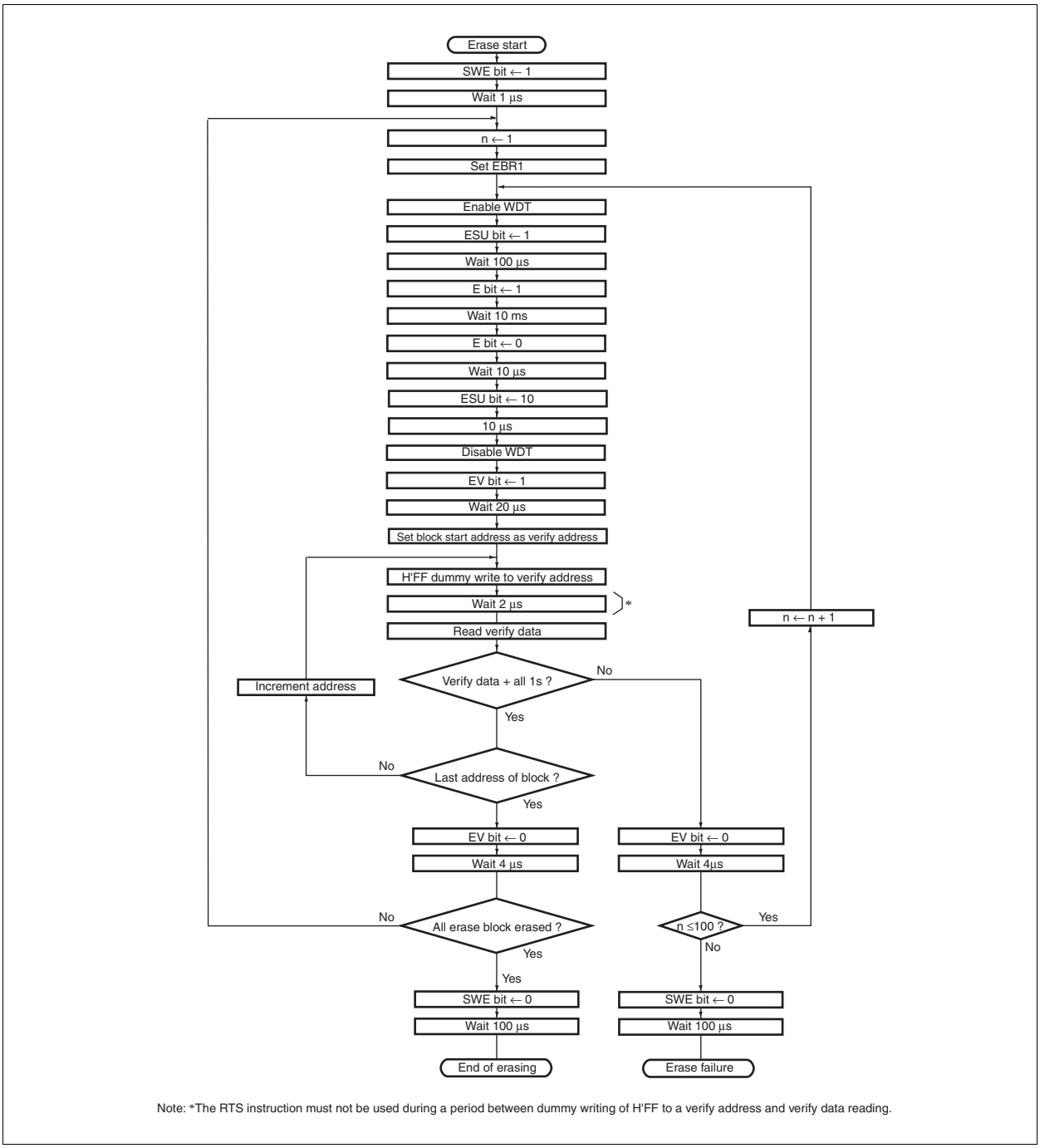



**Figure 2.7.2 Erase/Erase-Verify Flowchart**

## 2.9 Power-Supply-Voltage Detection Circuit Characteristics

### 2.9.1 Power-Supply-Voltage Detection Circuit Characteristics

**Table 2.9.1 Power-Supply-Voltage Detection Circuit Characteristics**

$V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| | | Values | | | |
|---|---|---|---|---|---|
| **Item** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Power-supply falling detection voltage | Vint (D) | 2.8 | 2.9 | 3.05 | V |
| Power-supply rising detection voltage | Vint (U) | 2.9 | 3.0 | 3.15 | V |
| Reset detection voltage 1* | Vreset1 | — | 2.3 | 2.6 | V |
| Lower-limit voltage of LVDR operation | $V_{LVDRmin}$ | 1.0 | — | — | V |

Note: * This voltage should be used when the falling and rising voltage detection function is used.

### 2.9.2 LVDI External Input Voltage Detection Circuit Characteristics

**Table 2.9.2 LVDI External Input Voltage Detection Circuit Characteristics**

Vcc = 3.0 to 3.6 V, AVcc = 3.0 to 3.6 V, $V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C

| | | Test | Values | | | |
|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| ExtD/ExtU input detection voltage | Vexd | | 0.95 | 1.15 | 1.35 | V |
| ExtD/ExtU input voltage range | VextD/VextU | VextD > VextU | –0.3 | — | Lower voltage of $AV_{cc}$ + 0.3 or $V_{cc}$ + 0.3 | V |

### 2.9.3 Power-On Reset Circuit Characteristics

**Table 2.9.3 Power-On Reset Circuit Characteristics**

$V_{SS}$ = 0.0 V, $T_a$ = –20 to +75°C, unless otherwise indicated.

| | | Test | Values | | | |
|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **Condition** | **Min.** | **Typ.** | **Max** | **Unit** |
| Pull-up resistance of $\overline{RES}$ pin | $R_{RES}$ | | 100 | 150 | — | kΩ |
| Power-on reset start voltage* | $V_{por}$ | | — | — | 100 | mV |

Note: * The power-supply voltage (Vcc) must fall below Vpor = 100 mV and then rise after charge of the $\overline{RES}$ pin is removed completely. In order to remove charge of the $\overline{RES}$ pin, it is recommended that the diode be placed in the Vcc side. If the power-supply voltage (Vcc) rises from the point over 100 mV, a power-on reset may not occur.

## ■ Pin Assignments

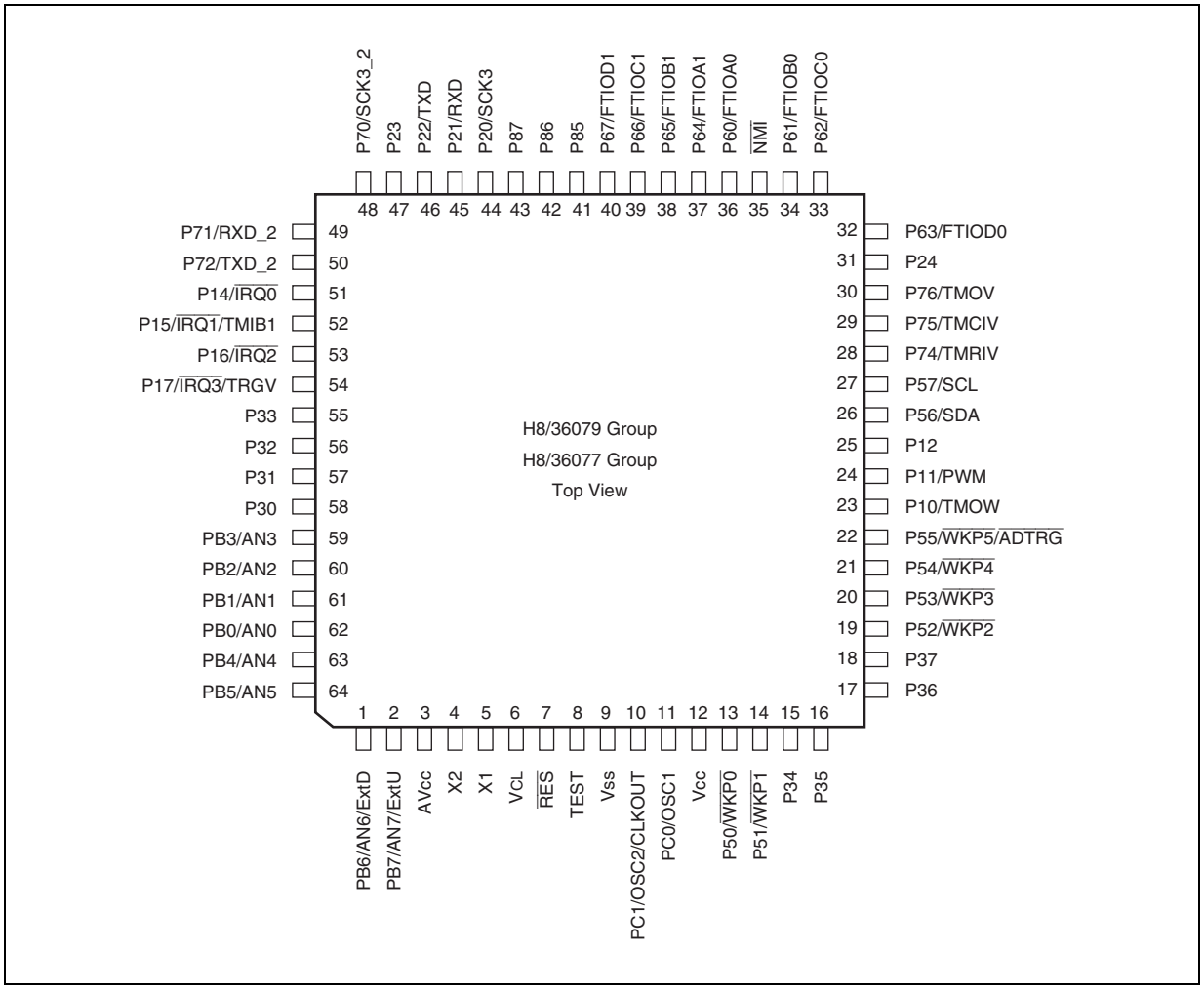
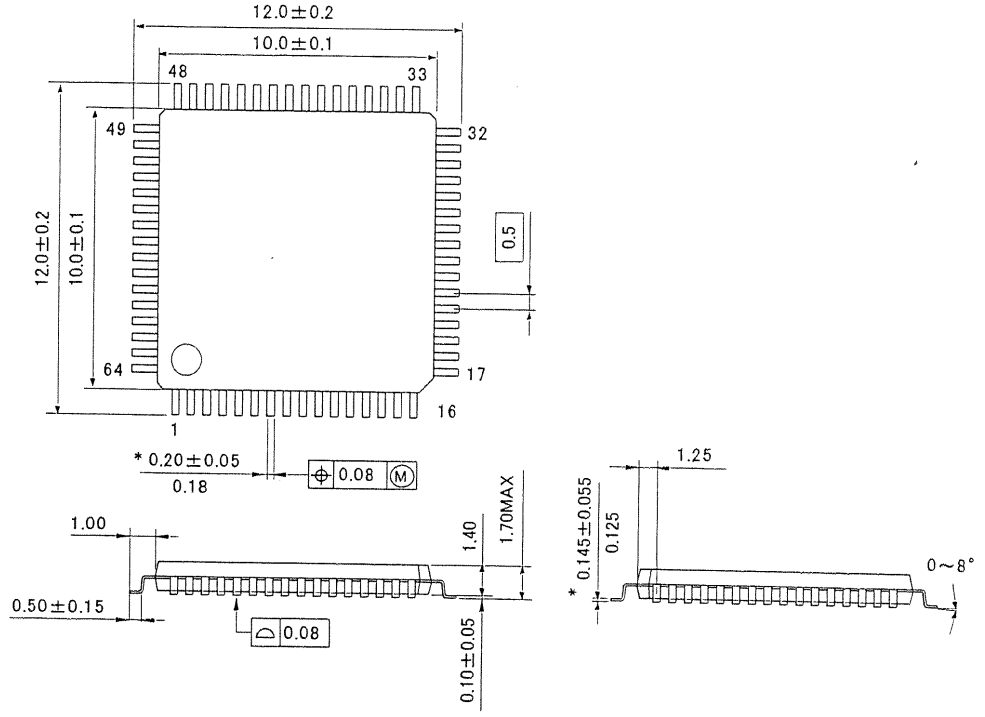



**Figure 1 Pin Assignments (FP-64K, FP-64A)**




*
めっき厚含み寸法

素材寸法

*
Dimension including the plating thickness

Base material dimension

(単位 unit:mm)

| | |
|---|---|
| パッケージコード (Package CODE) | FP-64K,FP-64KV |
| JEITAコード (JEITA CODE) | EDR-7311準拠 |
| JEDECコード (JEDEC CODE) | ——— |
| 重量(g) (mass) | 0.3g |

REVISIONS

| SYM. | N. | PL | DATE | REVD. | CHKD. | APPD. |
|---|---|---|---|---|---|---|

| | |
|---|---|
| MM2 | 1 |
| MM1 | 1 |
| MQ | 1 |
| MM3 | 1 |
| MA | 1 |
| PROVI. SECT. | copy |

D.CHKD

| Gr. | A | B | C | D |
|---|---|---|---|---|
| PKG CODE | FP-64K/FP-64KV | | | |

REMARKS

DWN. M.TSUGANE 2004.03.17

CHKD. M.YAMADA 2004.03.18

APPD. F.Ito 2004.03.18

PROJECTION

SCALE NTS

2004.03.18 RECD.

TITLE

# FTR-OUTLN

## 顧客向け外形寸法図

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | AN | 528 | M | PKGFTR 1190 |

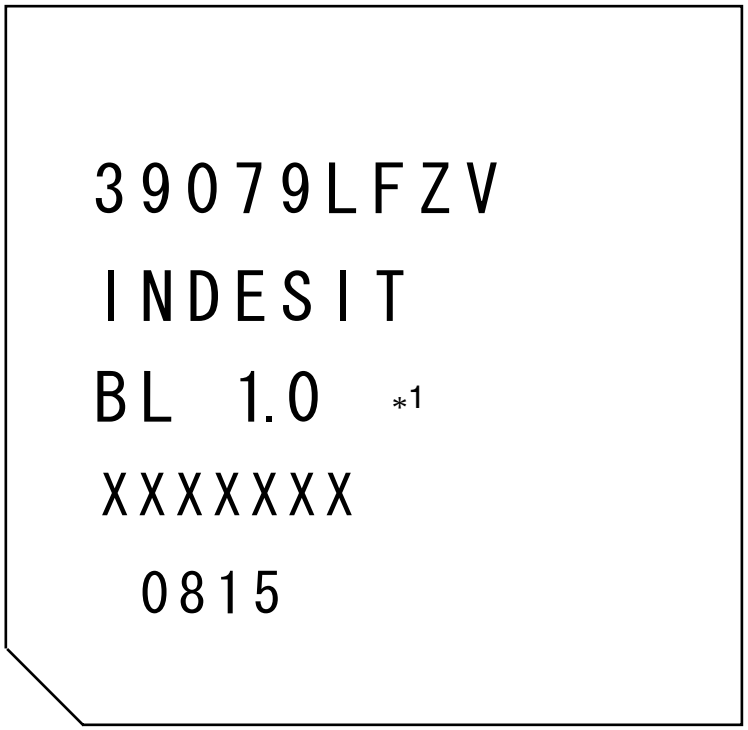
Renesas Technology Corp.

343 4Q01699

SH. 1 / E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

## ■ Mark Specification Example




| | |
|---|---|
| 39079LFZV | : Type |
| INDESIT | : Customer's Parts No.1 |
| BL 1.0 | : Customer's Parts No.2 |
| 0815 | : Production Lot Code (EIA Code)<br>(A number of four figures) |
| XXXXXXX | : Trace Code |

Note: 1. In case of reprogramming chips that are already marked with Customer's Parts No.2 (boot version), a dot will be added right side boot version.

**Figure 1 Mark Specification Example**

## ■ Functional Block Diagram

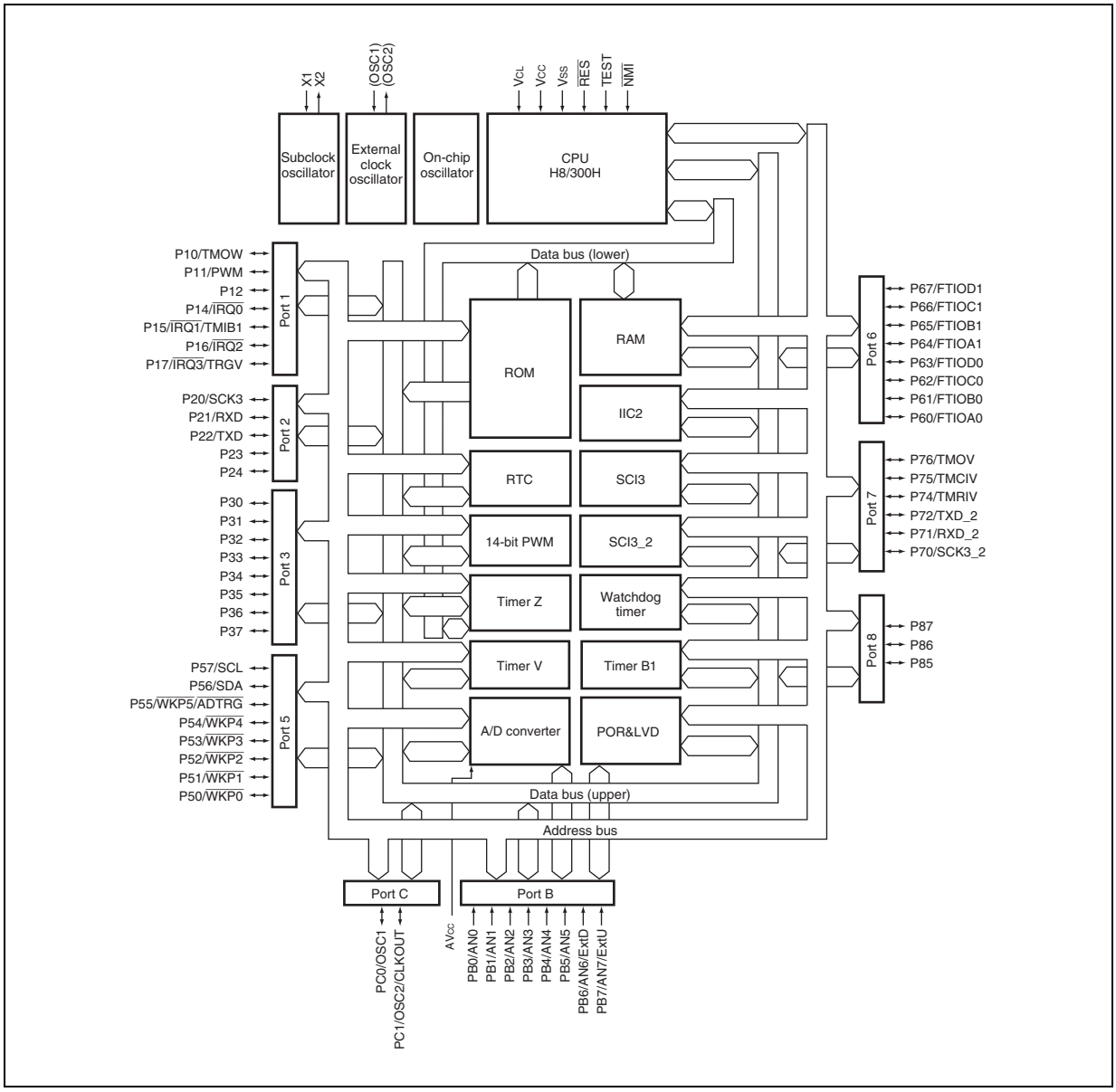



**Figure 1 Functional Block Diagram**

## ■ Others

**(1) Problems with the delivery**

If any problems occur regarding the quality of supplied product etc, they will be solved by negotiations between your company and Renesas Technology Corp.

**(2) Problems and revision to the specifications**

If any problems occur, or if any revision to the specifications is necessary, they will be solved by negotiations between your company and Renesas Technology Corp.

**(3) Production lot number**

EIA code

Indicate it with 4 digit.

Indicate it with under 2 digit of the year, and week of the year.

For example, number of 0508 is lot manufactured at the 08th week of 2005 years.

**(4) Packing and indication**

Semiconductor products applicable to this specification are packed in inner package to keep out foreign matters. This package includes the manufacture's abbreviations, lot number and product's name on it.

## 1.1 Address Space and Memory Map

Figure 1.1 shows the memory map.

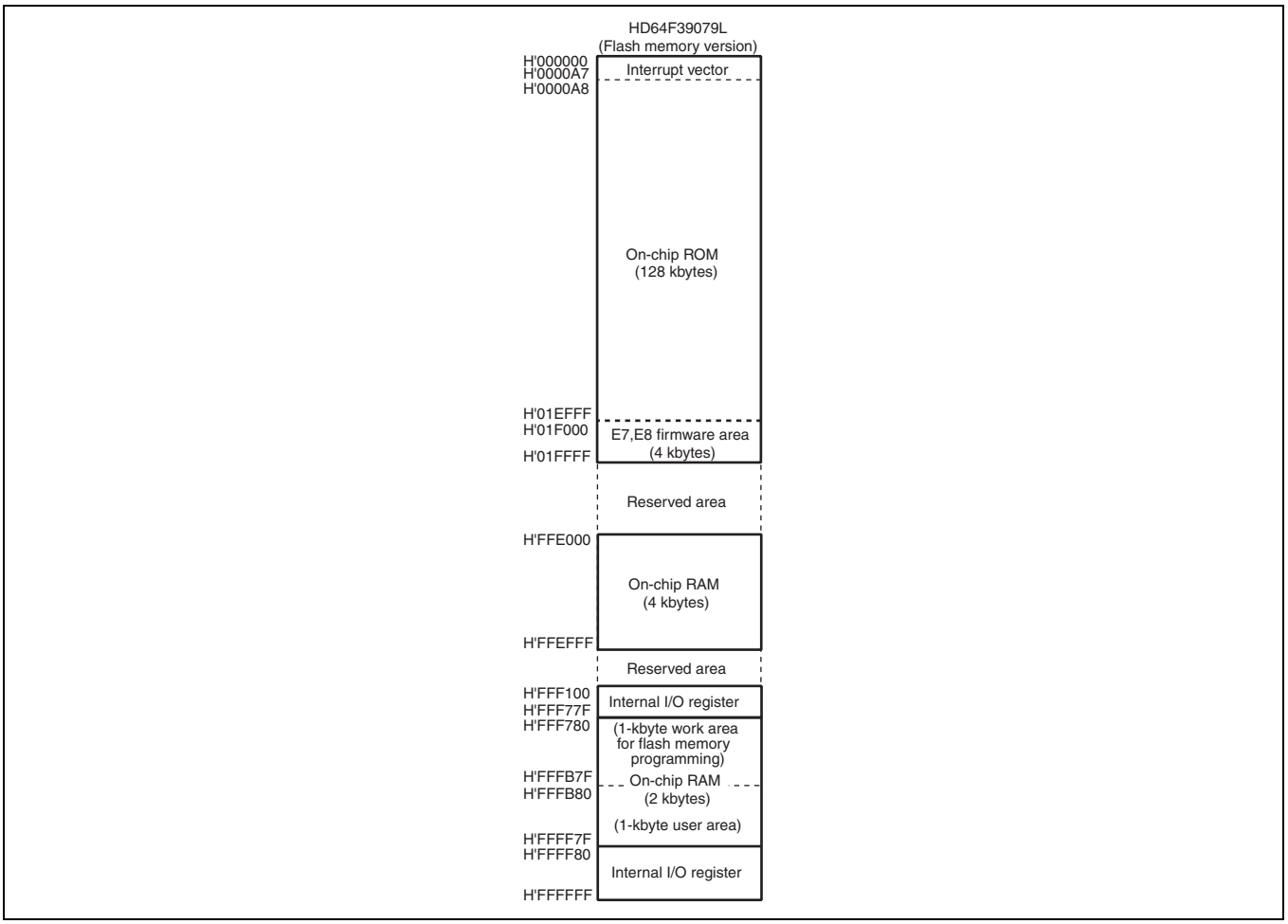



**Figure 1.1 Memory Map**

## 1.2 Block Configuration

Figure 1.2 shows the block configuration of flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The 128-kbyte flash memory is divided into 1 kbyte × 4 blocks, 28 kbytes × 1 block and 32 kbytes × 3 blocks. Erasing is performed in these units.

Programming is performed in 128-byte units starting from an address with lower eight bits H'00 or H'80.

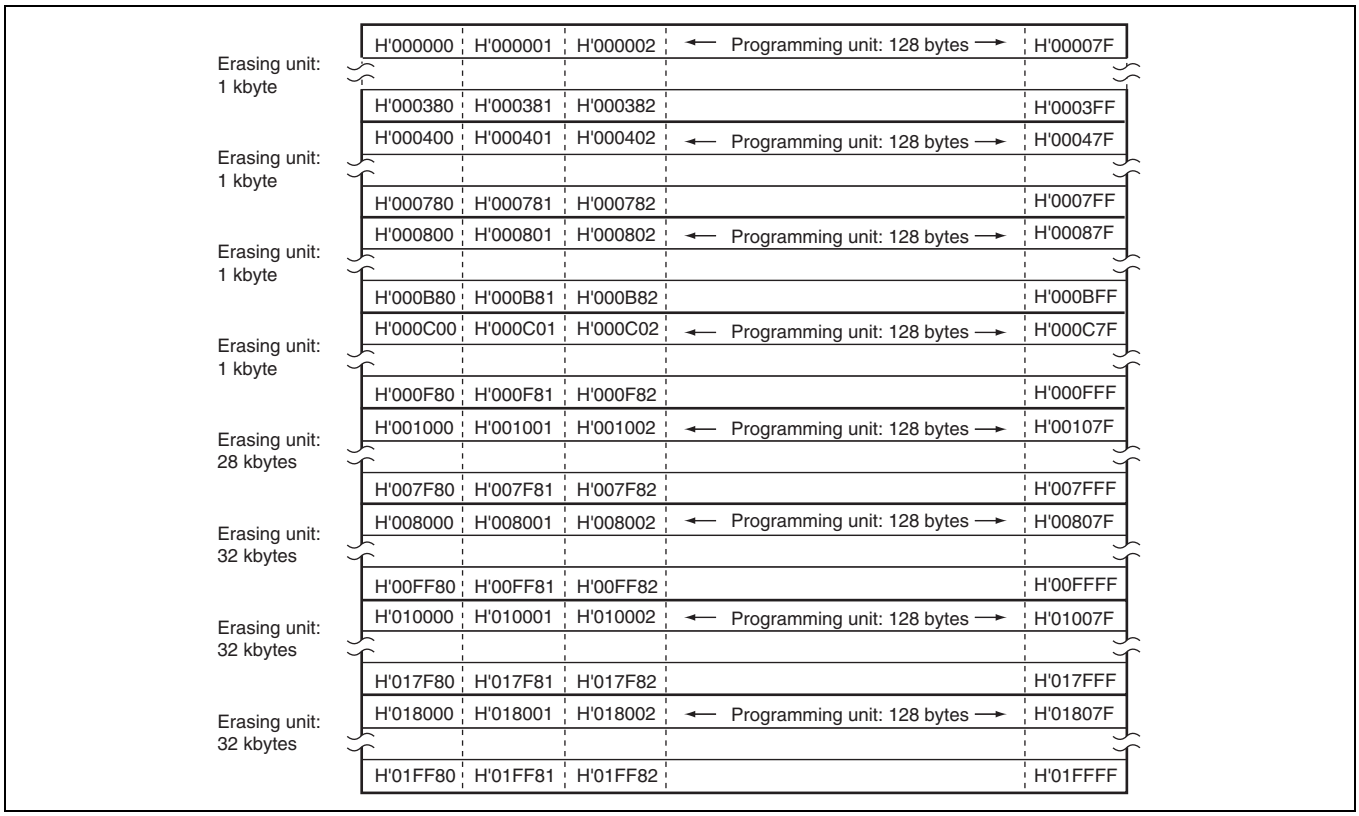



**Figure 1.2 Block Configuration of Flash Memory**

### 1.2.1 Erase Block Register 1 (EBR1)

EBR1 specifies the flash memory erase area block. EBR1 is initialized to H'00 when the SWE bit in FLMCR1 is 0. Do not set more than one bit at a time, as this will cause all the bits in EBR1 to be automatically cleared to 0.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | EB7 | 0 | R/W | When this bit is set to 1, 32 kbytes of H'018000 to H'01FFFF will be erased. |
| 6 | EB6 | 0 | R/W | When this bit is set to 1, 32 kbytes of H'010000 to H'017FFF will be erased. |
| 5 | EB5 | 0 | R/W | When this bit is set to 1, 32 kbytes of H'008000 to H'00FFFF will be erased. |
| 4 | EB4 | 0 | R/W | When this bit is set to 1, 28 kbytes of H'001000 to H'007FFF will be erased. |
| 3 | EB3 | 0/1 | R/W | When this bit is set to 1, 1 kbyte of H'000C00 to H'000FFF will be erased. |
| 2 | EB2 | 0/1 | R/W | When this bit is set to 1, 1 kbyte of H'000800 to H'000BFF will be erased. |
| 1 | EB1 | 0/1 | R/W | When this bit is set to 1, 1 kbyte of H'000400 to H'0007FF will be erased. |
| 0 | EB0 | 0/1 | R/W | When this bit is set to 1, 1 kbyte of H'000000 to H'0003FF will be erased. |

APPD. CHKD. REVD. DATE

REVISIONS
P.1 , W#PKGFTR, S#4179

SYM. N.PL
1
1

# リフロー法推奨条件 (小型パッケージ)
# Recommended Reflow Soldering Conditions

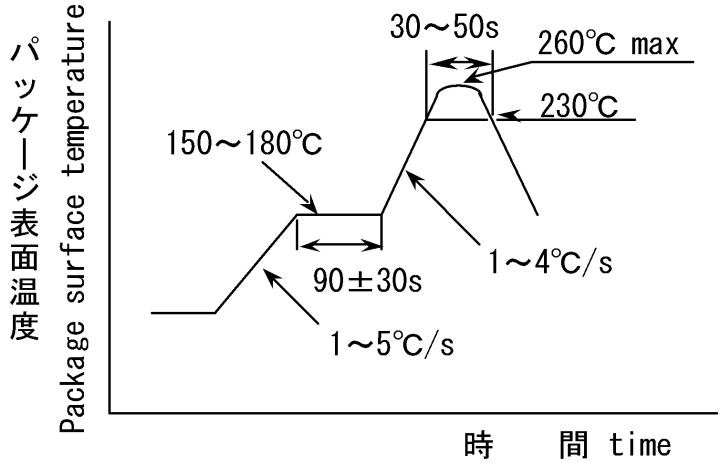
防湿包装開封後は再吸湿を避けるため、防湿包装開封後の保管条件以内にリフロー実装して下さい。
またそれ以上経過した場合はベーク条件の示すベークを行って下さい。

After opening the moisture proof packing, parts must be installed at the condition , the keeping condition after opening dry packing, against re- moisturized.
If the device has been stored longer than the specified time after opening packing, parts must be baked at the condition of the baking condition.

(1) 部品耐熱性 Parts capacity of heat proof

エアリフロー、N2リフロー :パッケージ表面温度 =260℃ max,
230℃以上の時間 =30～50秒

Air reflowing , N2 reflowing :Package surface temperature =260℃ max,
Over 230℃ time=30～50s




<The condition of Air reflowing, N2 reflowing>
<小型パッケージのエアリフロー、N2リフロー推奨条件>

(2) リフロー回数 : 3回 (防湿包装開封後の保管条件以内)
Reflowing times : 3times (While the keeping condition after opening dry packing)

| | |
|---|---|
| MHSM | 1 |
| Mタカサキ | D |
| MチョウL | D |
| MW | D |
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MA | 1 |
| MQ | 1 |
| PROVI. SECT. | copy |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| REMARKS | Pb－Free | | | | | | | | | |
| DWN. | | | PROJECTION | TITLE | | | | | | DWG.STAMP |
| CHKD. | | | SCALE NTS | FTR-REFL-COND 顧客向けリフロー条件 | | | | | | |
| APPD. | | | REGD. | SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. | |
| | | | | E | 5Z | B2 | 528 | E | PKGFTR 4179 | |
| | | | | Renesas Technology Corp. | | | | | | SH. |
| | | | | 343 4Q01178 | | | | | | 1 |
| | | | | | | | | | | E |

| D | C | B | A | Gr. |
|---|---|---|---|---|
| | | | GENERAL | 区分(GROUP) |

D.CHKD

| | |
|---|---|
| APPD. | R.KIMOTO |
| CHKD. | R.KIMOTO |
| REVD. | M.YAMADA |
| DATE | 2005.06.27 |
| REVISIONS | P.1 , W#PKGFTR, S#4502 |
| SYM.N.PL | 1 / 3 |

△3

# ベークについて(厚型)
# Baking Process (Thick type)

## 実装前のベーク(乾燥)処理について
About the baking process (Moisture removal process) before soldering

1) ベーク処理を必要とする場合　Baking is necessary in the following cases.

A) 防湿包装開封時に、インジケーターカードの30%スポットが
ピンクに変色している場合
When the 30% spot on the humidity indicator card turns pink, when the moisture-proof bag is opened.

B) 防湿包装開封後、規定の保管条件を超過した場合
When the storage conditions exceed the stipulation after the moisture-proof bag is opened.

2) 推奨ベーク条件　Recommended baking condition

| | ベーク温度<br>Baking Temperature | ベーク時間<br>Baking Time | 繰り返しベーク<br>Repetitve Baking |
|---|---|---|---|
| 厚型<br>(Thick type) | 125℃±5℃ | 16 to 24 hours | 累計で96時間以内<br>Total of 96 hours or less |

ベークの際は、耐熱性のあるトレイなどで処理してください。
なお、耐熱トレイには、「HEAT PROOF」または耐熱温度の表示がありますので、
処理の前にご確認ください。
Be sure to use heatproof trays, etc., when performing the baking process.
Heatproof trays are marked with the words "HEAT PROOF"
or carry an indication of their maximum temperature rating.
Confirm these markings before performing the baking process.

| | |
|---|---|
| MHSD | D |
| MチョウL | D |
| MW | D |
| MQ | 1 |
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MHSM | 1 |
| MA | 1 |
| PROVI. SECT. | copy |

D.CHKD

| | | | | |
|---|---|---|---|---|
| D | C | B | A GENERAL | Gr. 区分(GROUP) |

REMARKS 厚型

| | | | |
|---|---|---|---|
| DWN. | M.YAMADA | 2005.06.24 | PROJECTION |
| CHKD. | R.KIMOTO | 2005.06.24 | SCALE NTS |
| APPD. | R.KIMOTO | 2005.06.24 | |

2005.6.27 REGD.

Renesas Technology Corp.

TITLE
FTR-BAKE-COND
顧客向けベーク条件

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | AN | 528 | E | PKGFTR 4502 |

SH. 1 / E

343 4Q00874

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

REVISIONS

P.1 , W#PKGFTR, S#4782

SYM. N.PL 1 2

△2

# 防湿包装開封前の保管について
# Storage Before the Dry Pack is Opened

防湿包装開封前の保管期限は5～35℃、85%RH以下で2年です。
The time limit to leave the packages in a dry pack is 2 years, provided that the temperature is between 5 to 35℃ and the relative humidity is 85% or less.

| | |
|---|---|
| MHSD | D |
| MチョウL | D |
| MW | D |
| MQ | 1 |
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MHSM | 1 |
| MA | 1 |
| PROVI. SECT. | co py |

D.CHKD

| D | C | B | A | Gr. |
|---|---|---|---|---|
| | | | GENERAL | 区分(GROUP) |

REMARKS 防湿包装開封前

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-STRG-COND

顧客向け保管条件

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | AN | 528 | E | PKGFTR 4782 |

Renesas Technology Corp.

343 4Q00876

SH. 1 E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

REVISIONS

P.1 , W#PKGFTR, S#4180

SYM. N.PL 1 1

△1

# 防湿包装開封後の保管及び取り扱いについて
## Storage and Handling After the Moisture-proof Bag is Opened

防湿包装開封後は吸湿を避けるため、下記条件にて保管してください。
Parts must be kept as below after opening dry packing against re-moisturized.

| 項目 | 条件 | 備　考 |
|---|---|---|
| 温度<br>Temperature | 5℃～30℃ | |
| 湿度<br>Humidity | 60%RH以下<br>60% RH or less | |
| 時間＊<br>Time | 168時間以内<br>168 hours or less | ＊開封後～最終リフローはんだ付け完了までの時間<br>This refers to the total time between opening the moisture-proof bag and completing the final reflow soldering process. |

| | |
|---|---|
| MチョウL | D |
| MW | D |
| MQ | 1 |
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MHSM | 1 |
| MA | 1 |
| PROVI. SECT. | co py |

D.CHKD

D C B A GENERAL Gr. 区分(GROUP)

REMARKS 防湿包装開封後

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-STRG-COND

顧客向け保管条件

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | AN | 528 | E | PKGFTR 4180 |

Renesas Technology Corp.

343 4Q00877

SH. 1 E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

REVISIONS

| SYM. | N.PL | |
|---|---|---|
| 1 | | P.1 , W#PKGFTR, S#4179 |
| 2 | | |

# 2 鉛フリーめっき製品における実装上の注意点

Notes and Cautions in Reflow Soldering the Devices with the Lead-free Plated Terminals

鉛フリーめっき製品を実装する場合、リフロー温度プロファイル設定にあたっては、
以下の項目に留意して、ピーク温度を設定願います。
The reflow soldering temperature profile, especially the peak temperature, for the devices with the lead-free plated terminals should be set after taking the following into consideration .

（1）製品の表面温度が耐熱温度以下になっていること。
（2）リード部温度が実装用はんだの融点以上になっていること。
(1)The surface temperature of the devices to be mounted must be less than the thermal resistant temperature of those devices.
(2)The temperature at the terminals must be higher than the solder melting point.

特にSn-Biめっき製品を実装する場合、めっき膜の融点が220～230℃となっているため、
230℃以上での実装が必要です。
It is necessary that the peak temperature for the devices with the Sn-Bi plated terminals should be 230℃ and above (higher than the melting point of the plating solder, which is 220 to 230℃ for Sn-Bi solder).

| | |
|---|---|
| MチョウL | D |
| MW | D |
| MQ | 1 |
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MHSM | 1 |
| MA | 1 |
| PROVI. SECT. | co py |

D.CHKD

| REMARKS | Sn-Biめっき Sn-Bi plating |
|---|---|

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-REFL-NOTE

顧客向け実装注意点

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | AN | 528 | E | PKGFTR 4179 |

Renesas Technology Corp.

343 4Q01292

SH. 1 E

D C B A GENERAL Gr. 区分(Group)

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

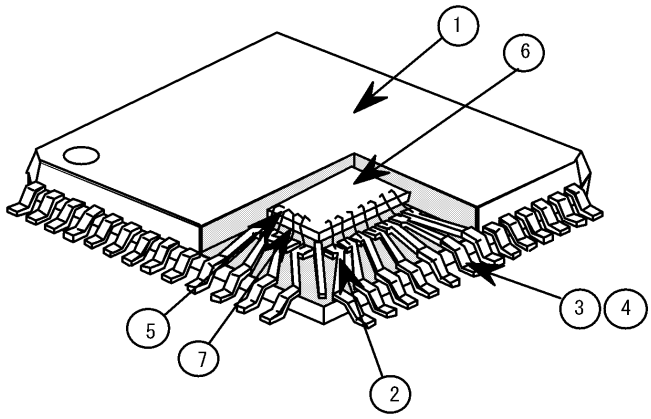
REVISIONS

P.1 , W#PKGFTR, S#4182

SYM.N.PL 1 1

1

## QFP内部構造図 (QFP Internal structure)




| 番号 (No.) | 部分 (Parts) | 材質 (Matelial) |
|---|---|---|
| ① | 封止樹脂 (Molding compound) | エポキシ樹脂 (Epoxy) 難燃性レベル (UL-Level) UL-94 V0 |
| ② | インナーリード処理 (Inner lead finish) | 部分銀めっき (Silver spot plating) |
| ③ | アウターリード処理 (Outer lead finish) | Sn-Biめっき (Sn-Bi plated) Sn:Tin Bi:Bismuth |
| ④ | リード (Lead) | 銅合金 (Copper Alloy) |
| ⑤ | ボンディングワイヤ (Bonding wire) | 金 (Gold) |
| ⑥ | チップ (Die) | シリコン (Silicon) |
| ⑦ | ダイボンディング材 (Die bonding) | 樹脂ペースト (Organic adhesive) |

| | |
|---|---|
| MM3 | 1 |
| MM2 | 1 |
| MM1 | 1 |
| MA | 1 |
| MQ | 1 |
| PROVI. SECT. | co py |

REMARKS: Sn-Biめっき

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-STRCT

QFP(Cu)内部構造図

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 03 | AN | 528 | E | PKGFTR 4182 |

Renesas Technology Corp.

343 4Q01326

SH. 1 E

D C B A QFP(CU) Gr. PKG

D.CHKD

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

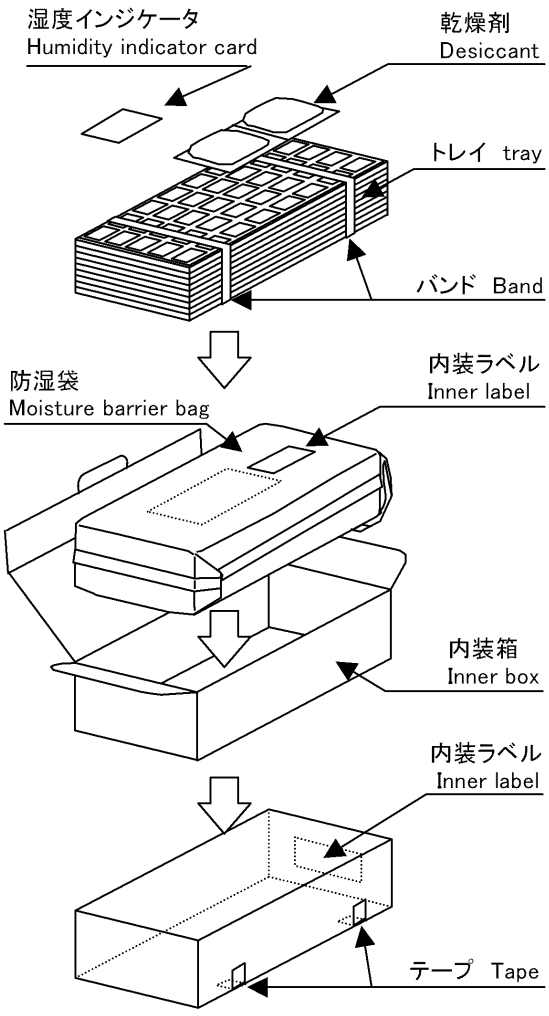
REVISIONS
P.1 , W#PKGFTR, S#4623

SYM. N.PL 1 5

△5

# トレイ包装仕様　Tray packing specification

## (a)包装フロー　Packing flow

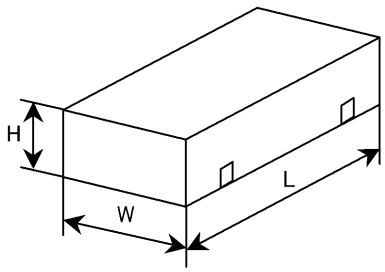



## (b)内装ラベル印字内容例
Example of Inner label content of print

| 略号 Abbreviation | データ名 Date name | 備考 note |
|---|---|---|
| P/N | 顧客型名 Customer No. | 必要な場合に表示 Display when it is necessary |
| PID | – | 弊社管理コード For our management |
| D/N | 製造者型名 Manufacture No. | – |
| QTY | 数量 Quantity | – |
| SPN | – | 弊社管理コード For our management |
| WP | 前工程生産国(若しくは地域) Wafer Process conutry (or region) name | 必要な場合に限り表示 Display only when it is necessary |
| AS | 後工程生産国(若しくは地域) Assembled conutry (or region) name | 必要な場合に表示 Display when it is necessary |
| (PARTIAL) | 端数表示 Partial display | 必要な場合に表示 Display when it is necessary |
| T/C | トレースコード Trace Code | – |
| S.LOT | – | 弊社管理コード For our management |
| Pb-Free T. | 鉛フリー表示 Pb-Free display | 製品が無鉛端子の場合に表示 Display when product is Pb-free terminal |
| MS Level | 開封後条件 Condition after opening | 必要な場合に表示 Display when it is necessary |

ー内装が複数ロットで構成される場合、ロットや数量情報をラベル上部に記載する場合があります。
When one interior is composed of two or more lots, information of lots or quantities might be described in the upper part of the label.

## (c)内装箱サイズ　Inner box size




unit : mm

| L | W | H |
|---|---|---|
| 330 | 152 | 75 |

箱の寸法は参考値です。
現物の寸法とは異なる場合がありますのでご了承願います。
The size of a box is a reference value and may differ from an actual size.

MチョウL D
MQ 1
PROVI. SECT. co py

| REMARKS | | | | | | |
|---|---|---|---|---|---|---|
| | | | | DWN. | PROJECTION | TITLE |
| | | | | CHKD. | | FTR-PCKNG |
| | | | | APPD. | SCALE NTS | 顧客向け包装図 |
| | | | | | REGD. | DWG.STAMP |

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 50 | 61 | ー ー ー, 3K00 | E | PKGFTR 4623 |

| D | C | B | A | Gr. |
|---|---|---|---|---|
| | | | TRAY-DRY-RT01 | TYPE |

D.CHKD

Renesas Technology Corp.

343 4Q01448

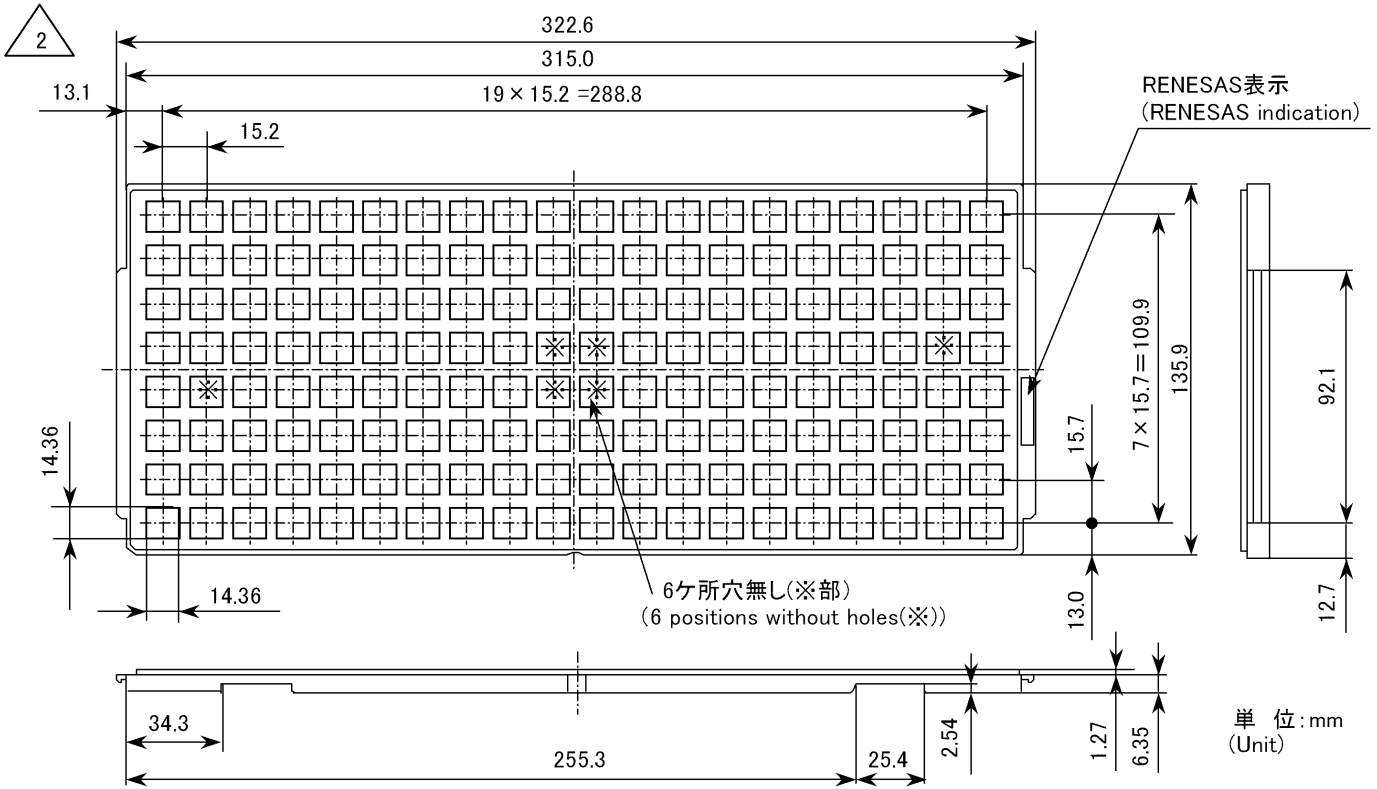
SH. 1 E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

DWN.:M.Kanai CHKD.:K.Goto APPD.:O.Ueda REGD.2007.02.27

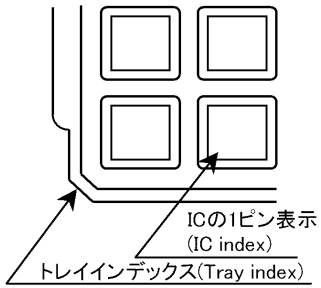
| SYM. | N.PL | REVISIONS | DATE | REVD. | CHKD. | APPD. |
|---|---|---|---|---|---|---|
| 2 | 2 | P.1 , W#PKGFTR, S#4719 | | | | |

D.CHKD. / PROVI. / SECT. / MQ 1 / Mチョウ L D / Co PY




| | |
|---|---|
| 型名 (Tray type) | L196-49 |
| 材質 (Material) | カーボンPPE (Carbon PPE) |
| 耐熱性 (Heat proof) | 130°CMAX , 24h |
| 表面抵抗 (Surface resistance value) | ≦1×10⁹Ω/□ |
| パッケージコード (Package code) | FP-64K,FP-64KV PLQP0048JB-A |
| 最大収納数 (Maximum storage No.) | 160 IC/トレイ 1280IC/内装箱 (160 IC/Tray 1280 IC/Inside box) |

ICのトレイ収納方向( IC placement direction)




トレイのインデックス
(図中の左下)に対して
ICの1ピンが
同じ方向(左下)に
なる様配列しています。

IC's are placed such
that IC 1st pin
the same direction
to tray index (bottom left).

REMARKS

| | E | D | C | B | A | Gr. |
|---|---|---|---|---|---|---|
| | | | | | L196-49 | TYPE |

DWN. / CHKD. / APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

# FTR-TRAY-OUTLN

# 顧客向けトレイ外形図

DWG.STAMP

| SD | TYPE | D.D | CLASS. | MD | WORK-SPEC No. |
|---|---|---|---|---|---|
| E | 03 | 6G | | E | PKGFTR 4719 |

Renesas Technology Corp.

343 4Q01665

SH. 1/E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ