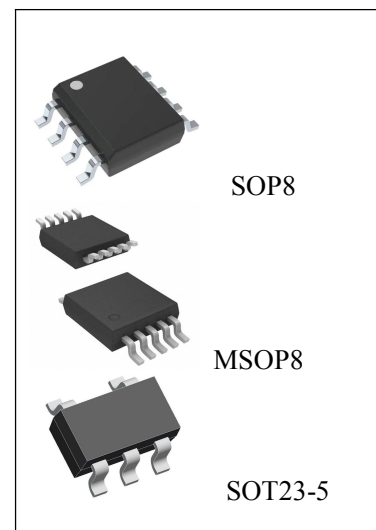


General Description

The D722 (dual)/D721(single) is low noise, low voltage, and low power operational amplifiers, that can be designed into a wide range of applications. The D721/2 has a high Gain- Bandwidth Product of 9MHz, a slew rate of 8.5V/ μ s, and a quiescent current of 0.97mA/amplifier at 5V.

The D721/2 is designed to provide optimal performance in low voltage and low noise systems. It provides rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage is 4mV for D721/2. It is specified over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$). The operating range is from 2.5V to 5.5V.

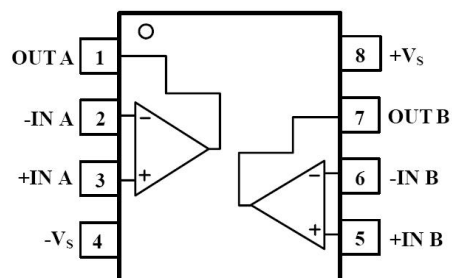


The single version D721 is available in SOT23-5 package and dual version D722 is available in SOP8 or MSOP8 packages.

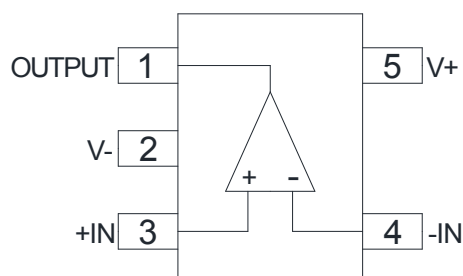
FEATURES

- Rail-to-Rail Input and Output: 1mV Typical V_{OS}
- High Gain-Bandwidth Product: 9MHz
- High Slew Rate: 8.5V/ μ s
- Settling Time to 0.1% with 2V Step: 0.36 μ s
- Overload Recovery Time: 0.4 μ s
- Low Noise : 8 nV/ $\sqrt{\text{Hz}}$
- Operates on 2.5 V to 5.5V Supplies
- Input Voltage Range = - 0.1 V to +5.6 V with $V_S = 5.5$ V
- Low Power: 0.65 mA/Amplifier Typical Supply Current

PIN CONFIGURATION



D722(SOP8/MSOP8)



D721(SOT23-5)

Applications

- Sensors ● Audio ● Active Filters ● A/D Converters
- Communications ● Test Equipment ● Cellular and Cordless Phones
- Laptops and PDAs ● Photodiode Amplification ● Battery-Powered Instrumentation

Absolute Maximum Ratings (Ta=25°C) *

Characteristic		Limit	Unit
Supply voltage		7.5	V
Common-mode input voltage		(-Vs)-0.5 ~ (+Vs)+0.5	V
Storage temperature range		-65 ~ +150	°C
Junction temperature		160	°C
Operation temperature range		-55 ~ +150	°C
Thermal resistance @ Ta=25°C	SOP8	125	°C/W
	MSOP8	216	°C/W
	SOT23-5	250	°C/W
Lead temperature range(soldering 10 sec)		260	°C
ESD susceptibility	HBM	1500	V
	MM	400	V

*: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Caution

This integrated circuit can be damaged by ESD. Silicore recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

(unless otherwise specified: $V_{CC+} = +5V$ with $V_{CC-} = 0V$, $V_{ICM} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range) *1

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
DC Performance						
Offset Voltage	V_{IO}	$T_{OP} = 25^{\circ}C$ $T_{min} < T_{OP} < T_{max}$		1.0	4.5 7.5	mV
Input Offset Voltage Drift	D_{VIO}/DT			5		$\mu V/^{\circ}C$
Input Offset Current *2	I_{IO}	$T_{OP} = 25^{\circ}C$ $T_{min} < T_{OP} < T_{max}$		1	10 100	pA
Input Bias Current *2	I_{IB}			1	10 100	pA
Common Mode Rejection Ratio $20 \log (\Delta V_{IC} / \Delta v_{io})$	CMR	0V to 5V, $V_{OUT} = 2.5V$ $T_{min} < T_{OP} < T_{max}$	64 55	86		dB
Supply Voltage Rejection Ratio $20 \log (\Delta V_{IC} / \Delta v_{io})$	SVR	$V_{CC} = 2.5 \sim 5V$	70	86		dB
Large Signal Voltage Gain	A_{VD}	$R_L = 10k\Omega$, $V_{OUT} = 0.5V$ to $4.5V$, $T = 25^{\circ}C$ $T_{min} < T_{OP} < T_{max}$	80 75	91		dB
High Level Output Voltage	$V_{CC} - V_{OH}$	$R_L = 10k\Omega$ $T_{min} < T_{OP} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{OP} < T_{max}$		15 100	40 40 150 150	mV
Low Level Output Voltage	V_{OL}	$R_L = 10k\Omega$ $T_{min} < T_{OP} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{OP} < T_{max}$		15 100	40 40 150 150	mV
Isink	I_{OUT}	$V_O = 5V$, $T_{OP} = 25^{\circ}C$ $T_{min} < T_{OP} < T_{max}$	40 30	50		mA
Isource		$V_O = 0V$, $T_{OP} = 25^{\circ}C$ $T_{min} < T_{OP} < T_{max}$	40 30	50		
Supply Current (per operator)	I_{CC}	No load, $V_{OUT} = 2.5V$ $T_{min} < T_{OP} < T_{max}$		0.92	1.2 1.2	mA
AC Performance						
Gain Bandwidth Product	GBP	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T_{OP} = 25^{\circ}C$		9		MHz
Unity Gain Frequency	F_u	$R_L = 2k\Omega$, $C_L = 100pF$, $T_{OP} = 25^{\circ}C$		8.5		MHz
Phase Margin	Φ_m	$R_L = 2k\Omega$, $C_L = 100pF$, $T_{OP} = 25^{\circ}C$		45		Degree
Gain Margin	Gm	$R_L = 2k\Omega$, $C_L = 100pF$, $T_{OP} = 25^{\circ}C$		8		dB
Slew Rate	SR	$R_L = 2k\Omega$, $C_L = 100pF$, $A_v = 1$, $T_{OP} = 25^{\circ}C$		4.8		V/ μs
Equivalent Input Noise Voltage	e_n	$f = 1kHz$, $T = 25^{\circ}C$ $f = 10kHz$, $T_{OP} = 25^{\circ}C$		27 21		$\frac{nV}{\sqrt{Hz}}$
Total Harmonic Distortion	THD+ e_n	$G = 1$, $f = 1kHz$, $R_L = 2k\Omega$, $B_w = 22kHz$, $T_{OP} = 25^{\circ}C$, $V_{ICM} = (V_{CC+} + 1)/2$, $V_{OUT} = 3.6V_{pp}$		0.0004		%

*1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.

*2. Guaranteed by design.

Application Information

Driving Capacitive Loads

The D721/2 can directly drive 4700pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should

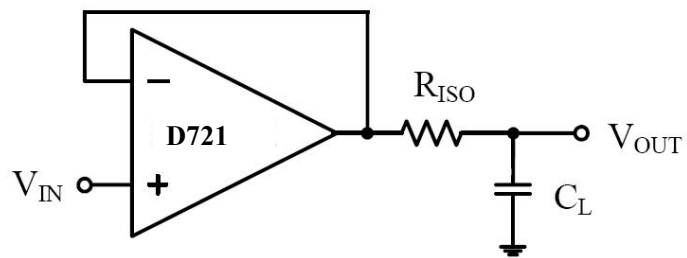


Fig 1. Indirectly Driving Heavy Capacitive Load

use an isolation resistor between the output and the capacitive load like the circuit in Fig1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD} .

An improvement circuit is shown in Fig2. It provides DC accuracy as well as AC stability. R_F provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

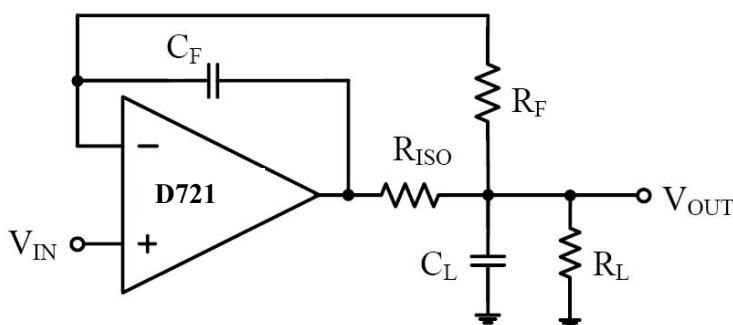


Fig2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The D721/2 operates from either a single +2.5V to +5.5V supply or dual $\pm 1.25\text{V}$ to $\pm 2.75\text{V}$ supplies. For single-supply operation, bypass the power supply V_{DD} with a $0.1\mu\text{F}$ ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate $0.1\mu\text{F}$ ceramic capacitors. $2.2\mu\text{F}$ tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

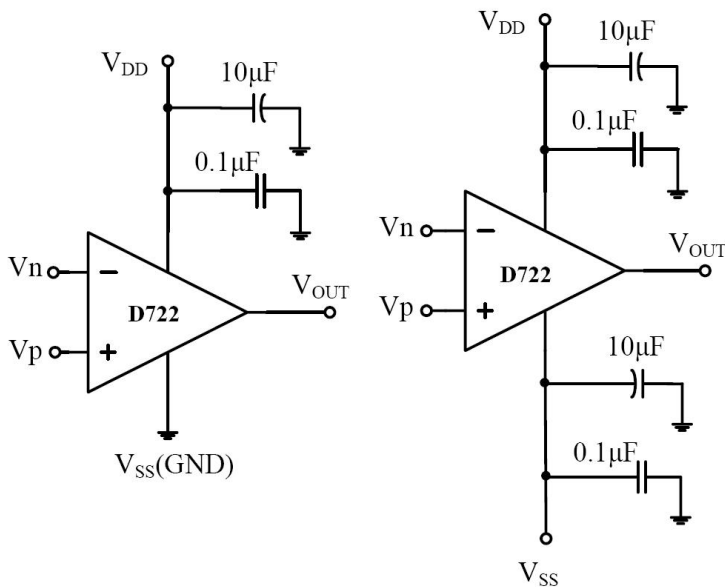


Fig3. Amplifier with Bypass Capacitors Grounding

Grounding

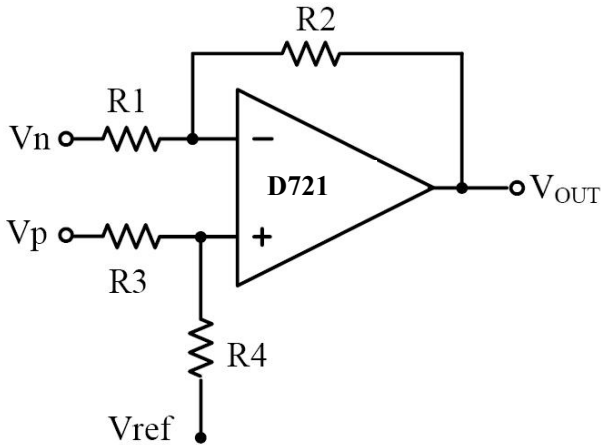
A ground plane layer is important for D721/2 circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Differential Amplifier

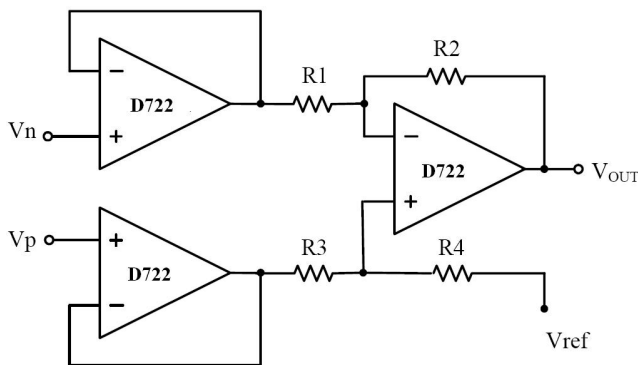
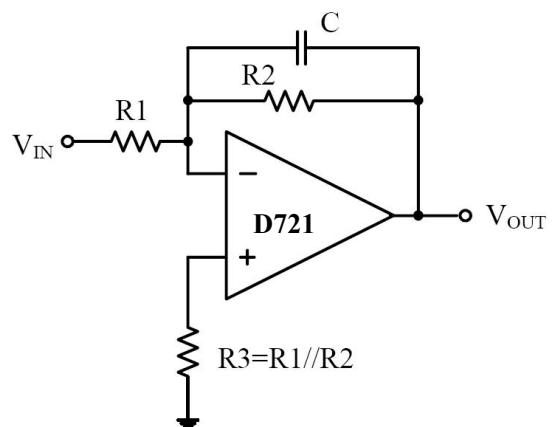
The circuit shown in Fig.4 performs the difference function. If the resistors ratios are equal ($R4 / R3 = R2 / R1$), then $V_{OUT} = (V_p - V_n) \times R2 / R1 + V_{ref}$.

**Fig4. Differential Amplifier****Instrumentation Amplifier**

The circuit in Fig.5 performs the same function as that in Fig.4 but with the high input impedance.

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of $(-R2/R1)$ and the -3dB corner frequency is $1/2\pi R2C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

**Fig5. Instrumentation Amplifier****Fig6. Low Pass Active Filter**

Outline Drawing

SOP8

Unit:mm

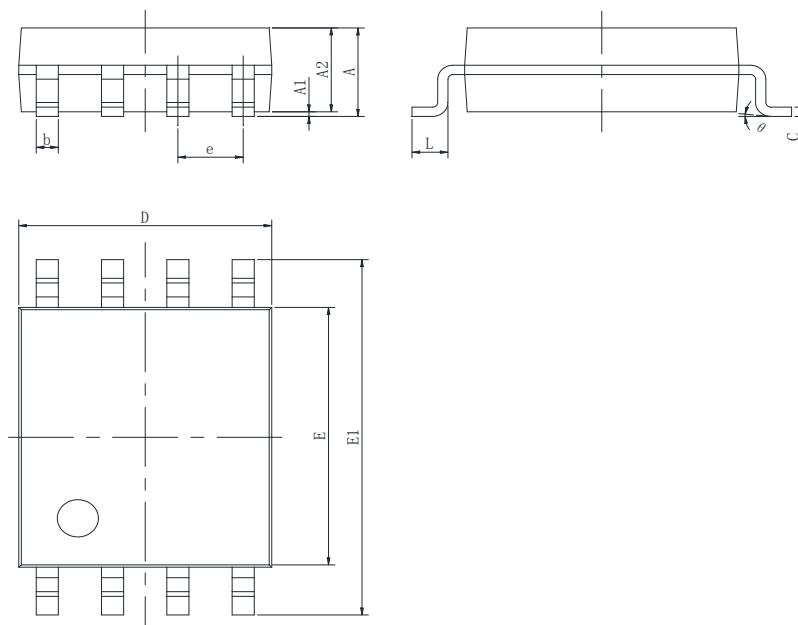
The diagram illustrates the SOP8 package dimensions in three views:

- Top View:** Shows the package footprint with dimensions D (total width), E (total height), and E1 (height including leads). A circular feature is located in the lower-left corner.
- Side View:** Shows the package profile with dimensions A (total height), A1 (height of the body), A2 (height of the leads), L (lead length), and θ (lead angle).
- Front View:** Shows the package with dimensions b (lead width), e (pitch), and A (total height).

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

MSOP8

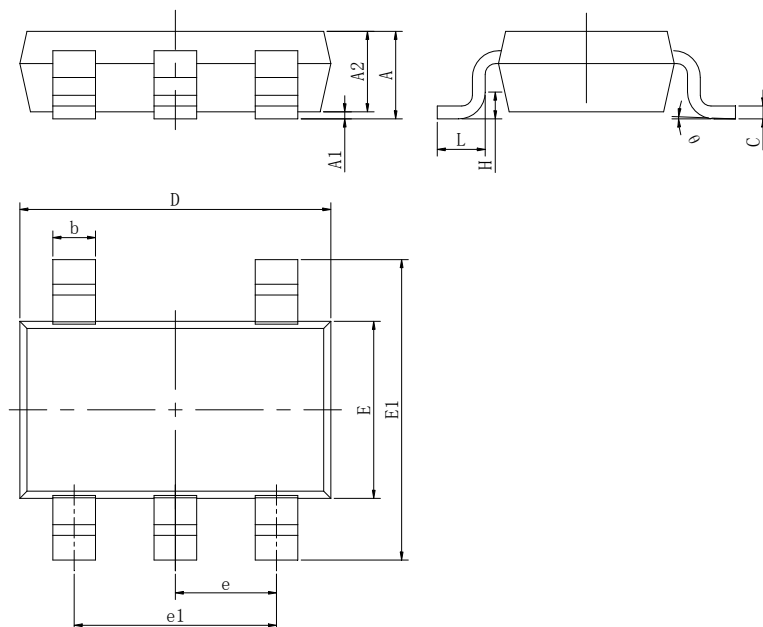
Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650(BSC)		0.026(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

SOT23-5

Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E	1.600	1.700	0.063	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037(BSC)	
e1	1.90 (BSC)		0.075(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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