

## General Description

The LTA77 is a 44-V micro-power alternative to the industry-standard OP77/OP07 precision amplifiers. The LTA77 offer outstanding dc precision and ac performance, including 25  $\mu\text{V}$  ultralow offset, below 0.3  $\mu\text{V}/^\circ\text{C}$  drift over temperature, 0.5  $\mu\text{V}_{\text{p-p}}$  input voltage noise and 0.9 MHz bandwidth. External offset trimming is not required in the majority of circuits.

A PSRR of 3  $\mu\text{V}/\text{V}$  (110 dB) and CMRR of 1.0  $\mu\text{V}/\text{V}$  (120 dB) maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the LTA77 ideally suited for high resolution instrumentation and other tight error budget systems.

The robust design of the LTA77 provides ease-of-use to the circuit designer: integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection. The LTA77 is optimized for operation at voltages from +6 V ( $\pm 3$  V) to +44 V ( $\pm 22$  V) over the extended temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

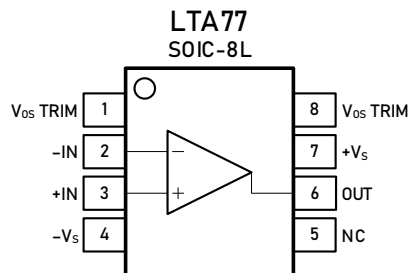
## Features and Benefits

- Offset Voltage: 25  $\mu\text{V}$  Maximum (LTA77E)
- Offset Voltage Drift: 0.3  $\mu\text{V}/^\circ\text{C}$  Maximum (LTA77E)
- 0.1 to 10 Hz Noise: 0.5  $\mu\text{V}_{\text{p-p}}$
- High Common-Mode Rejection: 0.1  $\mu\text{V}/\text{V}$  (140 dB)
- Wide Supply:  $\pm 3$  V to  $\pm 22$  V, 6 V to 44 V
- Wide Bandwidth: 0.9 MHz
- High Slew Rate: 0.48 V/ $\mu\text{s}$
- Low Quiescent Current: 1 mA per Amplifier
- EMI/RFI Filtered Inputs

## Applications

- Replaces OP07/OP77/OP97/OP177 with Improved Performance
- High-Side and Low-Side Current Sensing
- Multiplexed Data-Acquisition Systems
- Test and Measurement Equipment
- High-Resolution ADC Driver Amplifiers
- SAR ADC Reference Buffers
- Programmable Logic Controllers
- High Precision Comparator

## Pin Configuration (Top View)



## Pin Description

Symbol	Description
-IN	Inverting input of the amplifier. The voltage range is from $V_{S-}$ to $V_{S+}$ .
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
OUT	Amplifier output.
$V_{OS}$ TRIM	External input offset voltage adjustment
$+V_S$	Positive power supply. The voltage is from 6 V to 44 V. Split supplies are possible as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 6 V to 44 V.
$-V_S$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 6 V to 44 V.
NC	No connection.

## Ordering Information <sup>(1)</sup>

Type Number	Package Name	Package Quantity	Eco Class <sup>(2)</sup>	Marking Code
LTA77EXS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	ZT-77
LTA77FXS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	ZT-77

(1) Please contact to your Linearin representative for the latest availability information and product content details.

(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

## Limiting Value - In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, $V_{S+}$ to $V_{S-}$	44 V
Signal Input Terminals: Voltage, Current	$V_{S-}$ to $V_{S+}$ , $\pm 10$ mA
Output Short-Circuit	Continuous
Storage Temperature Range, $T_{stg}$	$-65$ °C to $+150$ °C
Junction Temperature, $T_j$	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

## ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 <sup>(1)</sup>	2 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 <sup>(2)</sup>	2 000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

## Electrical Characteristics

$V_S = \pm 15\text{ V}$ ,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CM} = V_S/2$ ,  $V_O = V_S/2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ , unless otherwise noted. Boldface limits apply over the specified temperature range,  $T_A = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ .

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<i>OFFSET VOLTAGE</i>						
Input offset voltage	$V_{OS}$	LTA77E		$\pm 10$	$\pm 25$	$\mu\text{V}$
		LTA77F		$\pm 20$	$\pm 60$	
Offset voltage drift	$V_{OS\text{ TC}}$	LTA77E, $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$			$\pm 0.3$	$\mu\text{V}/^\circ\text{C}$
		LTA77E, $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$			$\pm 0.6$	
Long-term stability <sup>(1)</sup>	$V_{OS\text{ TC}}$	LTA77E		$\pm 0.3$		$\mu\text{V}/\text{Mo}$
		LTA77F		$\pm 0.4$		
Power supply rejection ratio	PSRR	LTA77E, $V_S = \pm 3\text{ to } \pm 18\text{ V}$		0.7	3	$\mu\text{V}/\text{V}$
		LTA77F, $V_S = \pm 3\text{ to } \pm 18\text{ V}$		0.7	5	
<i>INPUT BIAS CURRENT</i>						
Input bias current	$I_B$	LTA77E			2	nA
		LTA77F			2.8	
Input offset current	$I_{OS}$		0.2			nA
<i>NOISE</i>						
Input voltage noise	$V_n$	$f = 0.1\text{ to }10\text{ Hz}$		0.5		$\mu\text{V}_{P-P}$
Input current noise	$I_n$	$f = 0.1\text{ to }10\text{ Hz}$		10		$\text{pA}_{P-P}$
<i>INPUT VOLTAGE</i>						
Common-mode voltage range	$V_{CM}$		$\pm 13$	$\pm 14$		V
Common-mode rejection ratio	CMRR	LTA77E, $V_{CM} = \pm 13\text{ V}$		0.1	1.0	$\mu\text{V}/\text{V}$
		LTA77F, $V_{CM} = \pm 13\text{ V}$		0.1	1.6	
<i>INPUT IMPEDANCE</i>						
Input capacitance	$C_{IN}$	Differential		2.0		pF
		Common mode		3.5		
<i>OPEN-LOOP GAIN</i>						
Open-loop voltage gain	$A_{VOL}$	LTA77E, $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	5,000	12,000		V/mV
		LTA77F, $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	2,000	6,000		
<i>FREQUENCY RESPONSE</i>						
Gain bandwidth product	GBW			0.9		MHz
Slew rate	SR	$G = +1$ , $C_L = 100\text{ pF}$ , $V_O = 1.5\text{ to }3.5\text{ V}$		0.5		V/ $\mu\text{s}$
<i>OUTPUT</i>						
Output voltage swing	$V_D$	$R_L = 10\text{ k}\Omega$		$\pm 14$	$\pm 14.9$	V
		$R_L = 1\text{ k}\Omega$		$\pm 13.5$	$\pm 14.5$	
Short-circuit current	$I_{SC}$			$\pm 22$		mA
Offset adjustment range				$\pm 1.5$		mV

(1) Long-term input offset voltage stability refers to the averaged trend line of  $V_{OS}$  vs. time over extended periods after the first 30 days of operation.

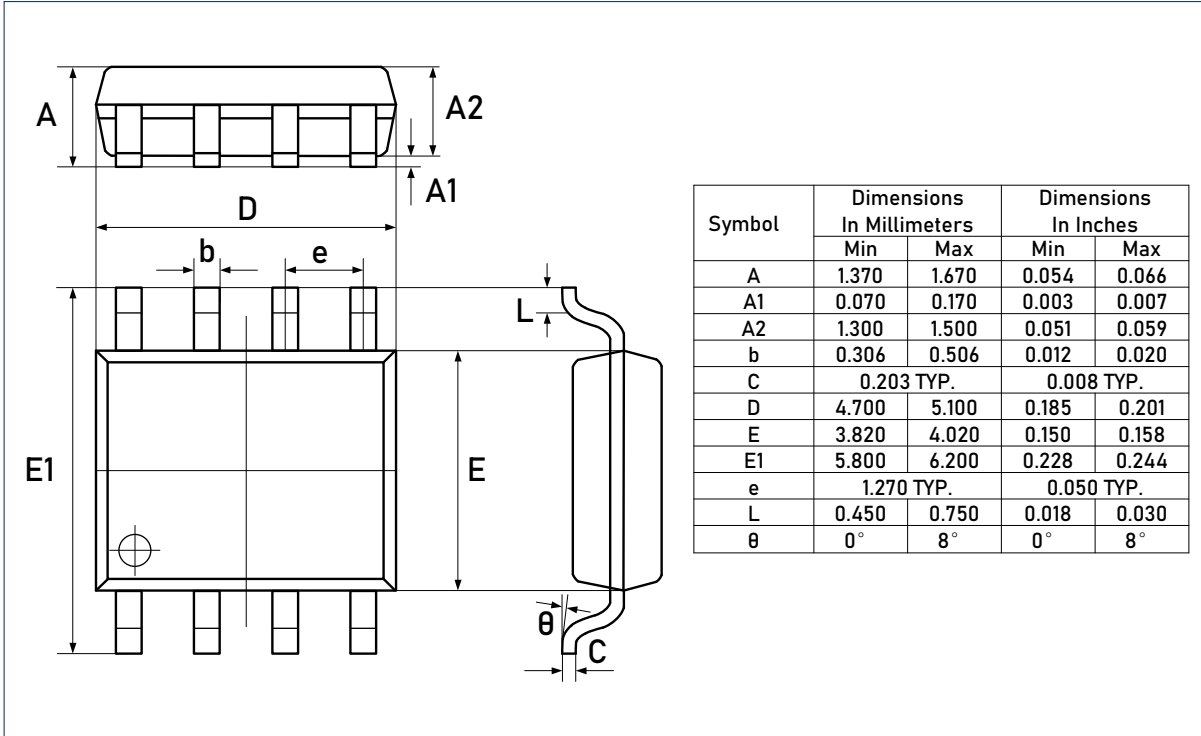
## Electrical Characteristics (continued)

$V_S = \pm 15\text{ V}$ ,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CM} = V_S/2$ ,  $V_O = V_S/2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ , unless otherwise noted. Boldface limits apply over the specified temperature range,  $T_A = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ .

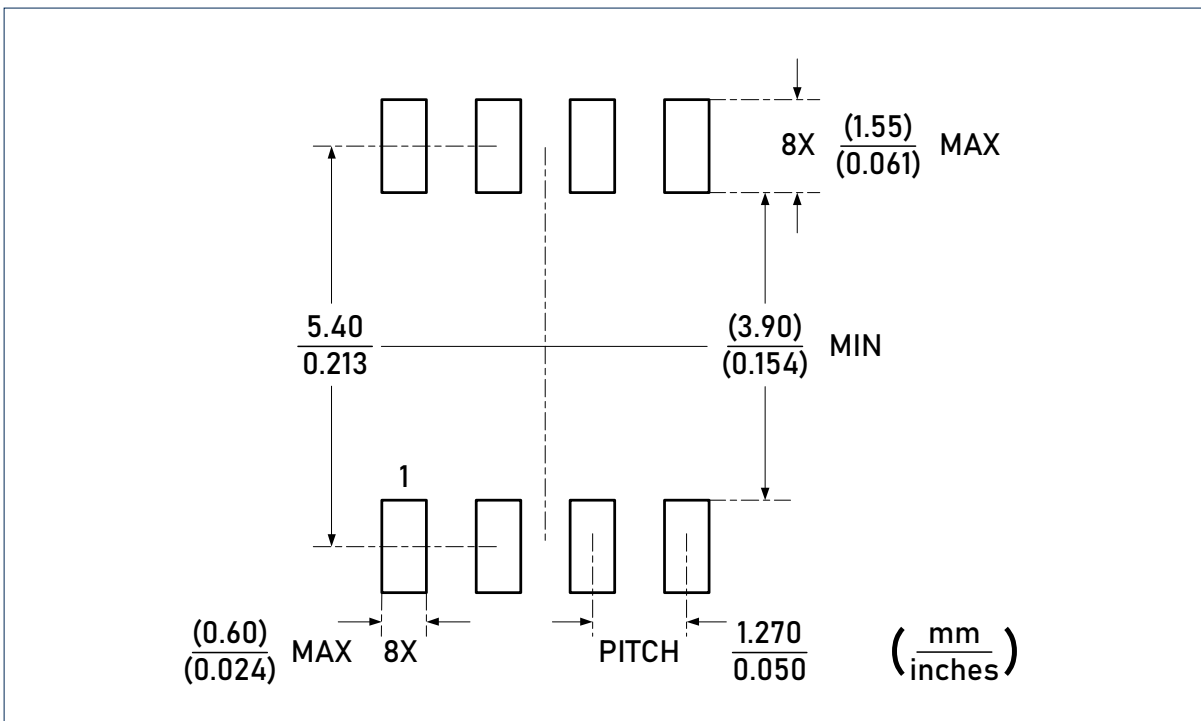
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<i>POWER SUPPLY</i>						
Operating supply voltage	$V_S$	$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$	<b>6</b>		<b>44</b>	V
Quiescent current (per amplifier)	$I_Q$	$V_S = \pm 15\text{ V}$ , no load		0.22	0.31	mA
		$V_S = \pm 3\text{ V}$ , no load		0.21	0.3	
<i>THERMAL CHARACTERISTICS</i>						
Operating temperature range	$T_A$		<b>-40</b>		<b>+125</b>	$^\circ\text{C}$
Package Thermal Resistance	$\theta_{JA}$	SOIC-8L		125		$^\circ\text{C/W}$

Package Outlines (continued)

DIMENSIONS, SOIC-8L



RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



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## Important Notice

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For additional product information, or full datasheet, please contact with the Linearin's Sales Department or Representatives.