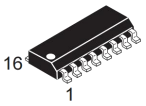
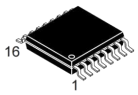
Features

- Complies with JEDEC standard no. 7A
- CMOS input levels
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Asynchronous reset
- Positive-edge triggered clock
- ESD protection:
  HBM JESD22-A114F exceeds 2000 V
  MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C



SOP16



TSSOP16

SSOP16

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC161M/TR	SOP-16	74HC161	REEL	2500pcs/reel
74HC161MT/TR	TSSOP-16	74HC161	REEL	2500pcs/reel
74HC161MS/TR	SSOP-16	74HC161	REEL	2500pcs/reel

General description

The 74HC161 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positivegoing edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset HIGH or LOW.

A LOW at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input (MR) sets Q0 to Q3 LOW regardless of the levels at input pins CP, PE, CET and CEP (thus providing an asynchronous clear function). The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$F_{max} = \frac{1}{t_{p(max)}(CP\,to\,TC)+t_{SU}(CEP\,to\,CP)}$$

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Functional diagram

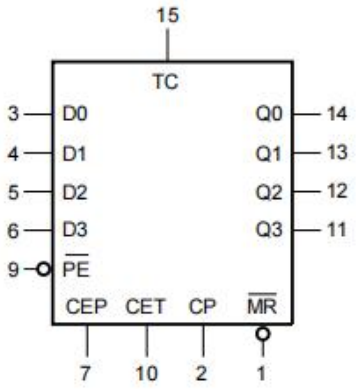


Fig.1.Logic symbol

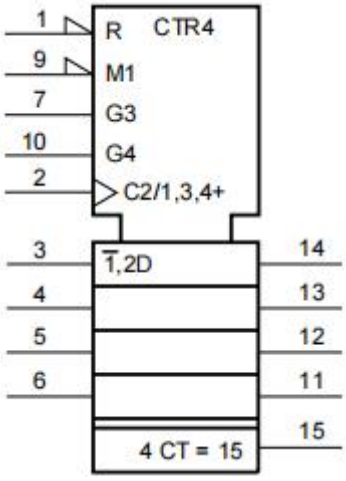


Fig.2.IEC logic symbol

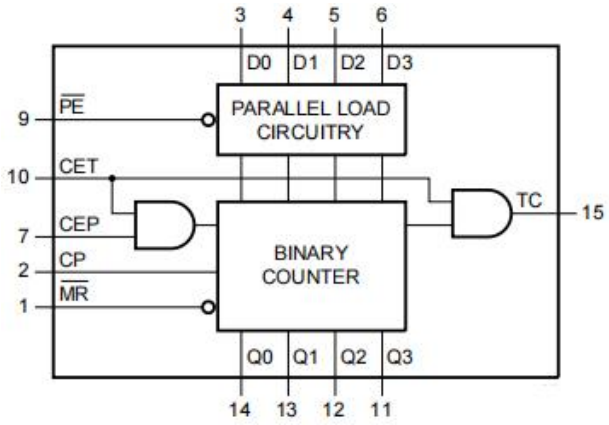


Fig. 3. Functional diagram

Presettable synchronous 4-bit binary counter; asynchronous reset

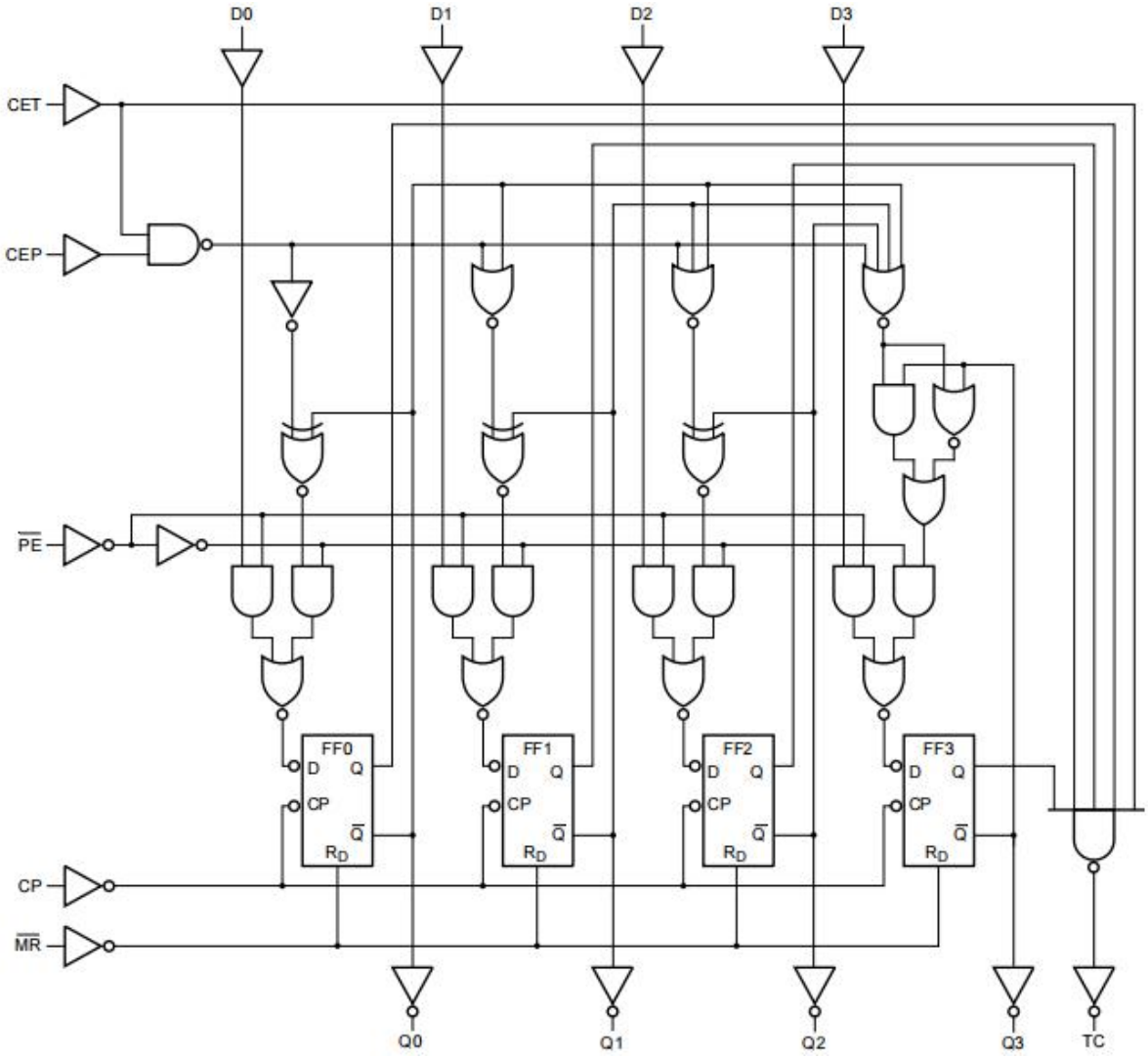


Fig. 4. Logic diagram

Pin Configuration

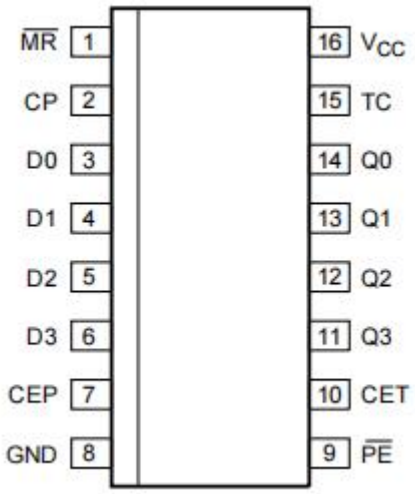


Fig 5.Pin configuration SOP-16

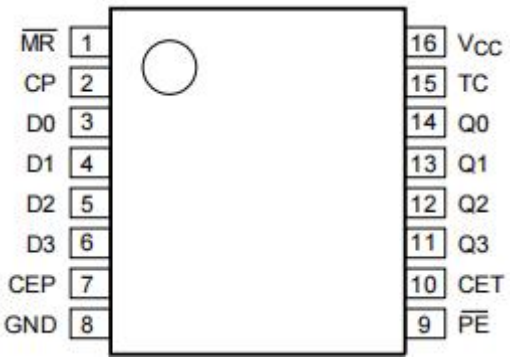


Fig 6.Pin configuration SSOP16 and TSSOP16

Pin description

Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
VCC	16	supply voltage

Function table[1]

Operating modes	Input						Output	
	MR	CP	CEP	CET	PE	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[2]
Count	H	↑	h	h	h	X	count	[2]
Hold (do nothing)	H	X	l	X	h	X	qn	[2]
	H	X	X	l	h	X	qn	L

1. H = HIGH voltage level

   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition L = LOW voltage level

   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

   qn = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition

   X = don't care

   ↑ = LOW-to-HIGH clock transition

2. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)

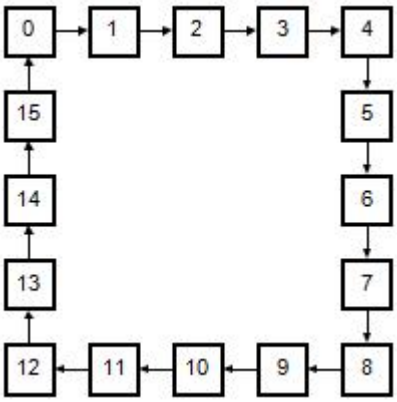
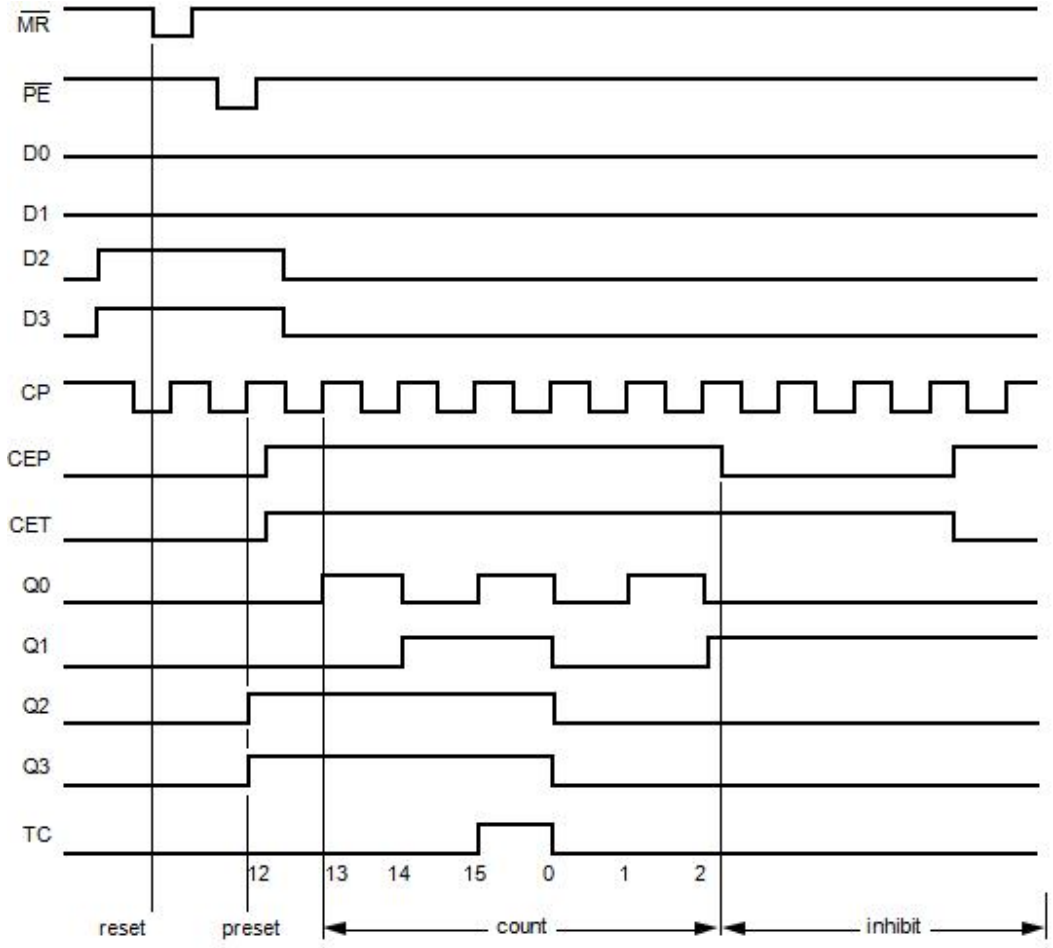


Fig. 7. State diagram



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 8.Typical timing sequence

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	V_O = -0.5 V to V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
Tstg	storage temperature		-65	+150	°C
Ptot	total power dissipation	[1]	-	500	mW

For SO16 packages: above 70 °C the value of Ptot derates linearly at 8mW/K.

For (T)SSOP16 packages: above 60 °C the value of Ptot derates linearly at 5.5mW/K.

Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	VCC	V
V_O	output voltage		0	-	VCC	V
Tamb	ambient temperature		-40	+25	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I_O = -4.0; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	V
		I_O = -5.2; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	μA
C_I	input capacitance		-	3.5	-	-	-	pF

Dynamic characteristics

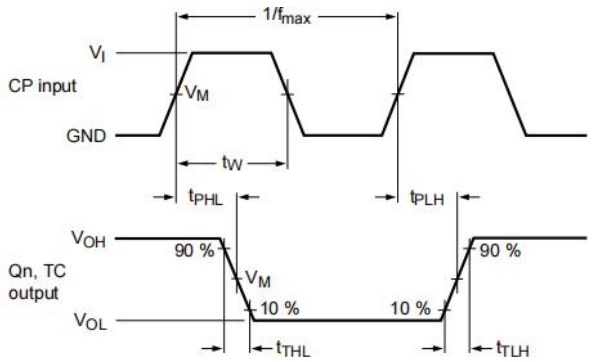
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 9[1]						
		V_{CC} = 2.0 V	-	61	190	-	240	ns
		V_{CC} = 4.5 V	-	22	38	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	19	-	-	-	ns
		V_{CC} = 6.0 V	-	18	32	-	41	ns
		CP to TC; see Fig. 9						
		V_{CC} = 2.0 V	-	69	215	-	270	ns
		V_{CC} = 4.5 V	-	25	43	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	ns
		V_{CC} = 6.0 V	-	20	37	-	46	ns
		CET to TC; see Fig. 10						
		V_{CC} = 2.0 V	-	33	150	-	190	ns
		V_{CC} = 4.5 V	-	12	30	-	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	ns
		V_{CC} = 6.0 V	-	10	26	-	38	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 11						
		V_{CC} = 2.0 V	-	63	210	-	265	ns
		V_{CC} = 4.5 V	-	23	42	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	ns
		V_{CC} = 6.0 V	-	18	36	-	45	ns
		$\overline{MR}$ to TC; see Fig. 11						
		V_{CC} = 2.0 V	-	63	220	-	275	ns
		V_{CC} = 4.5 V	-	23	44	-	55	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	ns
		V_{CC} = 6.0 V	-	18	37	-	47	ns
t_t	transition time	see Fig. 9 and Fig. 10 [2]						
		V_{CC} = 2.0 V	-	19	75	-	95	ns
		V_{CC} = 4.5 V	-	7	15	-	19	ns
		V_{CC} = 6.0 V	-	6	13	-	16	ns
t_W	pulse width	CP; HIGH or LOW; see Fig. 9						
		V_{CC} = 2.0 V	80	22	-	100	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	ns
		$\overline{MR}$; LOW; see Fig. 11						
		V_{CC} = 2.0 V	80	19	-	100	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
trec	recovery time	MR to CP; see Fig. 11						
		V_{CC} = 2.0 V	100	19	-	125	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	ns
tsu	set-up time	Dn to CP; see Fig. 12						
		V_{CC} = 2.0 V	80	25	-	100	-	ns
		V_{CC} = 4.5 V	16	9	-	20	-	ns
		V_{CC} = 6.0 V	14	7	-	17	-	ns
		$\overline{PE}$ to CP; see Fig. 12						
		V_{CC} = 2.0 V	100	30	-	125	-	ns
		V_{CC} = 4.5 V	20	11	-	25	-	ns
		V_{CC} = 6.0 V	17	9	-	21	-	ns
		CEP, CET to CP; see Fig. 13						
		V_{CC} = 2.0 V	170	47	-	215	-	ns
		V_{CC} = 4.5 V	34	17	-	43	-	ns
		V_{CC} = 6.0 V	29	14	-	37	-	ns
th	hold time	Dn, $\overline{PE}$, CEP, CET to CP; see Fig. 12 and Fig. 13						
		V_{CC} = 2.0 V	0	-14	-	0	-	ns
		V_{CC} = 4.5 V	0	-5	-	0	-	ns
		V_{CC} = 6.0 V	0	-4	-	0	-	ns
fmax	maximum frequency	CP; see Fig. 9						
		V_{CC} = 2.0 V	4.6	13	-	3.6	-	MHz
		V_{CC} = 4.5 V	23	40	-	18	-	MHz
		V_{CC} = 5.0 V; CL = 15 pF	-	44	-	-	-	MHz
		V_{CC} = 6.0 V	27	48	-	21	-	MHz
CPD	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; [3] fi = 1 MHz	-	33	-	-	-	pF

1. t_{pd} is the same as t_{PHL} and t_{PLH}.
2. tt is the same as t_{THL} and t_{TLH}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
4. $P_D = C_{PD} \times V_{CC}^2 \times fi \times N + \sum(C_L \times V_{CC}^2 \times fo)$ where:
5. fi = input frequency in MHz;
6. fo = output frequency in MHz;
7. C_L = output load capacitance in pF;
8. V_{CC} = supply voltage in V;
9. N = number of inputs switching;
10. $\sum(C_L \times V_{CC}^2 \times fo)$=sum of outputs.

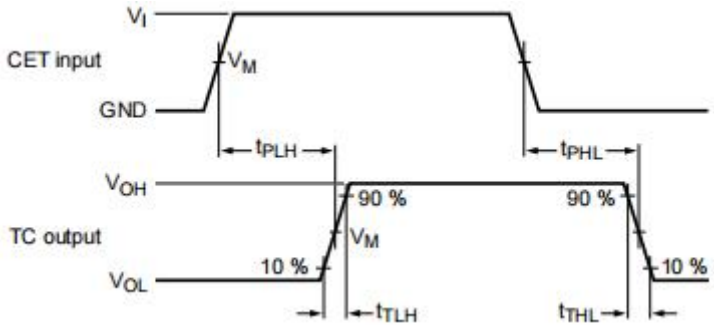
SWITCHING WAVEFORMS



Measurement points are given in **Table 8**.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

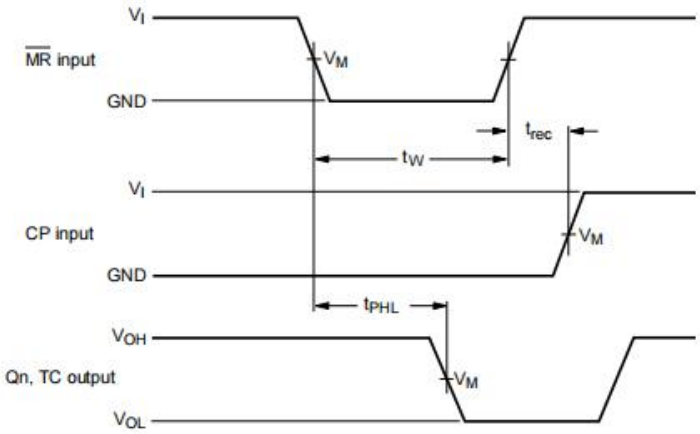
Fig. 9. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency



Measurement points are given in Table 8.

Logic levels VOL and VOH are typical output voltage levels that occur with the output load.

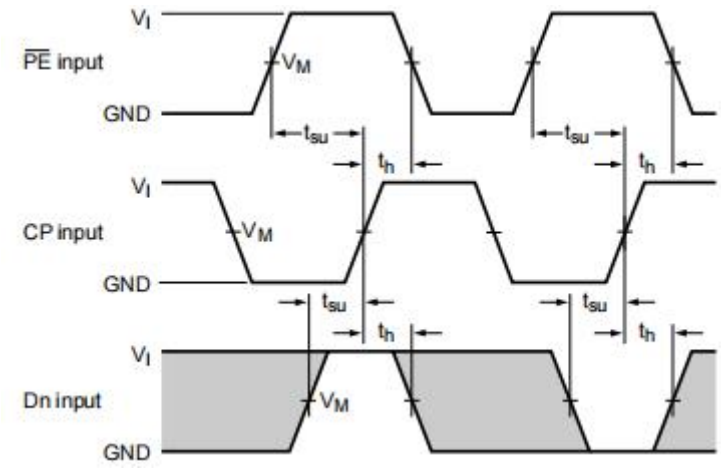
Fig. 10. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times



Measurement points are given in Table 8.

Logic levels VOL and VOH are typical output voltage levels that occur with the output load.

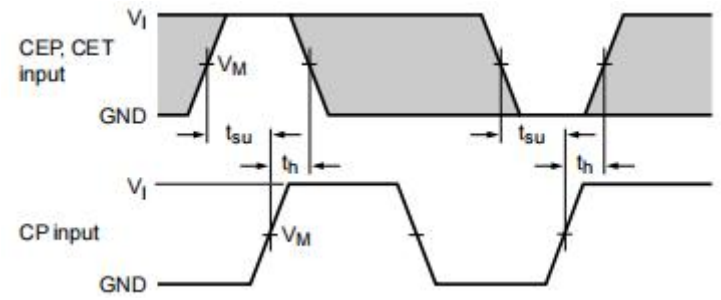
Fig. 11. The master reset (MR) pulse width, master reset to output (Qn, TC) propagation delays, and the master reset to clock (CP) recovery times



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 12. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times



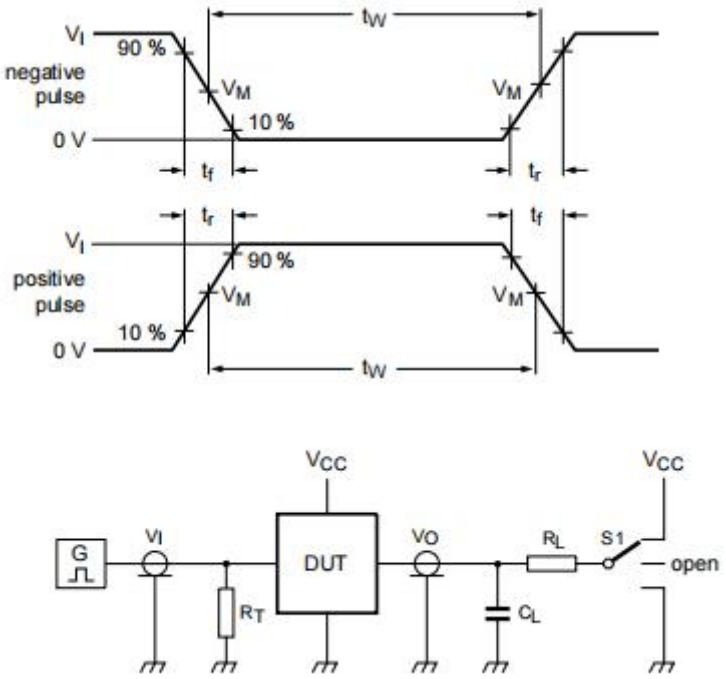
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 13. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Measurement points

Input		Output
VM	**VI**	**VM**
0.5 × V_{CC}	GND to V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.

Test circuit definitions:

RT = Termination resistance should be equal to output impedance Zo of the pulse generator

CL = Load capacitance including jig and probe capacitance

RL = Load resistance.

S1 = Test selection switch

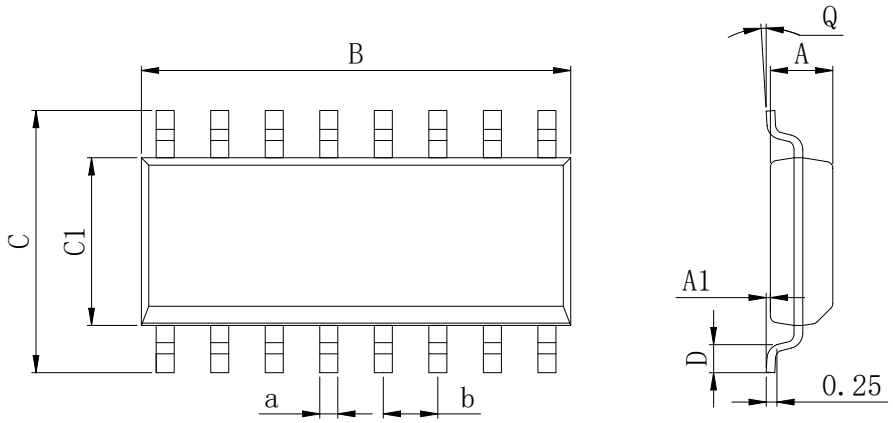
Fig. 14. Test circuit for measuring switching times

Test data

Input		Load		S1 position
V_I	tr, tf	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open

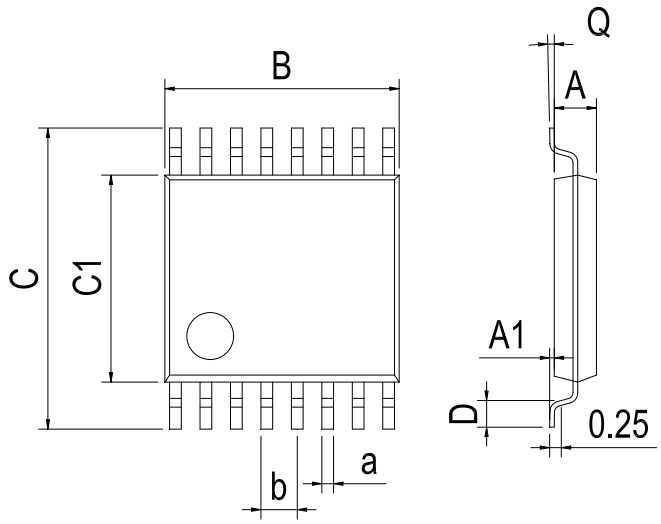
Physical Dimensions

SOP16



Dimensions In Millimeters(SOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

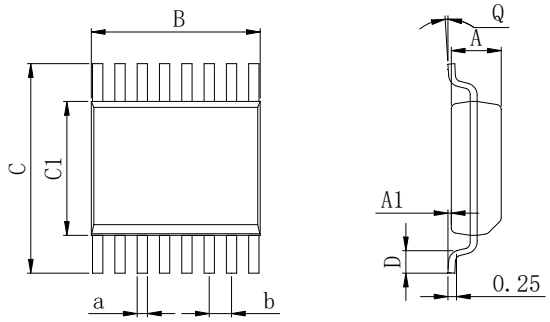
TSSOP16



Dimensions In Millimeters(TSSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Physical Dimensions

SSOP16



Dimensions In Millimeters(SSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.20	0.65 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.25	

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