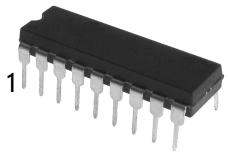
Pulse Width Modulation Control Circuit

Features

- 8.0V to 35V Operation
- 5.0V ±1% Trimmed Reference
- 1.0Hz to 400KHz Oscillator Range
- Dual Source/Sink Current Outputs: ± 100mA
- Digital Current Limiting
- Programmable Dead Time
- Undervolage-Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization



DIP18

SOP18

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
SG3526N	DIP18	SG3526	TUBE	800pcs/box
SG3526M/TR	SOP18	SG3526	REEL	2500pcs/reel

General Description

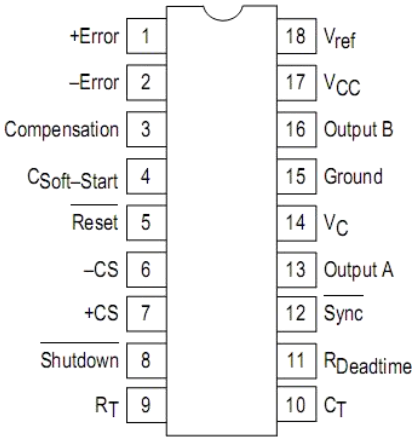
The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference,sawtooth oscillator,error amplifier, pulse width modulator, pulse metering and steering logic,and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout,digital current limiting,double pulse inhibit,adjustable deadtime and a data latch for single pulse metering;. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum fiexibility. The versatility of this device enables implementation or transformer coupled.

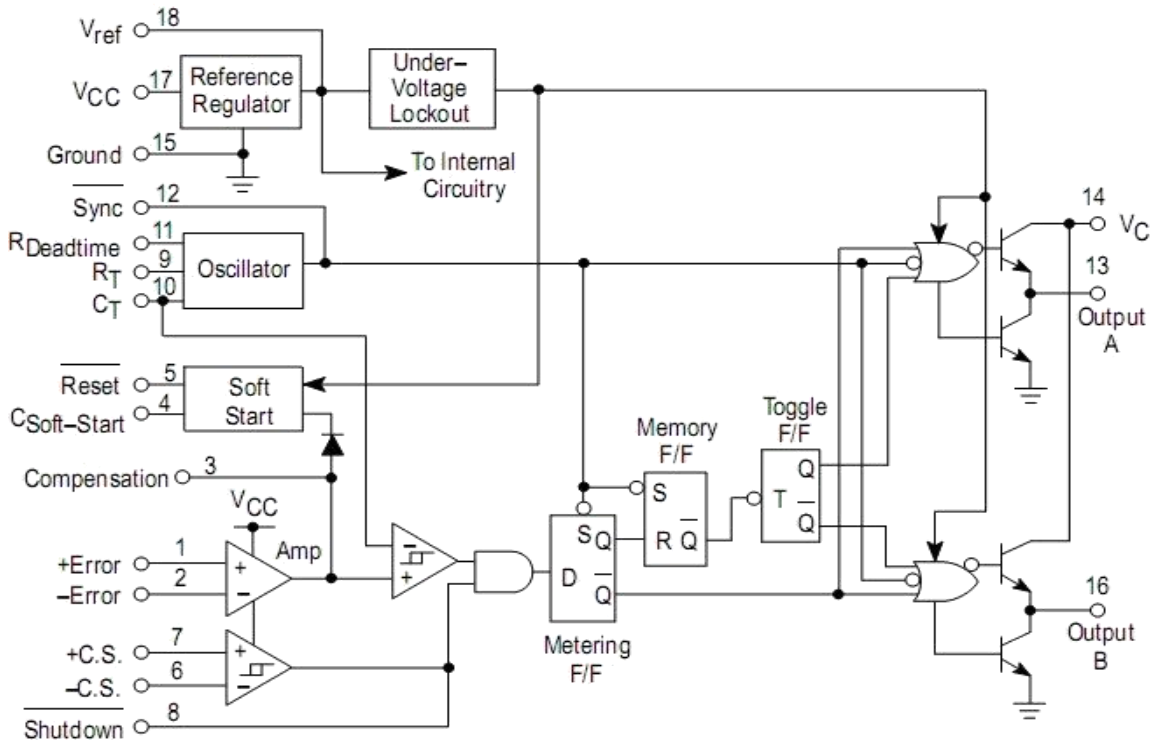
Pin Configuration

DIP18/SOP18



（Top View）

Representative Block Diagram



Maximum Ratings（Note1）

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	+40	Vdc
Collector Supply Voltage	Vc	+40	Vdc
Logic Inputs		-0.3 to + 5.5	V
Analog Inputs		-0.3 to +5.5	V
Output Current,Source or Sink	Io	±200	mA
Reference Load Current(Vcc=40V Note2)	Iref	50	mA
Logic Sink Current		15	mA
Power Dissipation Ta=+25℃ (note3)	Pd	1000	mW
Operating Temperature Range	Ta	0~70	℃
Storage Temperature Range	Tstg	-65 to +150	℃
Lead Temperature(Soldering, 10Seconds)	Tsolder	±300	℃

NOTES:

1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50℃.

Recommended Operating Conditions

Charachteristics	Symbol	Min	Max	Unit
Supply Voltage	Vcc	8.0	35	Vdc
Collector Supply Voltage	Vc	4.5	35	Vdc
Output Sink/Source Current(Each Output)	Io	0	±100	mA
Reference Load Current	Iref	0	20	mA
Oscilliator Frequency Range	Fosc	0.001	400	Khz
Oscillator Timing Resistor	Rt	2.0	150	KΩ
Osicllator Timing Capacitor	Ct	0.001	20	uF
Available Deadtime Range(40Khz)	-	3.0	50	%
Operating Junction Temperature Range	Tj	0	+125	℃

ELECTRICAL CHARACTERISTICS

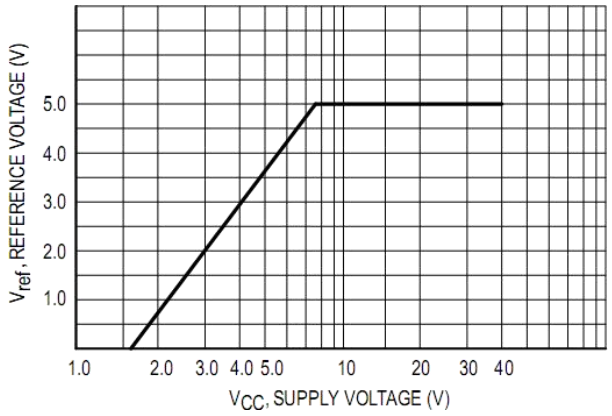
(VCC = +15 Vdc, TJ = Tlow to Thigh [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Reference Section					
Reference Output Voltage(Tj=+25℃)	Vref	4.90	5.00	5.10	V
Line Regulation(+8.0V ≤Vcc≤+35V)	Regline	-	10	30	mV
Load Regulation (0mA≤IL≤20mA)	Regload	-	10	50	mV
Short Circuit Current(Verf=0V)	Isc	25	80	125	mA
Undervoltage Lockout					
Reset Output Voltage(Vref=+3.8V)		-	0.2	0.4	V
Reset Output Voltage(Vref=+4.8V)		2.4	4.8	-	V
Oscillator Section(Note5)					
Initial Accuracy(Tj=+25℃)		-	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0V ≤Vcc≤+35V)	Δfosc/ Δ VCC	-	0.5	1.0	%
Minimun Frequency （Rt=150Kohm,Ct=20uF）	Fmin	-	0.5	-	Hz
Maximum Frequency (Rt=2.0Kohm,Ct=0.001uF)	Fmax	400	-	-	KHz
Sawtooth Peak Voltage （Vcc=35V）	Vosc(p)	-	3.0	3.5	V
Sawtooth Valley Voltage(Vcc=8.0V)	Vosc(V)	0.45	0.8	-	V
Error Amplifier Section (note6)					
Input Offset Voltage	Vio	-	2.0	10	mV
Input Bias Current	Iib	-	-350	-2000	nA
Input Offset Current	Iio	-	35	200	nA
Characteristics	Symbol	Min	Typ	Max	Unit

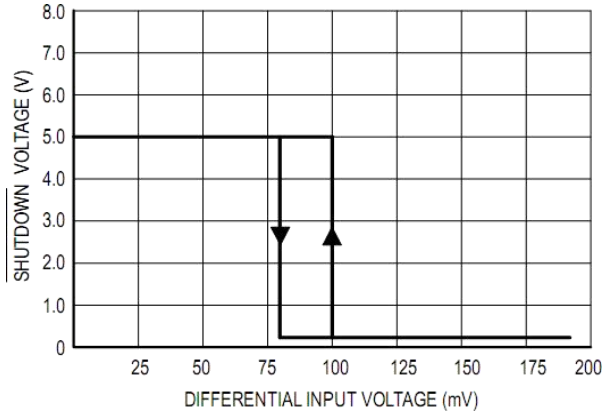
DC Open Loop Gain(Rl≥10Mohm)	Av	60	72	-	dB
High Output Voltage (Vpin1-Vpin2≥+150mV，Isource=100uA)	Voh	3.6	4.2	-	V
Low Output Voltage (Vpin2-Vpin1≥+150mV，Isink=100uA)	Vol	-	0.2	0.4	V
Common Mode Rejection Ratio(Rs≤2.0Kohm)	CMRR	70	94	-	dB
Power Supply Rejection Ration(+12V≤Vcc≤+18V)	PSRR	66	80	-	dB
PWM Comparator Section(Note5)					
Minimum Duty Cycle (Vcompensation = +0.4V)	Dcmin	-	-	0	%
Maximum Duty Cycle (Vcompensation = +3.6V)	Dcmax	45	49	-	%
Digital Ports(SYNC,SHUTDOWN,RESET)					
Output Voltage (High Logic Level) (Isource=40uA) (Low Logic Level) (Isink=3.6mA)	Voh Vol	2.4 -	4.0 0.2	- 0.4	V
Input Current-High Logic Level (High Logic Level)（Vih=+2.4V） (Low Logic Level) (Vil = +0.4V)	Iih Iil	- -	-125 -225	-200 -360	uA
Current Limit Comparator Section(note7)					
Sense Voltage(Rs≤50 Ω)	Vsense	80	100	120	mA
Input Bias Current	Iib	-	-3.0	-10	uA
Soft-Start Section					
Error Clamp Voltage(Reset=+0.4V)		-	0.1	0.4	V
Csoft-Start Charging Current(Reset=+2.4V)	Ics	50	100	150	uA
Output Drivers（each output,Vc=+15Vdc） Unless otherwise noted.					
Output High Level Isource = 20mA Isource = 100mA	Voh	12.5 12	13.5 13	- -	V
Output Low Level Isink = 20 mA Isink = 100mA	Vol	- -	0.2 1.2	0.3 2.0	V
Collector Leakage,Vc=+40V	Ic(Leak)	-	50	150	uA
Rise Time(CL=1000pF)	Tr	-	0.3	0.6	uS
Fall Time（CL=1000pF）	Tf	-	0.1	0.2	uS
Supply Current	Icc	-	18	30	mA
（Shutdown = +0.4V，Vcc=+35V，Rt=4.12K Ω）					

Notes:

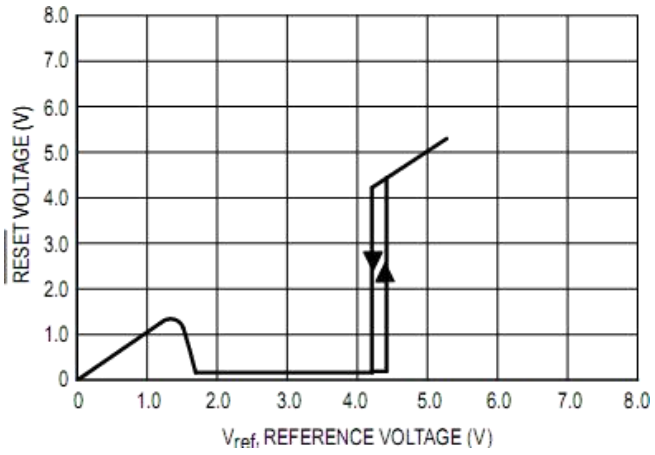
4. Tlow = 0°CThigh = +125℃
5. fosc=40KHz（Rt=4.12k Ω±1%,CT=0.01uF±1%，RD=0 Ω）
6. 0V ≤ VCM ≤ +5.2V
7. 0V ≤ VCM ≤ +12V



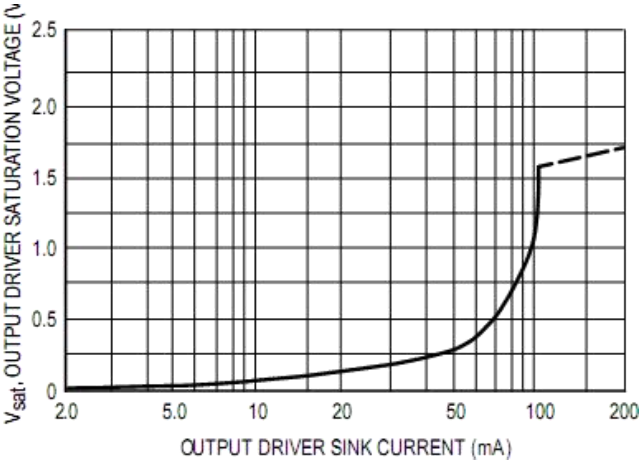
Reference Voltage as a Function Supply Votage



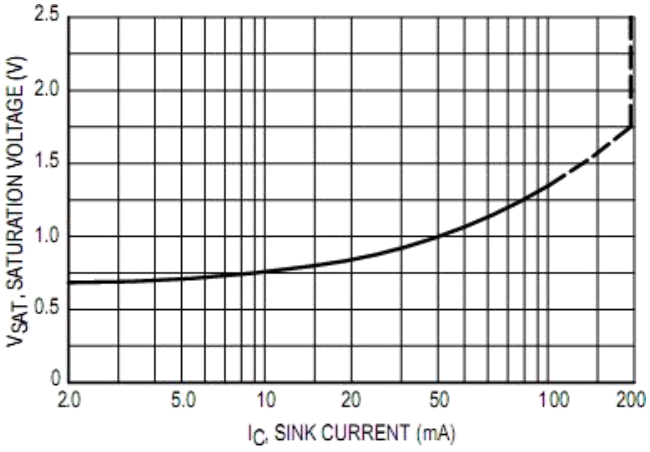
Current Limit Comparator Threshold



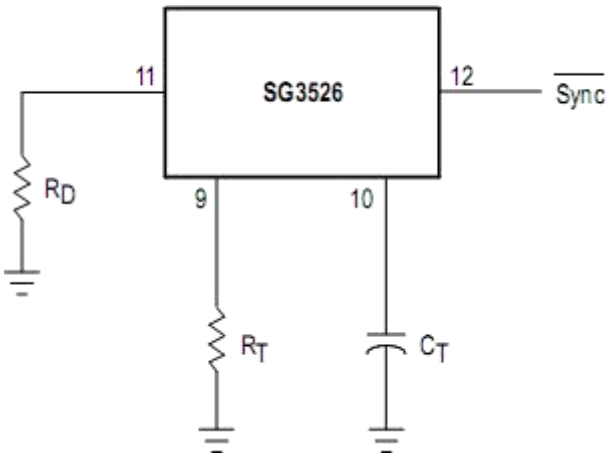
UnderVoltage Lockout Characteristic



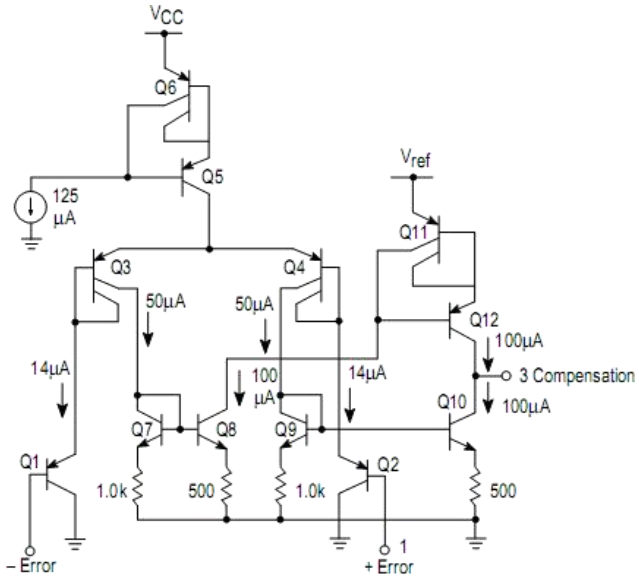
Output Driver Saturation Voltage as a Function of Sink Current



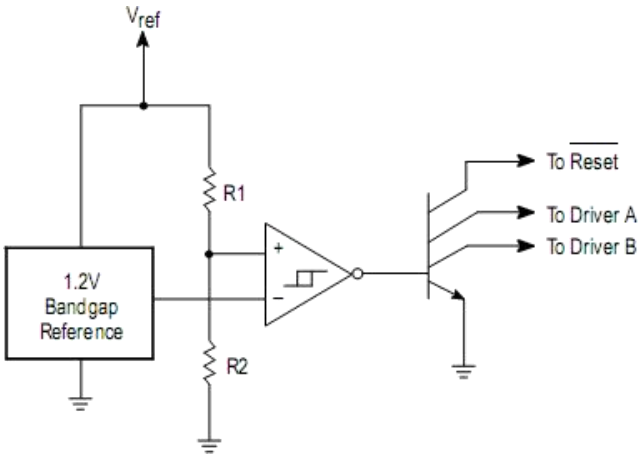
Vc Saturation Voltage as a Function of Sink Current



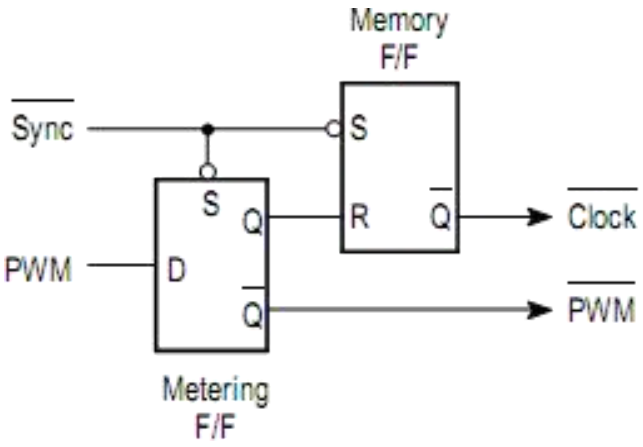
Oscillator Connections



Error Amplifier



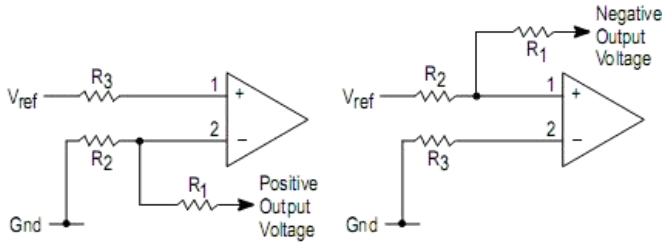
Undervotage Lockout



The metering Flip–Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip–Flop prevents double pulsing in a push–pull configuration by remembering which output produced the last pulse.

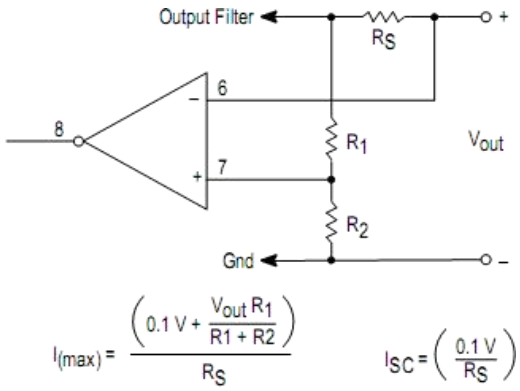
Pulse Processing Logic



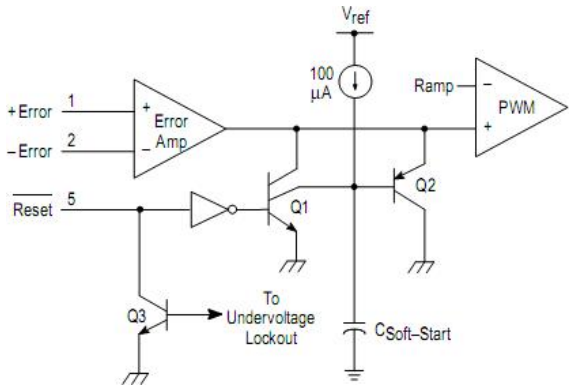
$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right) \qquad V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

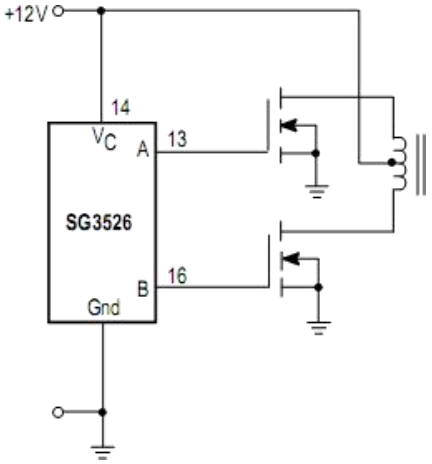
Error Amplifier Connects



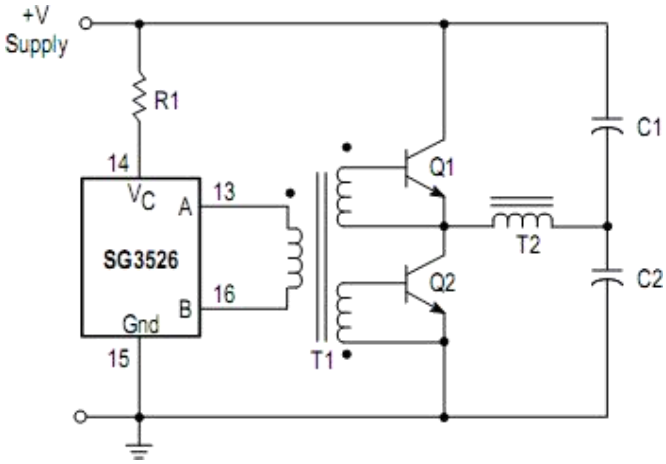
Foldback Current Limiting



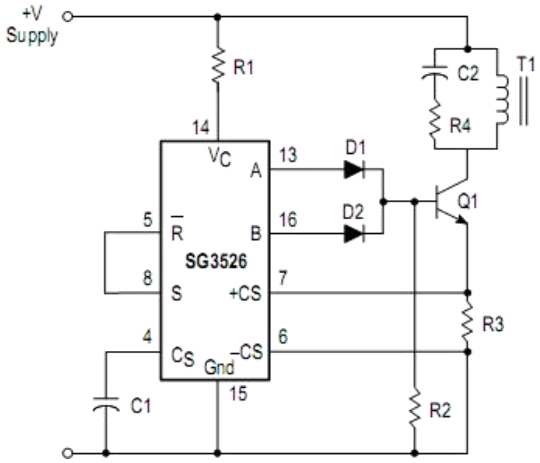
Soft-Start Circuity



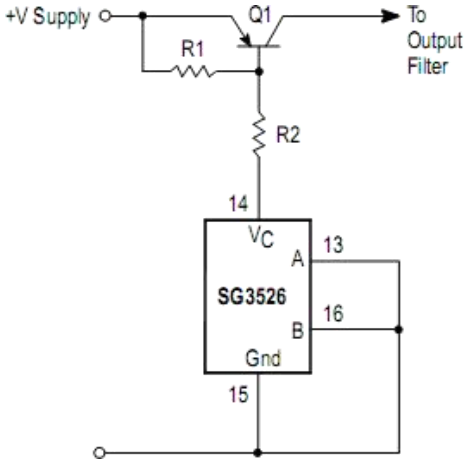
Driving VMOS Power FETs



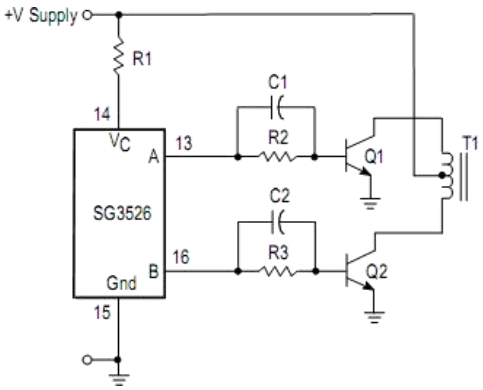
Half-Bridge Configuration



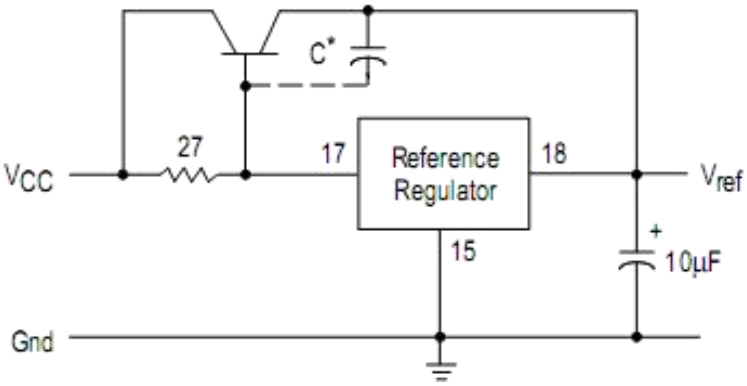
Flyback Converter with Current Limiting



Single-Ended Configuration



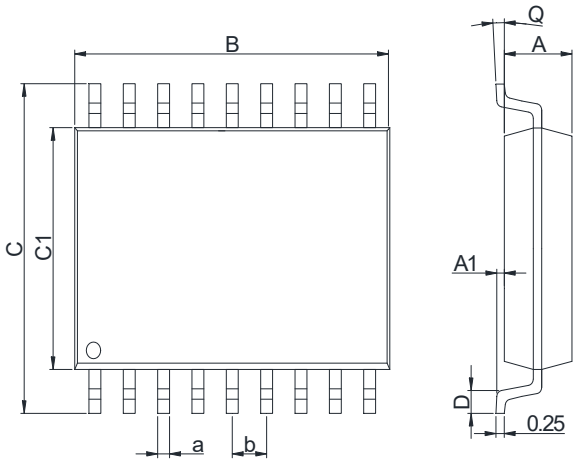
Push-Pull Configuration



Extending Reference Output Current Capability

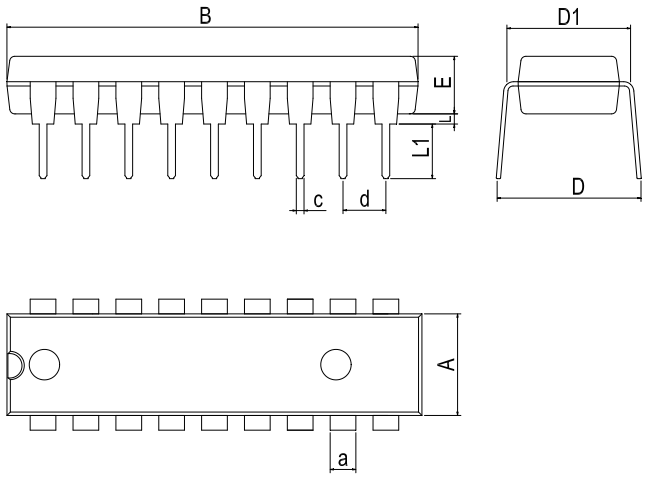
Package Information

SOP18



Dimensions In Millimeters(SOP18L)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.08	11.25	10.10	7.30	0.7	0°	0.35	1.27 BSC
Max:	2.50	0.28	11.65	10.50	7.70	1	8°	0.44	

DIP18



Dimensions In Millimeters(DIP18)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	22.24	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	23.24	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

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