RN8302B USER MANUAL

Date: 2019-08-09
Version: 1.1

CONTENTS

1. Introduction

1.1 Features

- Metering
  - ✓ Less than 0.1% error in total and fundamental active energy over a dynamic range of 5000：1, meet the accuracy requirement for the class 0.5S and 0.2S active electrical energy meter of the national grid.
  - ✓ Less than 0.1% error in total and fundamental reactive energy over a dynamic range of 5000：1.
  - ✓ Total and fundamental apparent energy.
  - ✓ Active and reactive power orientations, four-quadrant reactive judging.
  - ✓ No-load and startup function, adjustable startup threshold.
  - ✓ Adjustable electrical energy meter constant(EC).
  - ✓ Fast pulse count of the active, reactive and apparent powers.
  - ✓ Total and fundamental active, reactive and apparent CF frequency outputs.
- Measurement
  - ✓ Total and fundamental active, reactive and apparent powers.
  - ✓ Three-phase total, fundamental and harmonic Voltage RMS and current RMS.
  - ✓ Total and fundamental power factors.
  - ✓ Less than 0.02% accuracy of voltage line frequence.
  - ✓ Less than 0.02° resolution of fundamental voltage and current phase angle for each phase.
  - ✓ Seven channels zero-crossing detection and settable zero-crossing threshold.
  - ✓ Voltage phase sequence error detection.
  - ✓ Loss of voltage indication and settable loss of voltage threshold.
  - ✓ Flexible voltage and current waveform buffer data.
  - ✓ Voltage sag detection.
  - ✓ Overvoltage and overcurrent detection.
- Anti-tampering
  - ✓ Neutral current measurement.
  - ✓ A low power dissipated mode NVM2 for the current comparison and pre-judging. Settable two levels of threshold and less than 150μA of power dissipated.
  - ✓ A low power mode NVM1 to implement the low power current RMS measurement, and less than 2mA of power dissipated.
  - ✓ Transformer open-circuit and short-circuit detection function at the secondary side.
- Software Calibration
  - ✓ Channel gain calibration of seven ADCs, and compatible with the power calibration method.
  - ✓ Channel phase calibration of seven ADCs, current channel A, B and C support

per-phase calibration.

- ✓ Power gain and phase calibration.
- ✓ Active, reactive and RMS offset calibration.
- ✓ Checksum register to check the calibration data automatically.

- ◆ Compatible with three-phase three-wire system and three-phase four-wire system.
- ◆ 3.3V signle power supply with power monitoring function.
- ◆ On-chip 1.25V ADC reference voltage, typical 20 ppm/℃ of temperature coefficient, connectable reference voltage externally.
- ◆ High speed SPI interface with transmission rate up to 3.5Mbps and write protection function.
- ◆ One interrupt pin.
- ◆ Operating voltage range: 3.0V - 3.6V
- ◆ Operating temperature range: -40℃ - 85℃
- ◆ LQFP44 package is adopted.

1.2 Functional Block Diagram

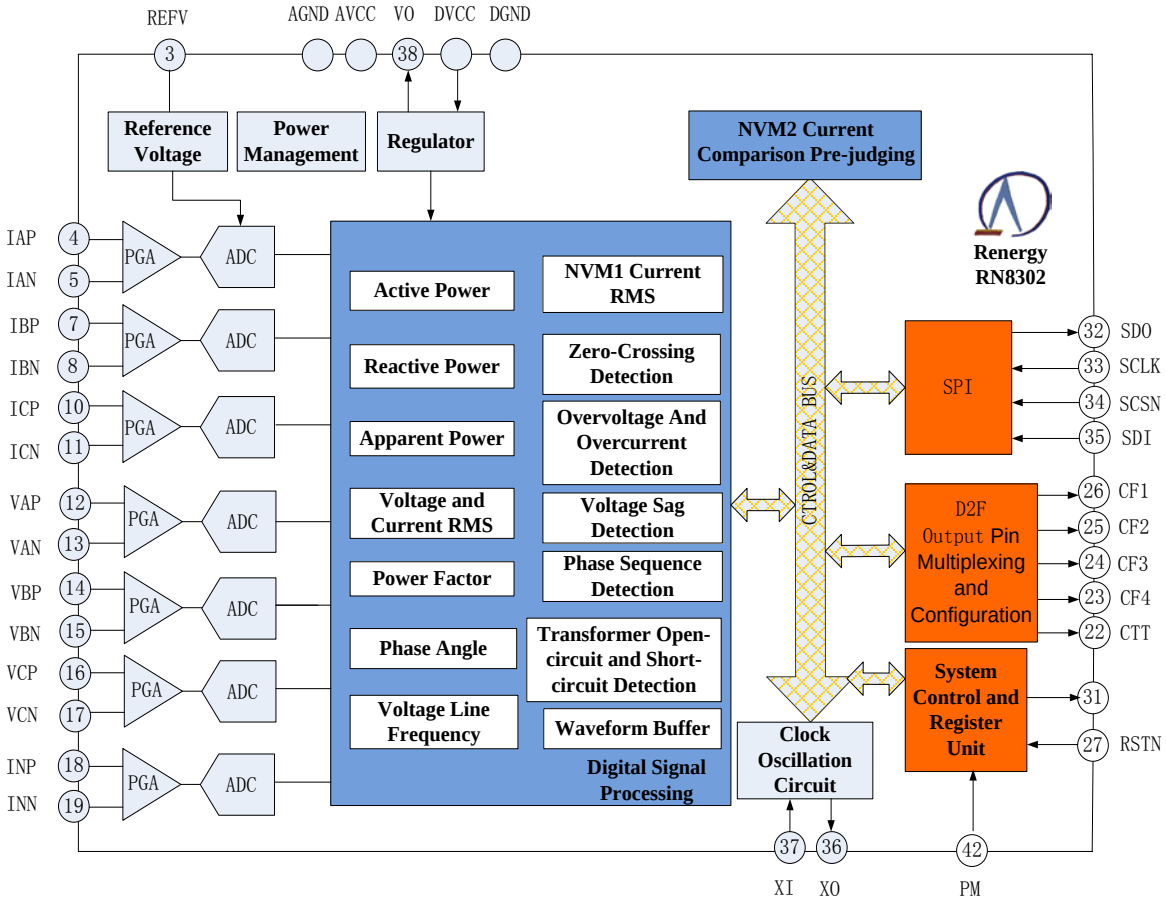


Figure 1-1 System Block Diagram

1.3 Pin Definition

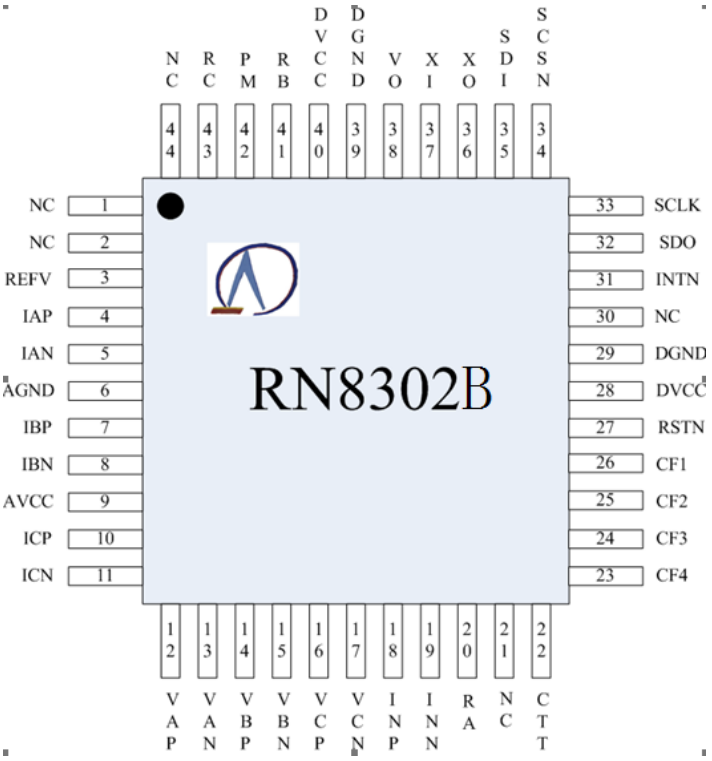


Figure 1-2 Pin Arrangement Diagram

Table 1-1 Description of RN8302B Pin Function

Pin No.	Name	Type	Description
1,2,21,30, 44	NC		Not connected
3	REFV	I/O	Output of the on-chip reference voltage when the register bit REFSEL (ADCCFG.14) = 0. This pin shound be decoupled to AGND with 10μF and 0.1μF capacitor. This pin is the input of the external high accurate reference voltage when the register bit REFSEL (ADCCFG.14) = 1, as the reference voltage of the internal ADC.
4,5	IAP, IAN	I	Positive and negative analog input pins for Phase A Current. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
6	AGND	Power	Analog ground.
7,8	IBP, IBN	I	Positive and negative analog input pins for Phase B Current. These pins are differential inputs, with the

			maximum input Vpp is 800mVpp in normal operation.
9	AVCC	Power	3.3V analog power supply. The operating range is 3.0V-3.6V. This pin shound be decoupled to AGND with 10μF capacitor and 0.1μF capacitor.
10,11	ICP, ICN	I	Positive and negative analog input pins for Phase C Current. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
12,13	VAP, VAN	I	Positive and negative analog input pins for Phase A Voltage. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
14,15	VBP, VBN	I	Positive and negative analog input pins for Phase B Voltage. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
16,17	VCP, VCN	I	Positive and negative analog input pins for Phase C Voltage. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
18,19	INP, INN	I	Positive and negative analog input pins for Neutral Current. These pins are differential inputs, with the maximum input Vpp is 800mVpp in normal operation.
20	RA		Reserved pin. Connect with the analog ground.
22	CTT	O	Used to perform the transformer open-circuit and short-circuit detection function at the secondary side.
23,24,25, 26	CF4, CF3, CF2, CF1	O	Calibration Frequency (CF) Logic Outputs. Can be configured by register CFCFG into any pulse of the all-phase sum output of the fundamental/total and active/reactive/apparent powers or the high frequency pulse of the all-phase sum output.
27	RSTN	I	Reset pin, active low. For the details, refer to **Chapter 2.3**. It is internal floating and shall be connected with the power supply or the 1KΩ pull-up resistor externally.
28,40	DVCC	Power	3.3 digital power supply. The operating range is 3.0V - 3.6V. This pin shound be decoupled to AGND with 10μF and 0.1μF capacitor.
29,39	DGND	Power	Digital ground.

31	INTN	O	Interrupt output pin, active low. High level, by default. When the allowed interrupt event of the interrupt enable register has occurred, the pin level is toggled. When CPU clears corresponding interrupt flag by the SPI interface, the pin resets its high level.
32	SDO	O	SPI serial data output, data is shifted out on the SCLK rising edge. When SCS_N is high, it stays in high impedance.
33	SCLK	I	SPI serial clock input. Serial clock to synchronize the serial interface configuration generated by MCU. The master writes data at the High level of SCLK, and the slave reads the data at the SCLK low level.
34	SCS_N	I	SPI selection signal, active low.
35	SDI	I	SPI serial data input. Data is shifted in on the SCLK falling edge.
36	XO	O	Output terminal of the clock crystal.
37	XI	I	Input terminal of the clock critical or the system clock input of the external clock. The typical frequency of the clock crystal is 8.192MHz. The typical value of the load capacitance is 15pF, and it is necessary to connect with the 10MΩ resistor between this pin and the XO pin.
38	VO	O	On-chip regulator output. This pin shall shunt 10μF capacitor and 0.1μF capacitor to the digital ground for the decoupling. Note that this pin shall not be connected with the external load.
41	RB		Reserved. Shall be connected with DVCC.
42	PM	I	Default operating mode select pin. PM = 1, select sleep mode (SLM). PM = 0, select measurement mode (EMM). This pin is internal floating and shall be pulled up with 1KΩ resistor externally or connected with grounded.
43	RC		Reserved. Shall be connected with digital ground.

1.4 Typical Application

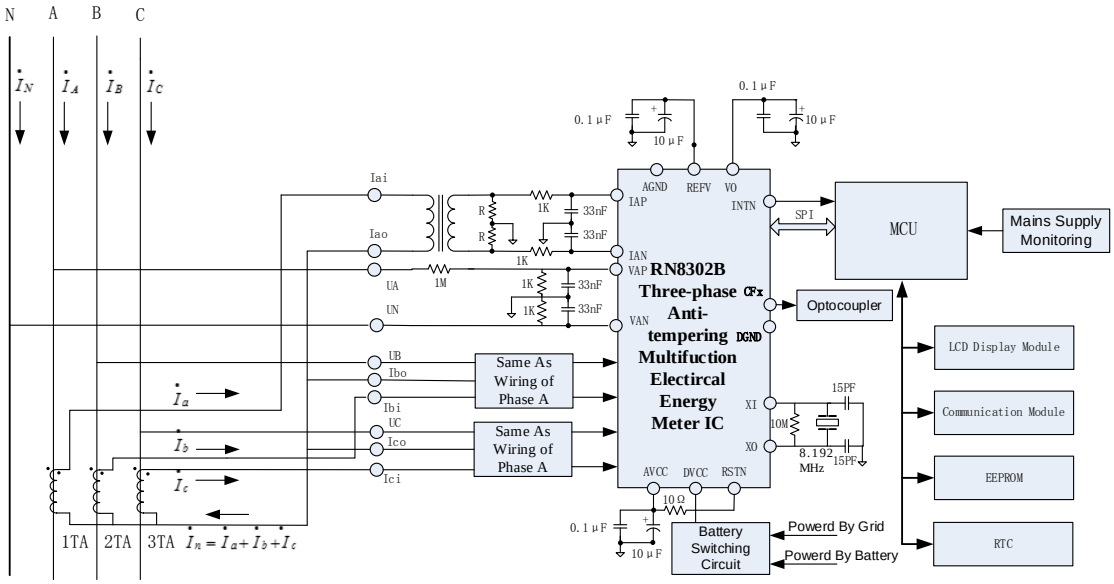


Figure 1-3 Typical Application Circuit Schematic of Three-phase Four-wire Meter

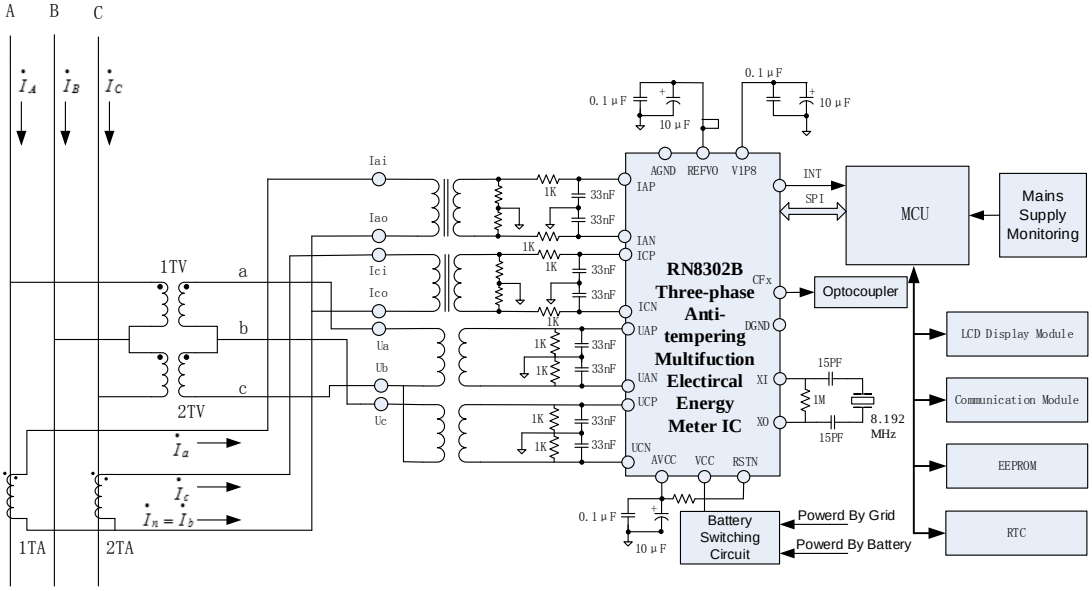


Figure 1-4 Typical Application Circuit Schematic of Three-phase Three-wire Meter

2 System Function

2.1 Power Supply Monitoring

The RN8302B contains an on-chip 3.3V analog power supply monitor supervises the power supply AVCC. When AVCC is lower than 2.70V under the room temperature, the RN8302B is reset globally. When AVCC is higher than 2.82V under the room temperature, the RN8302B operates normally.

2.2 Operating Mode

The RN8302B is equipped with four operating mode, such as the measurement mode (EMM), **no-voltage** mode 1 (NVM1), no-voltage mode 2 (NVM2) and sleep mode (SLM).

- Measurement Mode (EMM): It is used to measure and meter various electrical parameter when the electrical energy meter operates in the power supply mode.
- No-voltage Mode 1 (NVM1): It is used to measure the low power no-voltage current RMS.
- No-voltage Mode 2 (NVM2): It is used to pre-judge the low power no-voltage current.
- Sleep Mode (SLM): It is used in the sleep status when the electrical energy meter is powered by the backup battery after the grid is powered down.

The power dissipated of each modes for RN8302B is shown as follows:

Table 2-1 Power Dissipated in Each Operating Modes

(Room Temperature, AVCC= DVCC=3.3V)

Measuring Items	Symbol	Minimum	Typical	Maximum	Unit	Test Condition
Power Dissipated (EMM)	I_{EMM}		5		mA	fosc=8.192MHz
Power Dissipated (NVM1)	I_{NVM1}		2		mA	fosc=8.192MHz
Power Dissipated (NVM2)	I_{NVM2}		150		μA	
Power Dissipated (SLM)	I_{SLM}		2		μA	

The RN8302B operating mode is switched by the SPI command. For the mode switching command registers and the command words, refer to **Chapter 3.4.32**.

For the effect of the RN8302B mode switching on the register and the change, refer to **Chapter 3.5.4**.The bits of the system status register SYSSR (0x8A) WMS [1:0] indicate current operating mode of RN8302B.

The system default mode can be configured as SLM or EMM by the PM pin after RN8302B is power-on reset. Refer to **Chapter 1.4**.The bit of the system status register SYSSR (0x8A) PM indicates current operating mode of RN8302B.

For the details on the SYSSR (0x8A) register, refer to **Chapter 3.4.36**.

2.3 System Reset

RN8302B supports the following reset mode:

- Power-up and power-down reset
- External pin reset
- Software reset
- Wake-up reset

The power-up and power-down reset is the global reset, and other reset modes are the local reset. Upon completion of the reset, the reset flag bit of the system status register SYSR (B1 0x8A) changes. For the concrete description of the reset flag bit, refer to **Chapter 3.4.36** Register.

1. Power-up and Power-down Reset

After the power-up and power-down reset has occurred, the system is reset to the default mode SLM or EMM that is configured by the PM pin. The register is reset to the initial value in the default operating mode. The external pin level is reset to the initial state. For the details on the power-up and power-down reset register, refer to **Chapter 3.5.1**.

2. External Pin Reset

When the system is in the SLM mode, the external pin reset is invalid. When the system is in the EMM, NVM1 and NVM2 mode, the external pin reset is valid. After the external pin reset has occurred, the current operating mode of the system is constant, and only part of registers are reset to the initial value in this operating mode. For the details on the external pin reset register, refer to **Chapter 3.5.2**.

3. Software Reset

For the details on the software reset command registers, refer to **Chapter 3.4.33**.When the system is in the SLM mode, the software reset is invalid. When the system is in the EMM, NVM1 and NVM2 mode, the software reset is valid. After the software reset has occurred, the current operating mode of the system is constant, and only part of registers are reset to the initial value in this operating mode. For the details on the external pin reset to register, refer to **Chapter 3.5.3**.

4. Wake-up Reset

When SLM or NVM2 is switched to EMM or NVM1, the wake-up reset takes place. After the reset has occurred for 1.5ms, the register is reset to the initial value of the wake-up reset. For the details on the wake-up reset register, refer to **Chapter 3.5.4**.

2.4 Measurement Mode

The measurement mode (EMM) is used to measure and meter various electrical parameters when the electrical energy meter operates in the power supply mode.

2.4.1 Sampling Channel

The RN8302B sampling channel includes seven ADCs and the sampling data processing circuit.

Three of seven ADCs are used for phase current sampling, one of them is used for the neutral current sampling, and three of them are used for the voltage sampling. ADC takes the fully differential mode input,with the maximum input amplitude vpp is 800mVpp.

Configure PGA to amplify seven ADCs for 1/2/4/8 times respectively, and select whether the ADC reference voltage comes from the on-chip reference voltage or the external reference voltage. For the instruction for use of the ADCCFG register, refer to **Chapter 3.4.34**.

Carry out the channel phase calibration of seven ADCs by configuring the PHS register (B1 0x0C-0x12). For the instruction for use of the PHS register, refer to **Chapter 3.4.7** and **Chapter 4 Calibration**. Of which, the register PRTHx (B10x06-0x09) is set to implement the per-phase calibration of three current channels. For the details on the PRTHx register, refer to **Chapter 3.4.5**.

Carry out the channel gain calibration of seven ADCs by configuring the GS register (B1 0x13-0x19). For the instruction for use of the GS register, refer to **Chapter 3.4.8** and **Chapter 4 Calibration**.

Configure the high-pass filter enable and disable of seven sampling channels by configuring the HPFOFF [6:0] register in the EMUCFG register (B1 0x61).For the details on HPFOFF [6:0], refer to **Chapter 3.4.17 Register**.

Carry out the DC OFFSET calibration of seven ADCs by configuring DC_OS register (B1 0x1A - 0x20). For the details on the DC_OS register, refer to **Chapter 3.4.9**.

The real-time sampling data of seven ADCs for RN8302B is output to the waveform sampling register (B0 0x00-0x06). For the details on the waveform sampling register, refer to **Chapter 3.2.1**.

2.4.2 Sampled Waveform Buffer

In addition to In, six 24bits ADC sample data can be stored to the on-chip waveform storage cell, to carry out the FFT analysis.

1. Buffer Area Capacity

There are 768 address units in the buffer area, which can store the data of 128 points for six ADCs in one cycle, such as UA, UB, UC, IA, IB and IC.

2. Address Mapping

1) Byte Length: There are three bytes for one address unit, which is used to store one sampling data of ADC.

2) Address Mapping: 768 address units with the address 200H-4FFH.

3. Sampling Rate and Buffer Control

The waveform sampling rate can be configured by writing buffer control register WSAVECON (B1 0x63) under the condition of fosc = 8.192 Mhz. For 50Hz application, the waveform sampling rate is 6.4 KHz. For 60Hz application, the waveform sampling rate 7.699 KHz.

Whether the ADC data of each channels is written into the buffer and the arrangement mode in the buffer, the buffer size of each channels, enable/disable buffer and buffer status after the buffer is enabled are controlled by writing buffer control register WSAVECON (B1 0x63). For the details, refer to **Chapter 3.4.19**.

4. SPI BURST Read Operation of Buffer

Users can read the buffer data by SPI. For the details on the read operation of the buffer SPI, refer to **Chapter 5 Communication Interface**.

When SPI reads the waveform buffer successfully for one time, the data buffer addresses read for the last time are stored in the waveform buffer address register LRBufAddr (B1 0x8E). For the details on the LRBufAddr register, refer to **Chapter 3.4.40**.

5. Operating Mode and Waveform Buffer:

The waveform buffer in SLM, NVM2 and NVM1 is invalid. The waveform buffer RAM value is uncertain in the EMM mode after the power-up reset or the wake-up reset, write the value after write buffer or clear command. For the software reset and the hardware pin reset, the waveform buffer RAM value is constant.

2.4.3 Active Power

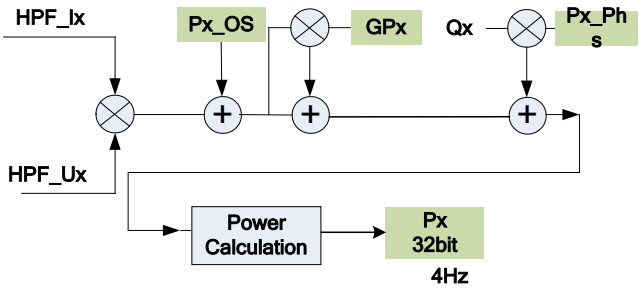


Figure 2-1 Per-Phase Active Power

1. Per-phase Active Power

For the details on the per-phase active power Px (x = A, B, C, the same below) register, refer to **Chapter 3.2.3**.

As shown in the figure below, carry out the active power gain calibration by the register in the per-phase active power channel. For the details on the GPx register, refer to **Chapter 3.4.11**.

Carry out the active power phase calibration by the Px_PHS register in the per-phase active power channel. For the details on the Px_PHS register, refer to **Chapter 3.4.12**.

Carry out the active power Offset calibration by the Px_OS register in the per-phase active power channel. For the details on the Px_OS register, refer to **Chapter 3.4.13**.

2. All-phase sum Active Power

The average value of the all-phase sum active power register P_T (B0 0x17) is the algebraic sum of the average active power for each per-phase. For the details on the P_T register, refer to **Chapter 3.2.3**.

P_T can be configured into the three-phase four-wire algorithm and the three-phase three-wire algorithm by selecting the register MODSEL (B1 0x86) in the three-phase four-wire and three-phase three-wire mode.

For the details on the MODSEL register, refer to **Chapter 3.4.35**.

If it is configured into the three-phase four-wire system, $P_T = P_A + P_B + P_C$.

If it is configured into the three-phase three-wire system, the power of phase B is not calculated, so $P_T = P_A + P_C$.

3. Fundamental Active Power

There is a set of the active power parameters and calibration registers which correspond to the total active power, and the fundamental power shares the MODSEL register with the total. For the details on the fundamental active power and calibration register, refer to Chapter **3.2.3**, **3.4.11** - **3.4.13**. The fundamental filter can attenuate the harmonic power with the frequency 120Hz or higher.

4. Active Power Direction

The total and fundamental active power orientation of the per-phase and all-phase sum is provided by the power orientationregister PQSign (0x66). For the details on the PQSign register, refer to **Chapter 3.4.21**. The PSIGNCfg [2:0] register in the **EMUCFG register** (B1 0x61) performs the sign reverse selection function of the PC/PB/PA/FPC/FPB/FPA active power.

2.4.3 Reactive Power

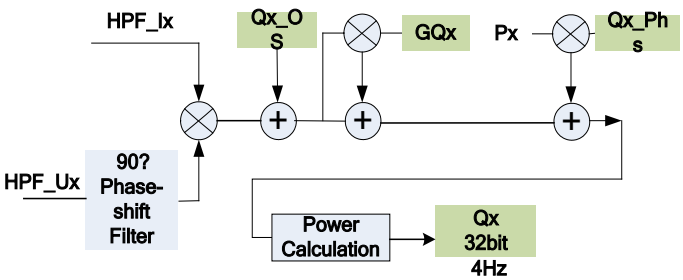


Figure 2-2 Per-Phase Reactive Power

The RN8302B provides the total and fundamental per-phase reactive power and all-phase sum reactive power and provides the sign bit of the per-phase and the all-phase sum reactive power for the four quadrants judging. Furthermore, it provides the reactive power gain calibration, phase calibration and Offset calibration register.

For the details on the reactive power and the calibration register, refer to **Chapter 3.2.2**, **3.4.11** - **3.4.13**. For the details on the power orientation register PQSign, refer to **Chapter 3.4.21**. The QSIGNCfg [2:0] register in the **EMUCFG register** (B1 0x61) performs the sign

reverse selection function of the QC/QB/QA/FQC/FQB/FQA reactive power.

The all-phase sum reactive power can be configured into the three-phase four-wire mode and the three-phase three-wire mode by the MODSEL register.

The RN8302B reactive 90°phase shift Hilbert algorithm ensures it can provide excellent phase shift characteristic and amplitude-frequency response characteristic within the 0 – 51 harmonic range.

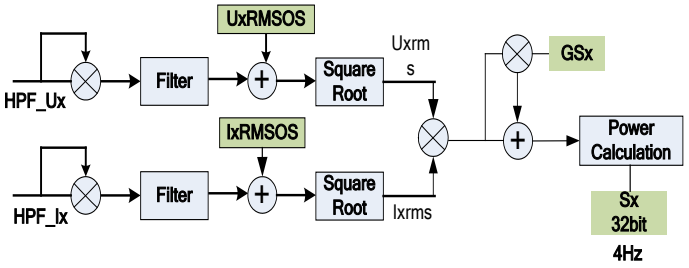


Figure 2-3 Split Phase Apparent Power

2.4.5 Apparent Power

The RN8302B provides the total and fundamental apparent power of the per-phase and all-phase sum. Furthermore, it also provides the gain calibration register of the apparent power.

For the details on the apparent power register, refer to **Chapter 3.2.3**. For the details on the power gain calibration register, refer to **Chapter 3.4.11**.

The per-phase apparent power takes the RMS method, namely, $Sx = Uxrms * Ixrms$. Where, Uxrms and Ixrms indicate the RMS value of phase x respectively. The all-phase sum apparent power can be configured into the three-phase four-wire mode and the three-phase three-wire mode by the MODSEL register.

2.4.6 Energy Output

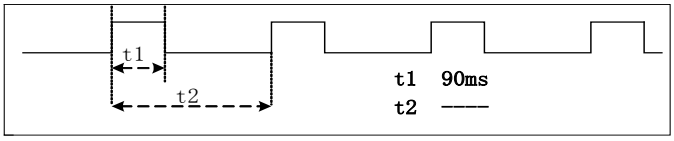
The RN8302B provides three energy output modes, such as the energy register, CF frequency output and fast pulse count Fcnt.

1. Energy Register:

The RN8302B provides several types of the energy registers, including the total/fundamental active/reactive/apparent, per-phase/all-phase sum and forward/reverse energy register. For the details, refer to **Chapter 3.2.6 Energy Register**.

2. Energy Pulse Output:

The all-phase sum pulse output, namely the Calibration Frequency output, can be connected with the standard electrical energy meter for the error comparison directly.The RN8302B provides four CF pins. For the definition of the CF pin, refer to **Chapter 1.4**.



Each CF output meets the following timing.

Note: When the pulse output period is less than 180ms, the

pulse is output in the equal duty cycle way.

CF1 is the all-phase sum CF frequency output of the total active power, CF2 is the all-phase sum CF frequency output of the total reactive power, CF3 is the all-phase sum CF frequency output of the total apparent power, and CF4 is the all-phase sum CF frequency output of the fundamental active power. Each CF pin can be configured into the any all-phase sum pulse output of the total active all-phase sum, total reactive, total apparent, total active, fundamental reactive and fundamental apparent power flexibly by the CFCFG register (0x60) by default.

Each CF pin outputs the pulse by taking HFCONST1 as the high-frequency pulse constant, to synchronize the update of corresponding all-phase sum energy register by default. Each CF pin can take HFCONST2 as the high-frequency pulse constant to output the pulse by configuring the CFCFG register (0x60). At this time, if HFCONST1 is not equal to HFCONST2, the CF pulse output doesn't synchronize with corresponding all-phase sum energy register update. This function can be used for measuring the maximum demand pulse.

For the CFCFG register, refer to **Chapter 3.4.16**.The MODSEL register is the three-phase four-wire mode by default.

Accordingly, the all-phase sum pulse output of each CF pin is also the three-phase four-wire mode. The MODSEL register is the three-phase four-wire mode by default. Accordingly, the all-phase sum pulse output of each CF pin is also the three-phase four-wire mode.

When the MODSEL register is the three-phase four-wire mode, configure the active all-phase sum energy cumulative mode in algebraic sum or absolute value sum mode by configuring the EPADDMOD register bit (EMUCFG.20). Accordingly, the all-phase sum pulse output cumulative mode of the active CF pin is also configured by the bit of the EPADDMOD register.

When the MODSEL register is the three-phase four-wire mode, configure the reactive all-phase sum energy cumulative in algebraic sum or absolute value sum mode by configuring the EPADDMOD register bit (EMUCFG.21). Accordingly, the all-phase sum pulse output cumulative mode of the reactive CF pin is also configured by the bit of the EPADDMOD register.

For the details on the EMUCFG register (B1 0x61), refer to **Chapter 3.4.17**.

If users require the per-phase pulse output during the calibration, configure which phases implement the all-phase sum operation by configuring the measurement control register EMUCON (B1 0x60). If users require CF1 outputs the active CF frequency of phase A only, configure PRUN0=1, PRUN1=0 and PRUN2=0 in EMUCON, phase B and C don't implement the all-phase sum operation, and the CF1 output pulse represents the active CF frequency of phase A.

For the details on the EMUCON register (B1 0x60), refer to **Chapter 3.4.18**.

3. Fast Pulse Count Register:

The fast pulse count register includes the total/fundamental active/reactive/apparent and per-phase/all-phase sum fast pulse count register. For the details, refer to **Chapter**

3.2.5.

2.4.7 Voltage RMS and Current RMS

1. Total Voltage RMS and Current RMS

The total Voltage RMS includes the three-phase Voltage RMS UA, UB and UC. The total current RMS includes the three-phase current RMS IA, IB, IC and the neutral current RMS IN.

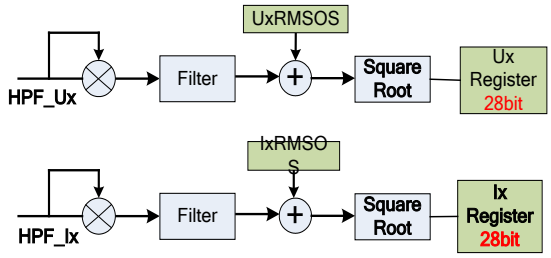


Figure 2-4 Voltage and Current RMS

Calibration of Voltage RMS and current RMS: ① Calibrate the gain by the channel gain register.② RMS OFFSET calibration. For the details, refer to **Chapter 3.4.8** and **3.4.10 Register** and **Chapter 4 Calibration**.

2. Fundamental Voltage RMS and Current RMS

The fundamental Voltage RMS includes the three-phase fundamental Voltage RMS FUA, FUB and FUC, and the fundamental current RMS includes the three-phase current RMS FIA, FIB and FIC.

In addition to output as the parameters, FUA, FUB and FUC are also taken as the criterion for the voltage zero-crossing detection, voltage line frequency measurement and phase angle threshold detection. In addition to output as the parameters, the current RMS FIA, FIB and FIC are also taken as the criterion for the startup of each fundamental phases, current zero-crossing detection and current phase angle threshold detection.

Calibration of Fundamental Voltage RMS and current RMS: ① Calibrate the gain by the channel gain register.② Fundamental RMS OFFSET calibration. For the details, refer to **Chapter 3.4.8** and **3.4.10 Register** and **Chapter 4 Calibration**.

3. Harmonic Voltage RMS and Current RMS

The harmonic Voltage RMS includes the three-phase fundamental Voltage RMS HUA, HUB and HUC, and the harmonic current RMS includes the three-phase current RMS HIA, HIB and HIC.

The harmonic RMS can be used to calculate the harmonic content of voltage and current channel. The relationship among the harmonic Voltage RMS, total Voltage RMS and current RMS and fundamental Voltage RMS and current RMS is shown as follows:

$$HU_X = \sqrt{U_X{}^2 - FU_X{}^2}\ ;\quad HI_X = \sqrt{I_X{}^2 - FI_X{}^2}$$

4. Voltage Vector sum Voltage RMS

It is defined as follows:

$$U_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (u_A(t) + u_B(t) + u_C(t))^2 dt}$$

Where, $u_A(t)$, $u_B(t)$ and $u_C(t)$ are the sampling value of each voltage channel ADCs.

5. Current Vector sum Current RMS

There are two algorithms for the current vector sum current RMS, taking the three-phase four-wire system with the neutral current transformer and without the neutral current transformer into account.

Algorithm 1: $I_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (i_A(t) + i_B(t) + i_C(t))^2 dt}$

Algorithm 2: $I_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (i_A(t) + i_B(t) + i_C(t) - i_N(t))^2 dt}$

Where, $i_A(t)$, $i_B(t)$, $i_C(t)$ and $i_N(t)$ are the sampling value of various current channel ADCs.

Which algorithm is taken is depended by the ISUMMOD bit in the measurement unit configuration register EMUCFG (B1 0x61).If ISUMMOD=0, take the algorithm 1. If ISUMMOD=1, take the algorithm 2.For the details on the ISUMMOD bit, refer to **Chapter 3.4.17**.

The update cycle for above RMS data is 250ms.For the details on the RMS register, refer to **Chapter 3.2.2**.

2.4.8 Startup and No-load Setting

The RN8302B takes current RMS as the criterion of the total active, reactive and apparent no-load and startup, and fundamental active, reactive and apparent no-load and startup.

For the total active, reactive and apparent no-load and startup function, the RN8302B provides the total current RMS- and fundamental current RMS-based criterion. Which criterion is taken is depended by the NoloadCFG bit in the measurement unit configuration register EMUCFG (B1 0x61).For the details on NoloadCFG, refer to **Chapter 3.4.17** Register.

For the fundamental active, reactive and apparent no-load and startup function, the RN8302B provides the fundamental current RMS-based criterion.

The RN8302B provides two startup current threshold registers. The total and fundamental active and apparent share one startup current threshold register IStart_PS (B1 0x02), and the total and fundamental reactive share one startup current threshold register IStart_Q (B1 0x03).For the details, refer to **Chapter 3.4.2 Startup Current Threshold Register**.

The RN8302B provides the no-load and startup judge result register Noload (B1 0x67),

to indicate the total active and apparent/total reactive/fundamental active and apparent/ fundamental reactive/fundamental apparent no-load status of each per-phase. For the details, refer to **Chapter 3.4.22 No-load Status Register**.

If the active, reactive or apparent energy of some phase are in the no-load staus, this phase stops measuring, the FCnt of this phase stops increasing, and the energy register of this phase stops increasing. Furthermore, this phase doesn't carry out the all-phase sum operation.

2.4.9 Power Factor

The power factor register of RN8302B includes the total power factor PfA/PfB/PfC/PfT of the per-phase and all-phase sum, and the fundamental power factor FPfA/FPfB/FPfC/FPfT of the per-phase and all-phase sum.

Total Per-phase Power Factor: $PFx = \frac{P_X}{S_X}$. Where, x＝a, b, c. Sx indicates the apparent power of each per-phase, and Px indicates the active power of each per-phase, which is the signed value.

Total All-phase sum Power Factor: $PF_T = \frac{P_T}{S_T}$. Where, x＝a, b, c. ST indicates the apparent power of each all-phase sum, and PT indicates the active power of each all-phase sum, which is the signed value.

The fundamental power factor is calculated by the fundamental active and fundamental apparent power parameters, and the calculation method is the same as that of the total.

For the details on the power factor register, refer to **Chapter 3.2.4**.

2.4.10 Phase Angle

The RN8302B performs the function of phase angle measurement among seven fundamental energys. For the description and usage of seven phase angle registers YUA, YUB, YUC, YIA, YIB, YIC and YIN, refer to **Chapter 3.2.7**.

For the rated input (Un=220mV, Ib=50mV), the phase angle resolution of RN8302B is less than 0.02°.

2.4.11 Voltage Line Frequency

The RN8302B performs the function of the voltage line frequency measurement. For the details on the voltage line frequency register UFeq (B0 0x57), refer to **Chapter 3.2.8** Register. The resolution of the voltage line frequency is up to 0.0001Hz, and the measuring accuracy is up to 0.02%.

2.4.12 Zero-crossing Detection

The RN8302B performs the forward zero-crossing function of the voltage and current waveform for seven fundamental energyss.

The RN8302B provides the voltage and current zero-crossing threshold register ZXOT (B1 0x05). If this fundamental Voltage RMS and current RMS is less than the ZXOT threshold, this zero-crossing current is not output. For the details on the ZXOT register, refer to **Chapter 3.4.4**.

The RN8302B provides seven zero-crossing interrupt outputs to the INT pin. For the details on the zero-crossing interrupt enable and flag register, refer to **Chapter 3.4.20** and **2.6 Interrupt**.

2.4.13 Loss of Voltage Detection

The RN8302B provides the loss of voltage threshold register LostVoltage (0x04) and the loss of voltage state flag bit LostVoltSA, LostVoltSB and LostVoltSC (B1 0x69.0-2) of each phase for the loss of voltage detection.

The loss of voltage threshold register LostVoltage (B1 0x04) is used to set the loss of voltage threshold of RN8302B.For the details, refer to **Chapter 3.4.3** Register.

The loss of voltage state flag bit LostVoltSA, LostVoltSB and LostVoltSC indicate the loss of voltage judgment result of each phase. For the details on the criterion and flag bit, refer to **Chapter 3.4.24**.

2.4.14 Voltage Phase Sequence Detection

The RN8302B performs the function of the voltage phase sequence error detection, and the voltage phase sequence error flag bit UPhSqErr (B1 0x69.3) indicates the detection result. For the details on the voltage phase sequence error criterion and the flag bit UPhSqErr, refer to **Chapter 3.4.24**.

2.4.15 Voltage Sag Detection

The RN8302B performs the function of the three-phase input voltage UA, UB and UC voltage sag detection.

Criterion of Voltage Sag Detection for Some Phase: If the high 16-bit of the peak absolute value for the voltage fundamental sample value of this phase is less than SAGLVL [15:0] and the duration is SAGCYC [7:0] half cycles, it is judged as this phase voltage is sag. Of which, SAGLVL [15:0] is the low 16-bit of the voltage sag threshold register SAGCFG (B1 0x58), and SAGCYC [7:0] is the high 8-bit of SAGCFG (B1 0x58).For the details on the SAGCFG register, refer to **Chapter 3.4.14**.

The voltage sag of some phase will cause the bit of the SAGUx (x=A, B, C) register for this phase in the PHASES register (B1 0x69) is set to 1, and the bit of the SAGIF register in the EMMIF register (B1 0x64) is set to 1. If SAGIE=1 in the EMMIE (B1 0x65) register, setting SAGIF to 1 will interrupt INT. It will clear this interrupt when clear SAGIF. At the same time, it will clear the SAGUx flag in the PHASES register.

For the details on the PHASES register, refer to **Chapter 3.4.24**.For the details on the bit of the SAGIE register and the bit of the SAGIF register, refer to **Chapter 3.4.20** and **2.6 Interrupt**.

2.4.16 Overvoltage and Overcurrent Detection

The RN8302B performs the overvoltage and overcurrent judging function of the three-phase input voltage and current.

Criterion of OverVoltage for Some Phase: When the high 16-bit of the absolute value for the voltage sample value of some phase is greater than the overvoltage threshold register OVLVL (0x59), it judges the voltage of this phase is overvoltage. For the details on the OVLVL register, refer to **Chapter 3.4.15**.

The overvoltage of some phase will cause the bit of the OVUx (x=A, B, C) register for this phase in the PHASES register (B1 0x69) is set to 1, and the bit of the OVIIF register in the EMMIF register is set to 1. If OVIIE=1 in the EMMIE register, setting OVIIF to 1 will cause the interrupt. It will clear this interrupt when clear OVIIF. At the same time, it will clear the OVUx flag in the PHASES register.

Criterion of OverCurrent for Some Phase: When the high 16-bit of the absolute value for the current sample value of some phase is greater than the overcurrent threshold register OILVL (0x60), it judges the current of this phase is overcurrent. For the details on the OVLIL register, refer to **Chapter 3.4.15**.

The overcurrent of some phase will cause the bit of the OVIx (x=A, B, C) register for this phase in the PHASES register (B1 0x69) is set to 1, and the bit of the OVIIF register in the EMMIF register is set to 1. If OVIIE=1 in the EMMIE register, setting OVIIF to 1 will cause the interrupt. It will clear this interrupt when clear OVIIF. At the same time, it will clear the OVIx flag in the PHASES register.

For the details on the PHASES register, refer to **Chapter 3.4.24**.For the details on the bit of the OVIIE register and the bit of the OVIIF register, refer to **Chapter 3.4.20** and **2.6 Interrupt**.

2.4.17 Transformer Open-circuit and Short-circuit Detection at Secondary Side

The RN8302B supports the proprietary Renergy transformer open-circuit and short-circuit detection function at the secondary side. For the details, refer to the application note **RN8302B Transformer Open-circuit and Short-circuit Detection Function at Secondary Side**.

2.5 Low Power Mode

The RN8302B provides the no-voltage mode 1 (NVM1) to measure the low power current RMS and the no-voltage mode 2 (NVM2) to pre-judge the low power no-voltage current, and judges the no-voltage accurately by current RMS. Furthermore, it will Supplies sleep mode (SLM), which is used in the sleep status when the electrical energy meter is powered by the backup battery after the grid is powered down.

Users can combine with NVM1, NVM2 and SLM, to complete each phase currents judgment and the current RMS measurement of the **no-voltage**. For the details, refer to the application note RN8302B No-voltage Measurement Function.

2.5.1 No-voltage Mode 1

The no-voltage mode 1 (NVM1) is used to measure the low power current RMS and judge the no-voltage accurately by current RMS.

The RN8302B includes the three-phase current RMS measurement unit under the NVM1 mode, and the result is output to the three-phase current RMS register IA_NVM1, IB_NVM1 and IC_NVM1 under the NVM1 mode. For the details on the register, refer to **Chapter 3.2.2**.

The error over the 400:1 range of the current RMS in the NVM1 mode is less than 0.5%.

This chip writes the GONVM1 command into the operating mode switching register (0x81) in the Write Enable condition in other operating modes, and the RN8302B is switched to NVM1 automatically and starts to calculate current RMS. The update cycle of the current RMS register in the NVM1 mode is 125ms. The current RMS register value is stable within 1.6s after the switching, and then users can read the current RMS register to judge the no-voltage.

The NVM1CFG register (0x70) configures the Interrupt Enable closure in the NVM1 mode. The NVM1IF register (0x71) NVM1Done is set after the switching. If NVM1IE=1, it will cause the interrupt. For the details on the NVM1CFG register, refer to **Chapter 3.4.26**.For the details on the NVM1IF register, refer to **Chapter 3.4.27**.

2.5.2 No-voltage Mode 2

The no-voltage mode 2 (NVM2) is used to pre-judge the low power no-voltage current.

The RN8302B includes the three-phase current comparison unit in the NVM2 mode, to compare the three-phase input current and the comparison unit threshold. Two levels of the comparison unit threshold are optional and can be configured by the bit of the NVM2TH [1:0] register in the NVM2CFG register (0x72).

The RN8302B can configure the current comparison cycle in the NVM2 mode by the bit

of the NVM2TNUM[4:0] register in the NVM2CFG register (0x72).

RN8302B can configure the interrupt enable closure in the NVM2 mode by the bit of the NVM2IE register in the NVM2CFG register (0x72).For the details on the NVM2CFG register, refer to **Chapter 3.4.28**.

Three registers NVM2CMP A/B/C (0x73-75) are used to output and process three comparators in the NVM2 mode. It shall be initialized as 0x0000 during the normal use. For the details on the register, refer to **Chapter 3.4.29**.

After RN8302B configures above register in other operating modes (such as SLM, EMM and NVM1), write the GONVM2 command into the operating mode switching register (0x81) in the Write Enable condition. The RN8302B is switched to NVM2 automatically and enables the comparison of the three-phase input current for one time by the **NVM2CFG register** configuration. The comparison result is stored in the NVM2IF register (0x76) after NVM2TNUM [4:0] + 1 cycles. If NVM2IE=1, the bit of the NVM2Done (NVM2IF.0) register is set upon completion of the comparison of the three-phase input current and causes the interrupt. For the details on the NVM2IF register, refer to **Chapter 3.4.30** and **2.6**.

2.5.3 Sleep Mode

The SPI and AVCC power supply monitoring operate only in the sleep mode, and users can read and write **NVM1, NVM2 and System Configuration and Status Register** by SPI.

When the external pin PM is configured to 1 and power-up reset, the system is in the SLM mode.

After the GOEMM, GONVM1 and GONVM2 command are written into the **Operating Mode Switching Register** (0x81) in the SLM mode in the Write Enable condition, The RN8302B is switched to EMM, NVM1 and NVM2 automatically.

After the GOSLM command are written into the **Operating Mode Switching Register** (0x81) in other operating modes in the Write Enable condition, switch to SLM automatically.

2.6 Interrupt

The RN8302B interrupt is summarized as shown in the table below.

Table 2-6-1: Interrupt in EMM Mode of RN8302B

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
15	Overvoltage and Overcurrent Interrupt	When any phase of the three-phase voltage is overvoltage or any phase of the three-phase current is overcurrent, OVIIF is set to 1.If OVIE = 1, it will cause the INTN pin is toggled from high to low. OVIIF writes 1 and clears 0, and clears the interrupt and the OVUA, OVUB,	OVIIE	OVIIF

		OVUC, OIIA, OIIB and OIIC status flag bits in the PHASES status register.		
14	Voltage Sag Interrupt	When any phase of the three-phase voltage sags, SAGIF is set to 1.If SAGIE = 1, it will cause the INTN pin is toggled from high to low. SAGIF writes 1 and clears 0, and clears the interrupt and the SAGUA, SAGUB and SAGUC status flag bits in the PHASES status register.	SAGIE	SAGIF
13	Status Change Interrupt of Current Segment 3	When any phase of current RMS for three phases A/B/C changes compared to the piecewise status set by IRegion3H/IRegion3L, IRegion3IF is set to 1. Query the Regions register further, to confirm which piecewise status of the current RMS changes. If IRegion3IE = 1, it will cause the INTN pin is toggled from high to low.IRegion3IF writes 1 and clears 0, and clears the interrupt at the same time.	IRegion3IE	IRegion3IF
11	CF4 Pulse Output Interrupt	CF4 outputs the pulse, and the output changes into the high level from the low level. CF4IF is set to 1.If CF4IE = 1, it will cause the INTN pin is toggled from high level to low level. CF4IF writes 1 and clears 0.It clears 0 and clears interrupt simultaneously.	CF4IE	CF4IF
10	CF3 Pulse Output Interrupt	CF3 outputs the pulse, and the output changes into the high level from the low level. CF3IF is set to 1.If CF3IE = 1, it will cause the INTN pin is toggled from high level to low level. CF3IF writes 1 and clears 0.It clears 0 and clears interrupt simultaneously.	CF3IE	CF3IF
9	CF2 Pulse Output Interrupt	CF2 outputs the pulse, and the output changes into the high level from the low level. CF2IF is set to 1.If C2IE = 1, it will cause the INTN pin is toggled from high level to low level.	CF2IE	CF2IF

		CF2IF writes 1 and clears 0.It clears 0 and clears interrupt simultaneously.		
8	CF1 Pulse Output Interrupt	CF1 outputs the pulse, and the output changes into the high level from the low level. CF1IF is set to 1.If C1IE = 1, it will cause the INTN pin is toggled from high level to low level. CF1IF writes 1 and clears 0.It clears 0 and clears interrupt simultaneously.	CF1IE	CF1IF
7	IN Forward Zero-crossing Interrupt	When IN > ZXOT and IN is forward zero-crossing, ZXINIF is set to 1.If ZXINIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXINI writes 1, clears 0 and clears interrupt simultaneously.	ZXINIE	ZXINIF
6	IC Forward Zero-crossing Interrupt	When IC > ZXOT and IC is forward zero-crossing, ZXICIF is set to 1.If ZXICIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXICIF writes 1, clears 0 and clears interrupt simultaneously.	ZXICIE	ZXICIF
5	IB Forward Zero-crossing Interrupt	When IB > ZXOT and IB is forward zero-crossing, ZXIBIF is set to 1.If ZXIBIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXIBIF writes 1, clears 0 and clears interrupt simultaneously.	ZXIBIE	ZXIBIF
4	IA Forward Zero-crossing Interrupt	When IA > ZXOT and IA is forward zero-crossing, ZXIAIF is set to 1.If ZXIAIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXIAIF writes 1, clears 0 and clears interrupt simultaneously.	ZXIAIE	ZXIAIF
3	UC Forward Zero-crossing Interrupt	When UC > ZXOT and UC is forward zero-crossing, ZXUCIF is set to 1.If ZXUCIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXUCIF writes 1, clears 0 and clears interrupt simultaneously.	ZXUCIE	ZXUCIF
2	UB Forward Zero-crossing	When UB > ZXOT and UB is forward zero-crossing, ZXUBIF is set to 1.If	ZXUBIE	ZXUBIF

	Interrupt	ZXUBIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXUBIF writes 1, clears 0 and clears interrupt simultaneously.		
1	UA Forward Zero-crossing Interrupt	When UA > ZXOT and UA is forward zero-crossing, ZXUAIF is set to 1.If ZXUAIE = 1, it will cause the INTN pin is toggled from high level to low level. ZXUAIF writes 1, clears 0 and clears interrupt simultaneously.	ZXUAIE	ZXUAIF
0	Waveform Sampling Interrupt	It synchronizes the 8Khz rate refresh with the waveform sampling register. WAVUDIF writes 1 and clears 0.If WAVUDIE = 1, It clears 0 and clears interrupt simultaneously.	WAVUDIE	WAVUDIF

Table 2-6-2 Interrupt in NVM1 Mode of RN8302B

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
1	NVM1 Mode Switching	Refer to the chapter NVM1IE and NVM1IF.	NVM1IE	NVM1Done

Table 2-6-3 Interrupt in NVM2 Mode of RN8302B

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
1	Completion of NVM 2 Mode Switching and Current Comparison	Refer to the chapter NVM2 IE and NVM2IF.	NVM 2IE	NVM 2Done

Note:

1. The RN8302B Interrupt Related to Operating Mode: The interrupt in the EMM mode doesn't play any role in the low power mode. The NVM1 interrupt plays its role in the NVM1 mode only, and the NVM2 interrupt plays its role in the NVM2 mode only, but doesn't play any role in any other modes.
2. IF is both the status register and the interrupt flag register. IF is not controlled by the IE interrupt Enable.

3 Register

3.1 Parameter Register List

Table 3-1 Parameter Register (Bank0) List

Address	Name	R/W	Byte Length	EMM Power-up Reset Value	Description
Total Measurement Parameter Register					
00H	UAWAV	R	3	--	Voltage sampling data of phase A
01H	UBWAV	R	3	--	Voltage sampling data of phase B
02H	UCWAV	R	3	--	Voltage sampling data of phase C
03H	IAWAV	R	3	--	Current sampling data of phase A
04H	IBWAV	R	3	--	Current sampling data of phase B
05H	ICWAV	R	3	--	Current sampling data of phase C
06H	INWAV	R	3	--	Neutral current sampling data
07H	UA	R	4	--	Voltage RMS of phase A
08H	UB	R	4	--	Voltage RMS of phase B
09H	UC	R	4	--	Voltage RMS of phase C
0AH	USUM	R	4	--	Voltage vector sum RMS
0BH	IA	R	4	--	Current RMS of phase A
0CH	IB	R	4	--	Current RMS of phase B
0DH	IC	R	4	--	Current RMS of phase C
0EH	IN	R	4	--	Neutral current RMS
0FH	Reserved			0x000000	Reserved
10H	ISUM	R	4	--	Current vector sum RMS
11H	IA_NVM1	R	3	0x000000	Current RMS of phase A in NVM1 mode
12H	IB_NVM1	R	3	0x000000	Current RMS of phase B in NVM1 mode
13H	IC_NVM1	R	3	0x000000	Current RMS of phase C in NVM1 mode
14H	PA	R	4	--	Active power of phase A

15H	PB	R	4	--	Active power of phase B
16H	PC	R	4	--	Active power of phase C
17H	PT	R	4	--	Active power of all-phase sum
18H	QA	R	4	--	Reactive power of phase A
19H	QB	R	4	--	Reactive power of phase B
1AH	QC	R	4	--	Reactive power of phase C
1BH	QT	R	4	--	Reactive power of all-phase sum
1CH	SA	R	4	--	Apparent power of phase A
1DH	SB	R	4	--	Apparent power of phase B
1EH	SC	R	4	--	Apparent power of phase C
1FH	ST	R	4	--	Apparent power of all-phase sum
20H	PfA	R	3	--	Power factor of phase A
21H	PfB	R	3	--	Power factor of phase B
22H	PfC	R	3	--	Power factor of phase C
23H	PfT	R	3	--	Power factor of all-phase sum
24H	PAFCnt	R/W	3	--	Active fast pulse count of phase A
25H	PBFCnt	R/W	3	--	Active fast pulse count of phase B
26H	PCFCnt	R/W	3	--	Active fast pulse count of phase C
27H	PTFCnt	R/W	3	--	Active fast pulse count of all-phase sum
28H	QAFCnt	R/W	3	--	Reactive fast pulse count of phase A
29H	QBFCnt	R/W	3	--	Reactive fast pulse count of phase B
2AH	QCFCnt	R/W	3	--	Reactive fast pulse count of phase C
2BH	QTFCnt	R/W	3	--	Reactive fast pulse count of all-phase sum
2CH	SAFCnt	R/W	3	--	Apparent fast pulse count of phase A
2DH	SBFCnt	R/W	3	--	Apparent fast pulse count of phase B
2EH	SCFCnt	R/W	3	--	Apparent fast pulse count of phase C
2FH	STFCnt	R/W	3	--	Apparent fast pulse count of all-phase sum
30H	EPA	R	3	--	Active energy register of phase

					A
31H	EPB	R	3	--	Active energy register of phase B
32H	EPC	R	3	--	Active energy register of phase C
33H	EPT	R	3	--	Active energy register of all-phase sum
34H	PosEPA	R	3	--	Forward active energy register of phase A
35H	PosEPB	R	3	--	Forward active energy register of phase B
36H	PosEPC	R	3	--	Forward active energy register of phase C
37H	Pos EPT	R	3	--	Forward active energy register of all-phase sum
38H	NegEPA	R	3	--	Reverse active energy register of phase A
39H	NegEPB	R	3	--	Reverse active energy register of phase B
3AH	NegEPC	R	3	--	Reverse active energy register of phase C
3BH	Neg EPT	R	3	--	Reverse active energy register of all-phase sum
3CH	EQA	R	3	--	Reactive energy register of phase A
3DH	EQB	R	3	--	Reactive energy register of phase B
3EH	EQC	R	3	--	Reactive energy register of phase C
3FH	EQT	R	3	--	Reactive energy register of all-phase sum
40H	Pos EQA	R	3	--	Forward reactive energy register of phase A
41H	Pos EQB	R	3	--	Forward reactive energy register of phase B
42H	PosEQC	R	3	--	Forward reactive energy register of phase C
43H	PosEQT	R	3	--	Forward reactive energy register of all-phase sum
44H	Neg EQA	R	3	--	Reverse reactive energy register of phase A

45H	Neg EQB	R	3	--	Reverse reactive energy register of phase B
46H	Neg EQC	R	3	--	Reverse reactive energy register of phase C
47H	Neg EQT	R	3	--	Reverse reactive energy register of all-phase sum
48H	ESA	R	3	--	Apparent energy register of phase A
49H	ESB	R	3	--	Apparent energy register of phase B
4AH	ESC	R	3	--	Apparent energy register of phase C
4BH	EST	R	3	--	Apparent energy register of all-phase sum
Fundamental and Hamonic Measurement Parameter Register					
50H	YUA	R	3	0x000000	Fundamental phase angle register of sampling channel UA
51H	YUB	R	3	--	Fundamental phase angle register of sampling channel UB
52H	YUC	R	3	--	Fundamental phase angle register of sampling channel UC
53H	YIA	R	3	--	Fundamental phase angle register of sampling channel IA
54H	YIB	R	3	--	Fundamental phase angle register of sampling channel IB
55H	YIC	R	3	--	Fundamental phase angle register of sampling channel IC
56H	YIN	R	3	--	Fundamental phase angle register of sampling channel IN
57H	UFreq	R	3	--	Voltage line frequency
58H	FUA	R	4	--	Fundamental Voltage RMS of phase A
59H	FUB	R	4	--	Fundamental Voltage RMS of phase B
5AH	FUC	R	4	--	Fundamental Voltage RMS of phase C
5BH	FIA	R	4	--	Fundamental current RMS of phase A
5CH	FIB	R	4	--	Fundamental current RMS of phase B
5DH	FIC	R	4	--	Fundamental current RMS of

					phase C
5EH	FPA	R	4	--	Fundamental active power of phase A
5FH	FPB	R	4	--	Fundamental active power of phase B
60H	FPC	R	4	--	Fundamental active power of phase C
61H	FPT	R	4	--	Fundamental active power of all-phase sum
62H	FQA	R	4	--	Fundamental reactive power of phase A
63H	FQB	R	4	--	Fundamental reactive power of phase B
64H	FQC	R	4	--	Fundamental reactive power of phase C
65H	FQT	R	4	--	Fundamental reactive power of all-phase sum
66H	FSA	R	4	--	Fundamental apparent power of phase A
67H	FSB	R	4	--	Fundamental apparent power of phase B
68H	FSC	R	4	--	Fundamental apparent power of phase C
69H	FST	R	4	--	Fundamental apparent power of all-phase sum
6AH	FPfA	R	3	--	Fundamental power factor of phase A
6BH	FPfB	R	3	--	Fundamental power factor of phase B
6CH	FPfC	R	3	--	Fundamental power factor of phase C
6DH	FPfT	R	3	--	Fundamental power factor of all-phase sum
6EH	FPAFCnt	R/W	3	--	Fundamental active fast pulse count of phase A
6FH	FPBFCnt	R/W	3	--	Fundamental active fast pulse count of phase B
70H	FPCFCnt	R/W	3	--	Fundamental active fast pulse count of phase C
71H	FPTFCnt	R/W	3	--	Fundamental active fast pulse count of all-phase sum

72H	FQAFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase A
73H	FQBFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase B
74H	FQCFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase C
75H	FQTFCnt	R/W	3	--	Fundamental reactive fast pulse count of all-phase sum
76H	FSAFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase A
77H	FSBFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase B
78H	FSCFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase C
79H	FSTFCnt	R/W	3	--	Fundamental apparent fast pulse count of all-phase sum
7AH	FEPA	R	3	--	Fundamental active energy of phase A
7BH	FEPB	R	3	--	Fundamental active energy of phase B
7CH	FEPC	R	3	--	Fundamental active energy of phase C
7DH	FEPT	R	3	--	Fundamental active energy of all-phase sum
7EH	PosFEPA	R	3	--	Fundamental forward active energy register of phase A
7FH	PosFEPB	R	3	--	Fundamental forward active energy register of phase B
80H	PosFEPC	R	3	--	Fundamental forward active energy register of phase C
81H	PosFEPT	R	3	--	Fundamental forward active energy register of all-phase sum
82H	NegFEPA	R	3	--	Fundamental reverse active energy register of phase A
83H	NegFEPB	R	3	--	Fundamental reverse active energy register of phase B
84H	NegFEPC	R	3	--	Fundamental reverse active energy register of phase C
85H	Neg FEPT	R	3	--	Fundamental reverse active energy register of all-phase sum
86H	FEQA	R	3	--	Fundamental reactive energy of

					phase A
87H	FEQB	R	3	--	Fundamental reactive energy of phase B
88H	FEQC	R	3	--	Fundamental reactive energy of phase C
89H	FEQT	R	3	--	Fundamental reactive energy of all-phase sum
8AH	PosFEQA	R	3	--	Fundamental forward reactive energy register of phase A
8BH	PosFEQB	R	3	--	Fundamental forward reactive energy register of phase B
8CH	PosFEQC	R	3	--	Fundamental forward reactive energy register of phase C
8DH	Pos FEQT	R	3	--	Fundamental forward reactive energy register of all-phase sum
8EH	NegFEQA	R	3	--	Fundamental reverse reactive energy register of phase A
8FH	NegFEQB	R	3	--	Fundamental reverse reactive energy register of phase B
90H	NegFEQC	R	3	--	Fundamental reverse reactive energy register of phase C
91H	NegFEQT	R	3	--	Fundamental reverse reactive energy register of all-phase sum
92H	FESA	R	3	--	Fundamental apparent energy register of phase A
93H	FESB	R	3	--	Fundamental apparent energy register of phase B
94H	FESC	R	3	--	Fundamental apparent energy register of phase C
95H	FEST	R	3	--	Fundamental apparent energy register of all-phase sum
96H	HUA	R	4	--	Harmonic voltage RMS of phase A
97H	HUB	R	4	--	Harmonic voltage RMS of phase B
98H	HUC	R	4	--	Harmonic voltage RMS of phase C
99H	HIA	R	4	--	Harmonic current RMS of phase A
9AH	HIB	R	4	--	Harmonic current RMS of phase B

9BH	HIC	R	4	--	Harmonic current RMS of phase C

3.2 Description of Parameter Register

3.2.1 Waveform Sample Register

ADDR	**00H**	**01H**	**02H**	**03H**	**04H**	**05H**	**06H**
REG	UAWAV	UBWAV	UCWAV	IAWAV	IBWAV	ICWAV	INWAV

The seven ADCs sampled data of RN8302B is output to the waveform sample register after the high-pass filter.

The waveform sample register is a 24-bit signed number and takes the complement code format,with the MSB as a sign bit.The data refresh rate is 8KHZ.

When the channel gain is calibrated, the normalized value of the peak for the waveform sample register = Normalized value of corresponding total RMS register * sqrt(2) * 0.5.

For the details on the channel U and the channel I gain calibration, refer to **Chapter 4 Calibration**.

The flag bit of the flag register WAVUPIF (EMMIF.0) will be set to 1 when the waveform sample register is updated, cleared after write 1 .If enable the waveform register update interrupt WAVUPIE (EMMIE.0), it will cause the interrupt once the update takes place, and the INTN pin outputs the low level.

3.2.2 RMS Register

ADDR	**07H**	**08H**	**09H**	**0AH**	**0BH**	**0CH**	**0DH**
REG	UA	UB	UC	USUM	IA	IB	IC
ADDR	**0EH**	**10H**	**11H**	**12H**	**13H**		
REG	IN	ISUM	IA_NVM1	IB_NVM1	IC_NVM1		
ADDR	**58H**	**59H**	**5AH**	**5BH**	**5CH**	**5DH**	
REG	FUA	FUB	FUC	FIA	FIB	FIC	
ADDR	**96H**	**97H**	**98H**	**99H**	**9AH**	**9BH**	
REG	HUA	HUB	HUC	HIA	HIB	HIC	

There are five types of RMS registers as follows:

1 Total voltage RMS and current RMS (UA/UB/UC/IA/IB/IC/IN)

2 Fundamental voltage RMS and current RMS (FUA/FUB/FUC/FIA/FIB/FIC)

3 Harmonic voltage RMS and current RMS (HUA/HUB/HUC/HIA/HIB/HIC)

4 Total voltage and current vector sum voltage RMS and current RMS (USUM/ISUM)

5 NVM1 current RMS (IA_NVM1/IB_NVM1/IC_NVM1)

The type 1-4 of RMS is the four-byte register, which is a 28-bit (bit0-bit27) signed

number and takes the complement code format. The bit27 is the sign bit, and bit28-bit31 and bit27 are identical and are always 0.The update cycle of these four types of RMS parameters is 250ms.

The NVM1 current RMS is a three-byte signed number and takes the complement code format. The bit23 is the sign bit, and bit23 is always 0.The update cycle of the parameter is 150ms.

The relationship between the current RMS Ix_NVM1 in the NVM1 mode and the current RMS Ix of corresponding phase in the EMM mode under the condition that the channel gain register GSIx = 0 is shown as follows: ***Ix_NVM1=Ix*1.80038/16***

The current channel gain register GSIx is valid for the current RMS Ix in the EMM mode only, but invalid for the current RMS Ix_NVM1 in the NVM1 mode.

The type 1 – 4 of RMS is valid in the EMM mode only, but invalid in the NVM1 mode. The current RMS in the NVM1 mode is valid in the NVM1 mode, and it will read 0 in the EMM mode. Above registers are invalid in the SLM and NVM2 mode.

For the RMS parameter, the ***actual voltage RMS and current RMS = Krmsx*RMSReg'.***

Where, Krmsx indicates the conversion factor and RMSReg' indicates the complement code of above RMS registers RMSReg. This operation is completed by MCU.

3.2.3 Power Register

ADDR	**14H**	**15H**	**16H**	**17H**	**18H**	**19H**	**1AH**	**1BH**
REG	PA	PB	PC	PT	QA	QB	QC	QT
ADDR	**1CH**	**1DH**	**1EH**	**1FH**				
REG	SA	SB	SC	ST				
ADDR	**5EH**	**5FH**	**60H**	**61H**	**62H**	**63H**	**64H**	**65H**
REG	FPA	FPB	FPC	FPT	FQA	FQB	FQC	FQT
ADDR	**66H**	**67H**	**68H**	**69H**				
REG	FSA	FSB	FSC	FST				

The power register includes the total active power PA/PB/PC/PT, reactive power QA/QB/QC/QT and apparent power SA/SB/SC/ST of the per-phase and all-phase sum, the fundamental active power FPA/FPB/FPC/FPT, reactive power FQA/FQB/FQC/FQT and apparent power FSA/FSB/FSC/FST of the per-phase and all-phase sum.

The power register takes the binary complement code format and is the 32-bit signed number. Where, the MSB is the sign bit. For the apparent power, the highest bit is always 0.The update cycle of the power parameter is 250ms.

For the power parameter, the ***actual power = Kpx* PReg'***.

Where, Kpx indicates the conversion factor and PReg' indicates the complement code of corresponding power register PReg. This operation is completed by MCU.

3.2.4 Power Factor Register

ADDR	20H	21H	22H	23H	6AH	6BH	6CH	6DH
REG	PfA	PfB	PfC	PfT	FPfA	FPfB	FPfC	FPfT

The power factor register includes the total power factor PfA/PfB/PfC/PfT of the per-phase and all-phase sum, and the fundamental power factor FPfA/FPfB/FPfC/FPfT of the per-phase and all-phase sum.

The power factor register takes the binary complement code format and is the 24-bit signed number. Where, the highest bit is the sign bit, which is determined by the sign bit of the active power. The update cycle of the power factor parameter is 250ms.

Calculation Formula of Power Factor Parameter: ***Actual Power Factor = PfReg'/2^{23}***

Where, PfReg' indicates the complement code of corresponding power factor register PfReg.

3.2.5 Fast Pulse Count Register

ADDR	24H	25H	26H	27H	28H	29H
REG	PAFCnt	PBFCnt	PCFCnt	PTFCnt	QAFCnt	QBFCnt
ADDR	2AH	2BH	2CH	2DH	2EH	2FH
REG	QCFCnt	QTFCnt	SAFCnt	SBFCnt	SCFCnt	STFCnt
ADDR	6EH	6FH	70H	71H	72H	73H
REG	FPAFCnt	FPBFCnt	FPCFCnt	FPTFCnt	FQAFCnt	FQBFCnt
ADDR	74H	75H	76H	77H	78H	79H
REG	FQCFCnt	FQTFCnt	FSAFCnt	FSBFCnt	FSCFCnt	FSTFCnt

The fast pulse count register includes the total/fundamental, active/reactive/apparent and per-phase/all-phase sum fast pulse count register.

The fast pulse count register is a 18-bit (bit0 - bit17) signed number. Where, the bit17 is the sign bit, which is determined by the sign bit of the power. The bit18 - bit23 are the invalid bit, which is fixed to 0.

When the input is forward, Fcnt will increase forwardly, and it will compare HFCONST1 with Fcnt/2. If they are equal, Fcnt will clear zero, and corresponding energy register will increase by 1.When the input is reverse, Fcnt will increase reversely, and it will compare HFCONST1 with the complement code of Fcnt/2. If they are equal to each other, Fcnt will clear zero, and corresponding energy register will increase by 1.

3.2.6 Energy Register

ADDR	30H	31H	32H	33H	34H	35H	36H
REG	EPA	EPB	EPC	EPT	PosEPA	PosEPB	PosEPC
ADDR	37H	38H	39H	3AH	3BH	3CH	3DH

REG	PosEPT	NegEPA	NegEPB	NegEPC	NegEPT	EQA	EQB
ADDR	**3EH**	**3FH**	**40H**	**41H**	**42H**	**43H**	**44H**
REG	EQC	EQT	PosEQA	PosEQB	PosEQC	PosEQT	NegEQA
ADDR	**45H**	**46H**	**47H**	**48H**	**49H**	**4AH**	**4BH**
REG	NegEQB	NegEQC	NegEQT	ESA	ESB	ESC	EST
ADDR	**7AH**	**7BH**	**7CH**	**7DH**	**7EH**	**7FH**	**80H**
REG	FEPA	FEPB	FEPC	FEPT	PosFEPA	PosFEPB	PosFEPC
ADDR	**81H**	**82H**	**83H**	**84H**	**85H**	**86H**	**87H**
REG	PosFEPT	NegFEPA	NegFEPB	NegFEPC	NegFEPT	FEQA	FEQB
ADDR	**88H**	**89H**	**8AH**	**8BH**	**8CH**	**8DH**	**8EH**
REG	FEQC	FEQT	PosFEQA	PosFEQB	PosFEQC	PosFEQT	NegFEQA
ADDR	**8FH**	**90H**	**91H**	**92H**	**93H**	**94H**	**95H**
REG	NegFEQB	NegFEQC	NegFEQT	FESA	FESB	FESC	FEST

The energy register is a 24-bit unsigned number. The energy represented by the minimum unit of the register is 1/EC KWh. Of which, EC is the EC.

The RN8302B provides several types of the energy registers, including the fundamental/total, active/reactive/apparent, per-phase/all-phase sum, active and reactive forward/reverse energy register.

The energy register can be configured into the cleared type or cumulative type. If the bit of the ERegCAR (EMUCFG.19) register = 0, all energy registers are of the cleared type. If the bit of the ERegCAR (EMUCFG.19) register = 1, all energy registers are of the cumulative type. It is of the cleared type by default.

The forward active and reactive energy register meters the energy with the power more than 0 only, and the reverse active and reactive energy register meters the energy with the power less than 0 only.

The cumulative mode of the active energy register for the all-phase sum can be configured as the algebraic sum type and the absolute value sum type in the three-phase four-wire mode. If the bit of the EPADDMODE (EMUCFG.20) register = 0, the cumulative mode is of the algebraic sum type, and the active energy of the all-phase sum is integer by the algebraic sum of the per-phase power PA+PB+PC. If the bit of the EPADDMODE (EMUCFG.20) register = 1, the cumulative mode is of the absolute value sum type, and the active energy of the all-phase sum is integer by the absolute value sum type of the per-phase power |PA|+|PB|+|PC|. It is of the algebraic sum type by default.

The cumulative mode of the reactive energy register for the all-phase sum can be configured as the algebraic sum type and the absolute value sum type in the three-phase four-wire mode. If the bit of the EPADDMODE (EMUCFG.21) register = 0, the cumulative mode is of the algebraic sum type, and the reactive energy of the all-phase sum is integer by the algebraic sum of the per-phase power QA+QB+QC. If the bit of the EPADDMODE

(EMUCFG.21) register = 1, the cumulative mode is of the absolute value sum type, and the reactive energy of the all-phase sum is integer by the absolute value sum type of the per-phase power |QA|+|QB|+|QC|. It is of the algebraic sum type by default.

Note that the cumulative mode of the active and reactive energy register of the all-phase sum plays its role in the energy register of the all-phase sum, but doesn't play any role in the power register of the all-phase sum.

There is only the algebraic sum type for the active and reactive energy register of the all-phase sum in the three-phase three-wire mode. The bit of the EPADDMODE and EQADDMODE register can not be configured.

3.2.7 Phase Angle Register

ADDR	50H	51H	52H	53H	54H	55H	56H
REG	YUA	YUB	YUC	YIA	YIB	YIC	YIN

These registers are 24-bit unsigned number, which indicates the phase angle for each sample channel fundamental and the reference voltage channel fundamental. If take the UA channel as the phase angle reference, YIB indicates the phase angle between the fundamental IB and the fundamental UA. Users can get the phase angle of any two phases by the simple operation, for example, the phase angle between IA and IB is YIAIB = YIA - YIB. The update cycle is 32 signal cycles.

Three-phase four-wire: If FUA>ZXOT (normalized value, the same below), take the UA channel as the phase angle test benchmark. If FUA <ZXOT and FUB is greater than ZXOT, take the UB channel as the phase angle test benchmark. If FUA<ZXOT, FUB<ZXOT and FUC>ZXOT, take the UC channel as the phase angle test benchmark. If three phase fundamental voltages< ZXOT, each phase angles are 0.

Three-phase three-wire: If FUA > ZXOT, take the UA channel as the phase angle test benchmark. If FUA<ZXOT and FUC > ZXOT, take the UC channel as the phase angle test benchmark. If both FUA and FUC < ZXOT, each phase angles are 0.

When take the UA channel as the benchmark, if any one of FUB, FUC, FIA, FIB, FIC and FIN< ZXOT, this phase angle is 0, and if any one of FUC, FIA, FIB, FIC and FIN<ZXOT, this phase angle is 0. When take the UC channel as the benchmark, if any one of FIA, FIB, FIC and FIN< ZXOT, this phase angle is 0

Calculation Formula of Phase Angle: ***Actual Phase Angle = (REGY/2^{24})*360^{o}***. REGY indicates the value of the phase angle register.

3.2.8 Voltage Line Frequency Register

ADDR: 57H, REG: Ufreq.

This register is a 24-bit unsigned number, is the line frequency of the voltage. The update cycle is 32 signal cycles.

Three-phase four-wire: If FUA > ZXOT (normalized value, the same below), take the

UA channel as the frequency test benchmark. If FUA<ZXOT and FUB > ZXOT, take the UB channel as the frequency test benchmark. If FUA<ZXOT, FUB<ZXOT and FUC > ZXOT, take the UC channel as the frequency test benchmark.

Three-phase three-wire: If FUA > ZXOT, take the UA channel as the frequency test benchmark. If FUA<ZXOT and FUC > ZXOT, take the UC channel as the frequency test benchmark.

Calculation Formula of Voltage Line Frequency: ***Actual Frequency = fosc*8/REGF***. REGF indicates the value of the frequency register.

3.3 Configuration and Status Register List

Table 3-2 Configuration and Status Register (Bank1) List

Address	Name	R/W	Byte Length	EMM Power-up Reset Value	Description
EMM Calibration Register					
00H	HFConst1	R/W	2	0x1000	High-frequency pulse constant register 1
01H	HFConst2	R/W	2	0x1000	High-frequency pulse constant register 2
02H	IStart_PS	R/W	2	0x0250	Active and apparent startup current threshold register
03H	IStart_Q	R/W	2	0x0250	Reactive startup current threshold register
04H	LostVoltT	R/W	2	0x0400	**Loss of voltage** threshold
05H	ZXOT	R/W	2	0x0073	Zero-crossing threshold
06H	PRTH1L	R/W	2	0x0000	Lower limit of piecewise phase calibration current threshold 1
07H	PRTH1H	R/W	2	0x0000	Upper limit of piecewise phase calibration current threshold 1
08H	PRTH2L	R/W	2	0x0000	Lower limit of piecewise phase calibration current threshold 2
09H	PRTH2H	R/W	2	0x0000	Upper limit of piecewise phase calibration current threshold 2
0AH	IRegion3L	R/W	2	0x0000	Lower limit of current threshold 3
0BH	IRegion3H	R/W	2	0x0000	Upper limit of current threshold 3
0CH	PHSUA	R/W	1	0x80	Phase calibration register of sampling channel UA
0DH	PHSUB	R/W	1	0x80	Phase calibration register of

					sampling channel UB
0EH	PHSUC	R/W	1	0x80	Phase calibration register of sampling channel UC
0FH	PHSIA	R/W	3	0x808080	Per-phase calibration register of sampling channel IA
10H	PHSIB	R/W	3	0x808080	Per-phase calibration register of sampling channel IB
11H	PHSIC	R/W	3	0x808080	Per-phase calibration register of sampling channel IC
12H	PHSIN	R/W	1	0x80	Phase calibration of sample channel IN
13H	GSUA	R/W	2	0x0000	Channel gain of sample channel UA
14H	GSUB	R/W	2	0x0000	Channel gain of sample channel UB
15H	GSUC	R/W	2	0x0000	Channel gain of sample channel UC
16H	GSIA	R/W	2	0x0000	Channel gain of sample channel IA
17H	GSIB	R/W	2	0x0000	Channel gain of sample channel IB
18H	GSIC	R/W	2	0x0000	Channel gain of sample channel IC
19H	GSIN	R/W	2	0x0000	Channel gain of sample channel IN
1AH	DCOS_UA	R/W	2	0x0000	DC OFFSET calibration of sample channel UA
1BH	DCOS_UB	R/W	2	0x0000	DC OFFSET calibration of sample channel UB
1CH	DCOS_UC	R/W	2	0x0000	DC OFFSET calibration of sample channel UC
1DH	DCOS_IA	R/W	2	0x0000	DC OFFSET calibration of sample channel IA
1EH	DCOS_IB	R/W	2	0x0000	DC OFFSET calibration of sample channel IB
1FH	DCOS_IC	R/W	2	0x0000	DC OFFSET calibration of sample channel IC
20H	DCOS_IN	R/W	2	0x0000	DC OFFSET calibration of sample channel IN
21H	UA_OS	R/W	2	0x0000	Voltage RMS Offset of phase A
22H	UB_OS	R/W	2	0x0000	Voltage RMS Offset of phase B
23H	UC_OS	R/W	2	0x0000	Voltage RMS Offset of phase C
24H	IA_OS	R/W	2	0x0000	Current RMS Offset of phase A
25H	IB_OS	R/W	2	0x0000	Current RMS Offset of phase B
26H	IC_OS	R/W	2	0x0000	Current RMS Offset of phase C

27H	IN_OS	R/W	2	0x0000	Current RMS Offset of neutral line 1
28H	GPA	R/W	2	0x0000	Active power gain of phase A
29H	GPB	R/W	2	0x0000	Active power gain of phase B
2AH	GPC	R/W	2	0x0000	Active power gain of phase C
2BH	GQA	R/W	2	0x0000	Reactive power gain of phase A
2CH	GQB	R/W	2	0x0000	Reactive power gain of phase B
2DH	GQC	R/W	2	0x0000	Reactive power gain of phase C
2EH	GSA	R/W	2	0x0000	Apparent power gain of phase A
2FH	GSB	R/W	2	0x0000	Apparent power gain of phase B
30H	GSC	R/W	2	0x0000	Apparent power gain of phase C
31H	PA_PHS	R/W	2	0x0000	Active phase calibration register of phase A
32H	PB_PHS	R/W	2	0x0000	Active phase calibration register of phase B
33H	PC_PHS	R/W	2	0x0000	Active phase calibration register of phase C
34H	QA_PHS	R/W	2	0x0000	Reactive phase calibration register of phase A
35H	QB_PHS	R/W	2	0x0000	Reactive phase calibration register of phase B
36H	QC_PHS	R/W	2	0x0000	Reactive phase calibration register of phase C
37H	PA_OS	R/W	2	0x0000	Active power Offset of phase A
38H	PB_OS	R/W	2	0x0000	Active power offset of phase B
39H	PC_OS	R/W	2	0x0000	Active power offset of phase C
3AH	QA_OS	R/W	2	0x0000	Reactive power offset of phase A
3BH	QB_OS	R/W	2	0x0000	Reactive power offset of phase B
3CH	QC_OS	R/W	2	0x0000	Reactive power offset of phase C
3DH	FUA_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase A
3EH	FUB_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase B
3FH	FUC_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase C
40H	FIA_OS	R/W	2	0x0000	Fundamental current RMS offset of phase A
41H	FIB_OS	R/W	2	0x0000	Fundamental current RMS offset of phase B
42H	FIC_OS	R/W	2	0x0000	Fundamental current RMS offset of phase C

43H	GFPA	R/W	2	0x0000	Fundamental active power gain of phase A
44H	GFPB	R/W	2	0x0000	Fundamental active power gain of phase B
45H	GFPC	R/W	2	0x0000	Fundamental active power gain of phase C
46H	GFQA	R/W	2	0x0000	Fundamental reactive power gain of phase A
47H	GFQB	R/W	2	0x0000	Fundamental reactive power gain of phase B
48H	GFQC	R/W	2	0x0000	Fundamental reactive power gain of phase C
49H	GFSA	R/W	2	0x0000	Fundamental apparent power gain of phase A
4AH	GFSB	R/W	2	0x0000	Fundamental apparent power gain of phase B
4BH	GFSC	R/W	2	0x0000	Fundamental apparent power gain of phase C
4CH	FPA_PHS	R/W	2	0x0000	Fundamental active phase calibration register of phase A
4DH	FPB_PHS	R/W	2	0x0000	Fundamental active phase calibration register of phase B
4EH	FPC_PHS	R/W	2	0x0000	Fundamental active phase calibration register of phase C
4FH	FQA_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase A
50H	FQB_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase B
51H	FQC_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase C
52H	FPA_OS	R/W	2	0x0000	Fundamental active power offset of phase A
53H	FPB_OS	R/W	2	0x0000	Fundamental active power offset of phase B
54H	FPC_OS	R/W	2	0x0000	Fundamental active power offset of phase C
55H	FQA_OS	R/W	2	0x0000	Fundamental reactive power offset of phase A
56H	FQB_OS	R/W	2	0x0000	Fundamental reactive power offset of phase B
57H	FQC_OS	R/W	2	0x0000	Fundamental reactive power offset

					of phase C
58H	SAGCFG	R/W	3	0x000000	Voltage sag threshold configuration
59H	OVLVL	R/W	2	0x0000	Overvoltage threshold configuration
5AH	OILVL	R/W	2	0x0000	Overcurrent threshold configuration
EMM Configuration and Status Register					
60H	CFCFG	R/W	3	0x043210	CF pin configuration register
61H	EMUCFG	R/W	3	0x400000	EMU configuration register
62H	EMUCON	R/W	3	0x000000	EMU control register
63H	WSAVECON	R/W	1	0x00	Sampling data write cache control register
64H	EMMIE	R/W	2	0x0000	EMM interrupt enable register, write protection
65H	EMMIF	R	2	--	EMM interrupt flag and status register
66H	PQSign	R	2	--	Active and reactive power orientation register
67H	Noload	R	2	--	No-load and startup status register
68H	IRegionS	R	1	--	Current piecewise status register
69H	PHASES	R	2	--	Phase voltage and current status register
6AH	CheckSum1	R	3	--	EMM calibration and configuration register checksum
NVM1 Configuration and Status Register					
70H	NVM1CFG	R/W	1	0x01	NVM1 configuration register
71H	NVM1IF	R	1	--	NVM1 status register
NVM2 Configuration and Status Register					
72H	NVM2CFG	R/W	2	0x0F21	NVM2 Configuration Register
73H	NVM2CMPA	R/W	2	0x0256	NVM2 IA comparator control register
74H	NVM2CMPB	R/W	2	0x0256	NVM2 IB comparator control register
75H	NVM2CMPC	R/W	2	0x0256	NVM2 IC comparator control register
76H	NVM2IF	R	1	0x00	**NVM2** status register
System Configuration Register					
80H	WREN	R/W	1	0x00	Write enable register
81H	WMSW	R/W	1	It is the same as the pin PM	Operating mode switching register

				configuration.	
82H	SOFTRST	R/W	1	0x00	Software reset register
83H	ADCCFG	R/W	2	0x0000	ADC configuration register
86H	MODSEL	R/W	1	0x00	Three-phase four-wire/three-phase three-wire mode selection register
System Status Register					
8AH	SYSSR	R	2	--	System status register
8BH	CheckSum2	R	2	--	NVM1, NVM2 system configuration register checksum
8CH	RData	R	4	--	Data read by SPI previous time
8DH	WData	R	3	--	Data written by SPI previous time
8EH	LRBufAddr	R	2	0x0000	Address of waveform cache read last time
8FH	DeviceID	R	3	0x830200	RN8302B Device ID

3.4 Description of Configuration and Status Register

3.4.1 High-frequency Pulse Constant Register

Including two HFCONST registers HFCONST1 (0x00) and HFCONST2 (0x01). HFCONST1 can be used to configure the energy constant, and HFCONST2 can be used to output the CF high-frequency pulse during the calculation of the maximum demand or the small-signal CF acceleration function during the calibration.

Each CF pin can select whether the pulse is output via HFCONST1 or HFCONST2 by the CFCFG (0x60) register. During the comparison, compare it with the high 16-bit of the absolute value for PTFCNT, QTFCNT, STFCNT, FPTFCNT, FQTFCNT and FSTFCNT of the all-phase sum. If it is greater than or equal to the HFConst selected by CFCFG, it will output the CF pulse correspondingly.

The addition of the energy register is related to HFCONST1 only. Compare HFCONST1 with the high 16-bit of the absolute value for the fast pulse count register of the all-phase sum. If it is greater than or equal to the HFConst1, corresponding energy register is added by 1.

HFConst1 and HFConst2 are 1000H by default.

For the details on the calculation of HFConst, refer to **Chapter 4 Calibration Method**.

3.4.2 Startup Current Threshold Register

The RN8302B provides two startup current threshold registers. The total/fundamental active and apparent shares one startup current threshold register IStart_PS (0x02), and the

total and fundamental reactive shares one startup current threshold register IStart_Q (0x03).

IStart_PS and IStart_Q are 16-bit unsigned number. It is extended to 32-bit 0x000X_XXX0 to compare with the total current RMS IxRMS of each phase or the fundamental current RMS FIxRMS, to judge the no-load or startup.

Calculation Formula of IStart_PS and IStart_Q:

$$I_{Start} = (REGI_b * K) / 2\text{^}4$$

Where, IStart is the startup current threshold register value to be set, REGIb is the total or fundamental current RMS register value of the point Ib after the calibration, K = the ratio of the startup current to the nominal current value for some phase. If the startup current is 0.001Ib, K=0.001.

The reset value of IStart_Q is the same as that of IStart_PS, and both of them are 0x250. Users can reset them as needed.

3.4.3 Loss of voltage **Threshold Register**

This register LostVoltage (0x04) is used to set the loss of voltage threshold of RN8302B.It is a 16-bit unsigned number. Compare it with the high 16-bit of the total voltage RMS for each phase, namely bit27 - bit11, to judge the loss of voltage.

The default value of LostVoltage is 0x0400.Users can reset them as needed.

Calculation Formula of LostVoltage:

$$LostVoltage = INT((REGV_n * K) / 2\text{^}12))$$

Where, REGVn is the total voltage RMS register value of the rated voltage input after the calibration, and K = the ratio of the loss of voltage to the rated voltage for some phase. If the loss of voltage is 50% of the rated voltage, K = 0.5.

3.4.4 Zero-crossing Threshold Register

When the fundamental RMS of some channel is less than the zero-crossing threshold register value, this channel will not output the zero-crossing or calculate phase angle. The phase angle outputs 0x000000.

This register ZXOT (0x05) is a 16-bit unsigned number. Compare it with the bit27 - bit11 of the fundamental voltage RMS and current RMS FUx and FIx (x = A, B, C, the same below) of each phase, to judge it. The reset value of ZXOT is 0x0073. Users can reset them as needed.

Calculation Formula of ZXOT:

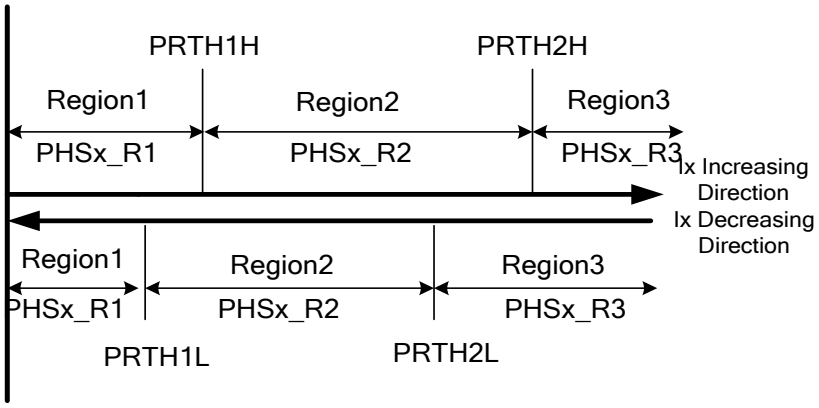
$$ZXOT = INT((REGI_b * K) / 2\text{^}12)$$

Where, REGIb is fundamental current RMS register value at the point Ib after

calibration, and K = the ratio of the zero-crossing threshold to the current at the point Ib for some phase. If the zero-crossing threshold is 50% of the rated current, K = 0.05.

3.4.5 Phase Compensation Region Setup Register

These registers PRTHx are used to set the per-phase angle difference calibration region. There are two pairs of the per-phase calibration current threshold PRTH registers with the address 0x06 - 0x09.As shown in the figure below: PRTH1L (0x06)/ PRTH1H (0x07) and PRTH2L (0x08)/ PRTH2H (0x09) can configure three split points of phase calibration regions. Region1 takes PHSx_R1 as the phase calibration parameter, Region2 takes PHSx_R2 as the phase calibration parameter, and Region3 takes PHSx_R3 as the phase calibration parameter. In the current Ix increment direction of some phase, it takes PRTH1H as the split point of Region1 and Region2 and PRTH2H as the split point of Region2 and Region3. In the current Ix decrement direction of some phase, it takes PRTH1L as the split point of Region1 and Region2 and PRTH2L as the split point of Region2 and Region3.



PRTHx is a 16-bit unsigned number. Compare it with bit27 - bit1 of the total current RMS Ix (x = A, B, C, the same below) for each phase, namely bit27 - bit12, to judge it.

Fault Tolerance: For ① When write PRTH2x < PRTH1x, fail to write it. ② When write PRTH1H < PRTH1L or PRTH1L > PRTH1H, fail to write it. ③ When write PRTH2H < PRTH2L or PRTH2L > PRTH2H, fail to write it.

When the PRTH1L register is 0, can not start the per-phase calibration, and clear PRTH1H (0x07) and PRTH2L (0x08)/PRTH2H (0x09).The current channel takes the low 8-bit of the PHSIx register as the phase calibration value of each channels.

3.4.6 Current Split Region Setup Register

Iregion3L (0x0A) and Iregion3H (0x0B) are not parallel with phase calibration register and are used to generate the current section flag and interrupt.

These two registers are the 16-bit unsigned number.Compare it with bit27 - bit12 of the total current RMS Ix (x = A, B, C) for each phase, to judge it. According to the result of the phase current and the Iregion3 threshold comparison, corresponding flag of the IregionS

status register is set or cleared. If the Iregion3x interrupt is enabled, it will generate the interrupt.

Fault Tolerance: When write Iregion3H < Iregion3L or Iregion3L > Iregion3H, fail to write it.

When the Iregion3L register is 0, disable this function.

3.4.7 Channel Phase Calibration Register

ADDR	0CH	0DH	0EH	0FH	10H	11H	12H
REG	PHSUA	PHSUB	PHSUC	PHSIA	PHSIB	PHSIC	PHSIN

PHSUA, PHSUB, PHSUC and PHSIN are used for phase calibration of UA, UB, UC and IN. These registers are 8-bit unsigned number, 0x80 by default. Under the condition of 50HZ, fosc=8.192Mhz, 1 LSB represents ***0.017578°***/LSB phase calibration.

PHSIA-PHSIC is used for the section calibration of three calibration regions for three current channels together with register PRTHx.These three registers are the 24-bit unsigned number. Take PHSIA as an example, three bytes of this register are shown as follows: {PHSIA_R3[23:16], PHSIA_R2[15:8] and PHSIA_R1[7:0]}.

Where, the low 8-bit PHSIA_R1[7:0] represents the phase calibration value of the region 1, the intermediate 8-bit PHSIA_R2[15:8] represents the phase calibration value of the region 2, and the high 8-bit PHSIA_R3[23:16] represents the phase calibration value of the region 3.The default value is 0x808080.

Phase Calibration Range: ±2.259° or 4.518° at 50HZ.

Phase Compensation Formula:

① Active error calibration during 0.5L. If the error at the 0.5L,I=Ib for some phase is err and the channel angle difference is θ, then:

$$\theta = \mathrm{Arcsin}\frac{-err}{\sqrt{3}}$$

For 50HZ, there is the relationship 0.017578°/LSB between the register PHSUA and the register PHSIA.

If adjust the PHSUA register, ***PHSUA = 0x80+INT (θ/0.017578°)***.

If adjust the PHSIA register and don't take the section calibration into account, then ***PHSIA_R1[7:0] = 0x80-INT (θ/0.017578°)***.

② Take the input of one channel as the benchmark, get the difference between the actual angle difference of the calibrated channel 1 and the reference channel 2 and the angle difference of the the program controlled power or the standard table as θ. If the phase register of this channel before the calibration, then

For 50HZ, the phase of the calibration channel ***PHS= PHS1+INT (θ/0.017578°)***.

3.4.8 Channel Gain Register

ADDR	13H	14H	15H	16H	17H	18H	19H
REG	GSUA	GSUB	GSUC	GSIA	GSIB	GSIC	GSIN

These registers can be used for the gain calibration of the RMS and power. They are 2-byte signed number and take the binary complement format,with the MSB as a sign bit , calibration range is (-1, +1).

Calibration Formula: If RegGain>=2^{15}, ***Gain=(RegGain-2^{16})/2^{15}***. Otherwise ***Gain=RegGain/2^{15}***. Of which, RegGain is the channel gain register value.

Taking the IB channel as an example, we assume the current RMS of the channel B before the calibration is IB, and the current RMS of the channel B after the calibration is IB', the relationship between them is ***IB'=IB+IB*Gain***.

The channel gain register is applicable for the gain calibration in the power calibration method. For the details ,refer to **Chapter 4 Calibration Method**.

3.4.9 Channel DC OFFSET Calibration Register

ADDR	1AH	1BH	1CH	1DH	1EH	1FH	20H
REG	DCOS_UA	DCOS_UB	DCOS_UC	DCOS_IA	DCOS_IB	DCOS_IC	DCOS_IN

These registers are used to replace the high-pass filter to eliminate the offset error during the measure of the DC component.

These register are 2-byte signed number and takes the binary complement format,with the MSB as a sign bit.

Calculation Formula: Taking the IA channel as an example, Assume the RMS of the IA channel is IA when the DCOS_IA is equal to 0, and the RMS register of the IA channel is IA' and DCOS_IA' is the complement code of the DCOS_IA register when the DCOS_IA is not equal to 0.

IA'= Sqrt（Abs((IA/2^{27})^2+Sign(DCOS_IA)*(DCOS_IA'/2^{15})^2)）*2^{27}

3.4.10 RMS OFFSET Calibration Register

ADDR	21H	22H	23H	24H	25H	26H	27H
REG	UA_OS	UB_OS	UC_OS	IA_OS	IB_OS	IC_OS	IN_OS
ADDR	3DH	3EH	3FH	40H	41H	42H	
REG	FUA_OS	FUB_OS	FUC_OS	FIA_OS	FIB_OS	FIC_OS	

Small signal accuracy of current RMS calibration for the voltage/current/fundamental voltage/fundamental energy. 2-byte signed number and takes the binary complement format, with the MSB as the sign bit.

Calibration Formula: Taking the IA channel as an example, assume the current RMS

register of phase A before the calibration is IA and the current RMS register of phase A before the calibration is IA', then ***IA'=Sqrt(Abs(IA^2+IA_OS*2^{14}))***.

3.4.11 Power Gain Register

ADDR	**28H**	**29H**	**2AH**	**2BH**	**2CH**	**2DH**	**2EH**
REG	GPA	GPB	GPC	GQA	GQB	GQC	GSA
ADDR	**2FH**	**30H**	**43H**	**44H**	**45H**	**46H**	**47H**
REG	GSB	GSC	GFPA	GFPB	GFPC	GFQA	GFQB
ADDR	**48H**	**49H**	**4AH**	**4BH**			
REG	GFQC	GFSA	GFSB	GFSC			

These registers are used for the gain calibration of the active/reactive/apparent/fundamental active/fundamental reactive/fundamental apparent power. 2-byte signed number and takes the binary complement format,with the MSB as the sign bit.

Calibration Formula: ***P1=P0(1+GP)***

Q1=Q0(1+GQ)

S1=S0(1+GS)

Where, P1, Q1 and S1 are the active, reactive and apparent power after the calibration, P0, Q0 and S0 are the power before the calibration, and GP, GQ and GS are the normalized value of the gain calibration register for the active, reactive and apparent power respectively.

These registers are applicable for the power gain calibration of the traditional pulse calibration, and the calibration error range is -∞- 50%.Taking the PF = 1.0 calibration of phase A as an example, and assume the active error reading of the normative meter is Err when IA=Ib, the calculation method of GPA is shown as follow:

$$Gain = \frac{-Err}{1+Err}$$

If the gain≥0, then ***GPA=INT[Gain*2^{15}]***. if the gain＜0, then ***GPA=INT[2^{16}+Gain*2^{15}]***.

3.4.12 Power Phase Calibration Register

ADDR	**31H**	**32H**	**33H**	**34H**	**35H**	**36H**	**4CH**
REG	PA_PHS	PB_PHS	PC_PHS	QA_PHS	QB_PHS	QC_PHS	FPA_PHS
ADDR	**4DH**	**4EH**	**4FH**	**50H**	**51H**		
REG	FPB_PHS	FPC_PHS	FQA_PHS	FQB_PHS	FQC_PHS		

The power phase calibration register takes the 2-byte binary complement format, with the MSB is the sign bit.

Calibration Formula: ***P2= P1+P_PHS*Q1***

Q2 = Q1-Q_PHS*P1

Where, P1 is the active power before the calibration, P2 is the active power after the calibration, Q1 is the reactive power before the calibration, and Q2 is the reactive power after the calibration. P_PHS and Q_PHS are the normalized value of the phase calibration register for the active and reactive power respectively.

Calibration Method: Taking phase A as an example, assume PF = 1.0, active gain calibration of phase A is completed, and assume PF=0.5L ,IA=Ib, the active error of the normative meter for phase A is Err, then,

$$\lambda = \frac{-Err}{1.732}$$

If $\lambda \geqslant 0$, then ***PA_PHS=*** λ ****2^15***. If λ <0, then ***PA_PHS=*** λ ****2^15+2^16***.

$$\gamma = \frac{-Err}{0.866}$$

If $\gamma \geqslant 0$, then ***QA_PHS=*** γ ****2^15***. If γ <0, then ***QA_PHS=*** γ ****2^15+2^16***.

3.4.13 Power OFFSET Calibration Register

ADDR	**37H**	**38H**	**39H**	**3AH**	**3BH**	**3CH**	**52H**
REG	PA_OS	PB_OS	PC_OS	QA_OS	QB_OS	QC_OS	FPA_OS
ADDR	**53H**	**54H**	**55H**	**56H**	**57H**		
REG	FPB_OS	FPC_OS	FQA_OS	FQB_OS	FQC_OS		

These registers are applicable for the precision calibration of the small signal for the total active/total reactive/fundamental active/fundamental reactive power. 2-byte signed number and take the binary complement format,with the MSB as the sign bit.

Calibration Formula: Taking the active power of the channel A as an example, assume the active power register of the channel A before the calibration is PA and the active power register of the channel A after the calibration is PA', then ***PA'=PA+ PA_OS***.

3.4.14 Voltage Sag Threshold Register

Address: 58H, Length: Three bytes, Default Value: 000000H

Bit	**Bit Name**	**Description**
16-23	SAGCYC[7:0]	Voltage sag time threshold. For the details, see below. = 00H, Disable the voltage sag judging function.
0-15	SAGLVL[15:0]	Voltage sag threshold configuration. If the high 16-bit of the absolute value for the voltage fundamental sample peak value of some phase< SAGLVL [15:0] and the duration is SAGCYC [7:0] half cycles, it is judged as voltage sag. This will cause the bit of SAGUx (x=A, B, C) in the PHASES register is set to 1, and the bit of SAGIF in the EMMIF register is set to 1. If SAGIE = 1 in the

		EMMIE register, it will cause the interrupt of INT. write 1 to clear SAGIF,interrupt,and clear the SAGUx flag. For the details, refer to the PHASES register and the EMMIE register and EMMIF register. = 0000H,disable this function.

Calculation Formula of SAGLVL:

$$SAGLVL = INT((\sqrt{2} * REGV_n * K) / 2\text{^}12)$$

Where, REGVn is the fundamental voltage RMS register value of the rated voltage input after the calibration, and K = the ratio of the voltage sag threshold to the rated voltage for some phase. If the voltage sag threshold is 10% of the rated voltage, K = 0.1.

3.4.15 Overvoltage and Overcurrent Threshold Register

It includes the overvoltage threshold register OVLVL and the overcurrent threshold register OILVL.

Overvoltage Threshold Register OVLVL:

Address: 59H, Length: Two bytes, Default Value: 0000H

When the high 16-bit of the absolute value for the voltage sample value of some phase is greater than OVLVL[15:0], judge this phase voltage is overvoltage. This will cause the bit OVUx (x=A, B, C) for this phase in the PHASES register set to 1, and the bit of OVIIF in the EMMIF register is set to 1. If OVIIE=1 in the EMMIE register, setting OVIIF to 1 will cause the interrupt. Write 1 to OVIIF to clear this bit and clear the interrupt and the OVUx flag. For the details, refer to the PHASES register and the EMMIE register and EMMIF register.

If OVLVL[15:0] = 0000H, disable the voltage sag judging function.

Calculation Formula of OVLVL:

$$OVLVL = INT((\sqrt{2} * REGV_n * K / 2\text{^}12))$$

Where, REGVn is the total voltage RMS register value of the rated voltage input after the calibration, and K = the ratio of the overvoltage to the rated voltage for some phase. If the overvoltage is 1.2 times of the rated voltage, K = 1.2.

Overcurrent Threshold Register OILVL:

Address: 5AH, Length: Two bytes, Default Value: 0000H

When the high 16-bit of the absolute value for the current sample value of some phase is greater than OILVL[15:0], judge this phase current is overcurrent. This will cause the bit of the OVIx (x=A, B, C) for this phase in the PHASES register set to 1, and the bit of the OVIIF n the EMMIF register is set to 1. If OVIIE=1 in the EMMIE register, setting OVIIF to 1 will cause the interrupt. Write 1 to OVIIF to clear this bit and clear the interrupt and the OVIx flag. For the details, refer to the PHASES register and the EMMIE register and EMMIF register.

If OILVL[15:0] = 0000H, it will disable the overcurrent judging function.

Calculation Formula of OILVL:

$$OILVL = INT((\sqrt{2} * REGI_b * K / 2\text{^}12))$$

Where, REGIb is the total current RMS register value of the rated voltage input after the calibration, and K = the ratio of the overcurrent to the rated current for some phase. If the overcurrent is 10 times of the rated current, K = 10.

3.4.16 CF Pin Configuration Register

Address: 60H, Length: Three bytes, Default Value: 0x043210

This register CFCFG is used to configure the CF pin.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>19-23</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>16-18</td><td>CTTCfg [2:0]</td><td>Reserved.3’b100, by default.</td></tr>
<tr><td>15</td><td>CF4FConst</td><td>CF4 high frequency pulse selection.
=0, take HFCONST1 as the high frequency pulse constant.
=1, take HFCONST2 as the high frequency pulse constant.
0, by default.</td></tr>
<tr><td>12-14</td><td>CF4Cfg [2:0]</td><td>CF4 Output Pulse Control Bit.
<table>
<tr><td>Code</td><td>Description</td></tr>
<tr><td>3’b000</td><td>Total active pulse output.</td></tr>
<tr><td>3’b001</td><td>Total reactive pulse output.</td></tr>
<tr><td>3’b010</td><td>Total RMS apparent pulse output.</td></tr>
<tr><td>3’b011 (default)</td><td>Fundamental active pulse output.</td></tr>
<tr><td>3’b100</td><td>Fundamental reactive pulse output.</td></tr>
<tr><td>3’b101</td><td>Fundamental RMS apparent pulse output.</td></tr>
<tr><td>3’b110</td><td>Reserved.</td></tr>
<tr><td>3’b111</td><td>Disable the CF4 pin output pulse.</td></tr>
</table></td></tr>
<tr><td>11</td><td>CF3FConst</td><td>CF3 high frequency pulse selection.
=0, take HFCONST1 as the high frequency pulse constant.
=1, take HFCONST2 as the high frequency pulse constant.
0, by default.</td></tr>
</table>

<table>
<tr><td>8-10</td><td>CF3Cfg[2:0]</td><td>CF3 Output Pulse Control Bit.<table><tr><td>Code</td><td>Description</td></tr><tr><td>3’b000</td><td>Total active pulse output.</td></tr><tr><td>3’b001</td><td>Total reactive pulse output.</td></tr><tr><td>3’b010 (default)</td><td>Total RMS apparent pulse output.</td></tr><tr><td>3’b011</td><td>Fundamental active pulse output.</td></tr><tr><td>3’b100</td><td>Fundamental reactive pulse output.</td></tr><tr><td>3’b101</td><td>Fundamental RMS apparent pulse output.</td></tr><tr><td>3’b110</td><td>Reserved.</td></tr><tr><td>3’b111</td><td>Disable the CF3 pin output pulse.</td></tr></table></td></tr>
<tr><td>7</td><td>CF2FConst</td><td>CF2 high frequency pulse selection.
=0, take HFCONST1 as the high frequency pulse constant.
=1, take HFCONST2 as the high frequency pulse constant.
0, by default.</td></tr>
<tr><td>4-6</td><td>CF2Cfg[2:0]</td><td>CF2 Output Pulse Control Bit<table><tr><td>Code</td><td>Description</td></tr><tr><td>3’b000</td><td>Total active pulse output.</td></tr><tr><td>3’b001 (default)</td><td>Total reactive pulse output.</td></tr><tr><td>3’b010</td><td>Total RMS apparent pulse output.</td></tr><tr><td>3’b011</td><td>Fundamental active pulse output.</td></tr><tr><td>3’b100</td><td>Fundamental reactive pulse output.</td></tr><tr><td>3’b101</td><td>Fundamental RMS apparent pulse output.</td></tr><tr><td>3’b110</td><td>Reserved.</td></tr><tr><td>3’b111</td><td>Disable the CF2 pin output pulse.</td></tr></table></td></tr>
<tr><td>3</td><td>CF1FConst</td><td>CF1 high frequency pulse selection.
=0, take HFCONST1 as the high frequency pulse constant.
=1, take HFCONST2 as the high frequency pulse constant.
0, by default.</td></tr>
</table>

<table>
<tr><td>0-2</td><td>CF1Cfg[2:0]</td><td>CF1 Output Pulse Control Bit
<table>
<tr><th>Code</th><th>Description</th></tr>
<tr><td>3’b000 (default)</td><td>Total active pulse output.</td></tr>
<tr><td>3’b001</td><td>Total reactive pulse output.</td></tr>
<tr><td>3’b010</td><td>Total RMS apparent pulse output.</td></tr>
<tr><td>3’b011</td><td>Fundamental active pulse output.</td></tr>
<tr><td>3’b100</td><td>Fundamental reactive pulse output.</td></tr>
<tr><td>3’b101</td><td>Fundamental RMS apparent pulse output.</td></tr>
<tr><td>3’b110</td><td>Total active pulse output.</td></tr>
<tr><td>3’b111</td><td>Disable the CF1 pin output pulse.</td></tr>
</table></td></tr>
</table>

3.4.17 Measurement Unit Configuration Register

Address: 61H, Length: Three bytes, Default Value: 0x400000

This register EMUCFG is used to configure the measurement module.

Bit	Bit Name	Description
22-23	Reserved	Reserved.2’b01, by default.
21	EQADDMOD	All-phase sum reactive energy cumulative mode selection. = 0, Algebraic sum cumulative mode, = 1, Absolute value cumulative mode. MODSEL = 0, namely, select the three-phase four–wire system, the write function of this bit is invalid,stay 0. MODSEL = 1, namely, select the three-phase three-wire system, this bit can be configured, 0 by default.
20	EPADDMOD	All-phase sum active energy cumulative mode selection. = 0, Algebraic sum cumulative mode, = 1, Absolute value cumulative mode. MODSEL = 0, the write function of this bit is invalid, stay 0. MODSEL = 1, this bit can be configured, 0 by default.
19	ERegCAR	Energy register type section. = 0, cleared after read type. = 1, cumulative type. 0, by default.
18	ISUMMOD	Current vector sum calculation mode selection. = 0, the neutral line current doesn’t participate in the calculation. = 1, the neutral line current participates in the calculation. MODSEL = 0, the write function of this bit is invalid, stay 0. MODSEL = 1, this bit can be configured, 0 by default.
17	Reserved	Reserved.

16	NoLoadCFG	Startup mode selection. = 0, The total startup takes the total current RMS and startup threshold as the comparative judgment. = 1, The total startup takes the fundamental current RMS and startup threshold as the comparative judgment. 0, by default.
15	Reserved	Reserved
12-14	QSIGNCfg[2:0]	QC/QB/QA/FQC/FQB/FQA reactive power sign reverse selection. = 0, the reactive power sign is constant. = 1,take the complement of the reactive power, sign bit changes. 3'b000, by default.
11	Reserved	Reserved.
8-10	PSIGNCfg[2:0]	PC/PB/PA/FPC/FPB/FPA active power sign reverse selection. PSIGN0 controls phase A, PSIGN1 controls phase B, PSIGN2 controls phase C, the same as above. = 0, the active power sign is constant. = 1, take the complement of the active power, sign bit changes. 3'b000, by default.
7	Reserved	Reserved.
0-6	HPFOFF[6:0]	Sample channel {IN, IC, IB, IA, UC, UB, UA} high-pass filter enables selection bit. = 0, select the high-pass filter enable, = 1, select the high-pass filter disable. Default status = 7'b0000000, select the high-pass filter enable.

3.4.18 Measurement Control Register

Address: 62H, Length: Three bytes, Default Value: 0x000000

This register EMUCON is used to control the enable/disable of each phase (A/B/C) active/reactive/RMS apparent/fundamental active/fundamental reactive/fundamental apparent electrical energy meter.

Bit	Bit Name	Description
23	Reserved	Reserved.
20-22	FSRUN[2:0]	Enable bit of fundamental apparent meter for phase C/B/A. FSRUNx = 1, enable the fundamental electric energy apparent meter of this phase, and participates in the calculation for all-phase sum. FSRUNx = 0, disable the fundamental electric energy apparent meter of this phase, and doesn't participate in the calculation for

		all-phase sum. Default 3'b000.
19	Reserved	Reserved.
16-18	FQRUN[2:0]	Enable bit of fundamental reactive meter for phase C/B/A. FQRUNx = 1, enable the fundamental reactive electrical energy meter of this phase, and this phase participates in the calculation for the all-phase sum. FQRUNx = 0, disable the fundamental reactive electrical energy meter of this phase, and this phase doesn't participate in the calculation for the all-phase sum. The default status is 3'b000.
15	Reserved	Reserved.
12-14	FPRUN[2:0]	Enable bit of fundamental active meter for phase C/B/A. FPRUNx = 1, enable the fundamental active electrical energy meter of this phase, and participates in the calculation for all-phase sum. FPRUNx = 1, disable the fundamental active electrical energy meter of this phase, and this phase doesn't participate in the calculation for the all-phase sum. Default 3'b000.
11	Reserved	Reserved.
8-10	SRUN[2:0]	Enable bit of apparent meter for phase C/B/A. SRUNx = 1, enable the apparent electrical energy meter of this phase, and participates in the calculation for the all-phase sum. SRUNx = 0, disable the apparent electrical energy meter of this phase, and doesn't participate in the calculation for the all-phase sum. Default 3'b000.
7	Reserved	Reserved.
4-6	QRUN[2:0]	Enable bit of reactive meter for phase C/B/A. QRUNx = 1, enable the reactive electrical energy meter of this phase, and participates in the calculation for the all-phase sum. QRUNx = 0, disable the reactive electrical energy meter of this phase, and doesn't participate in the calculation for the all-phase sum. Default 3'b000.
3	Reserved	Reserved.
0-2	PRUN[2:0]	Enable bit of active meter for phase C/B/A.PRUN0 controls phase A, PRUN1 controls phase B, and PRUN2 controls phase C. This bit has no effect on the calculation of the power and RMS, but has an effect on the measuring of the active electric

		energy for the per-phase and all-phase sum. Ditto. PRUNx = 1, enable the active electrical energy meter of this phase, and this phase participates in the calculation for the all-phase sum. PRUNx = 0, disable the active electrical energy meter of this phase, and this phase doesn't participate in the calculation for the all-phase sum. Default 3'b000.

3.4.19 Sample data Write Buffer Control Register

Address: 63H, Length: One byte, Default Value: 00H

This register WSAVECON controls whether it writes buffer each channels ADC data, how to arrange in the buffer area, buffer size and the waveform sample rate, which are defined by the register as follows:

Bit	Bit Name	Description
7	Reserved	Reserved.
6	WFreqSEL	= 0, for the baseband 50HZ sample and 8.192Mhz crystal oscillation, the sample rate is 6.4Khz. = 1, for the baseband 60HZ sample and 8.192Mhz crystal oscillation, the sample rate is 7.699KHz.

<table>
<tr><td>4-5</td><td>WSCOMM[1:0]</td><td>= 2’b00 or 2’b11, no operation,
= 2’b01, the buffer area is cleared.
= 2’b10, Start to write waveform data to buffer area according to the Configure of BUFCFG[3:0].
<table>
<tr><th>WBUFCOM[1:0]</th><th>Command or Status</th></tr>
<tr><td>2’b00</td><td>Write 2’b00 is invalid, no operation (default).
Reading 2’b00, the buffer area is idle, or write operation is completed, and it can implement the read operation.
It is idle by default after reset.</td></tr>
<tr><td>2’b01</td><td>Buffer area clear command. The whole BUF is cleared within 20ms after configure this command.</td></tr>
<tr><td>2’b10</td><td>Start to write waveform data to buffer area according to the Configure of BUFCFG[3:0].</td></tr>
<tr><td>2’b11</td><td>Write 2’b11 is invalid, no operation.
Reading 2’b11 indicates the buffer area response command, it is in the write operation (clear or write data), write operation is invalid in this busy state.</td></tr>
</table></td></tr>
<tr><td>0-3</td><td>BUFCFG[3:0]</td><td>ADC Data Buffer Configuration:
Determine whether each channel ADC data is written into buffer and the address mapping of ADC data. Shown in table below.</td></tr>
</table>

When WSCOMM[1:0] is written into 2’b01, RN8302B responds to clear buffer command, WBUFCOMM = 2’b11, BUF starts to clear. During the clear, doesn’t respond to the new command. After 20ms, the whole BUF is cleared, WBUFCOMM = 2’b00.

When WSCOMM[1:0] is written into 2’b10, RN8302B responds to start buffer command, WBUFCOMM = 2’b11, the data starts to write into the buffer according to the BUFCFG[0:3] configuration. During the write, doesn’t respond to the new command. When the buffer is full, stop write, and WBUFCOMM = 2’b00.

After the start buffer command, the bits of the BUFCFG[3:0] determines whether each channels ADC data writes into the buffer and the address mapping in the buffer. There are 768 address units in the buffer with the address 200H-4FFH as shown below.

Address Mapping	BANK	BUFCFG[3:0]											
		4'b0000r11x	4'b0001	4'b0010	4'b0011	4'b0100	4'b0101	4'b0110	4'b0111	4'b1000	4'b1001	4'b1010	4'b1011

		x											
200H 27FH	BANK2	UA	UA	IA	UA	UB	UC	UA	UB	UC	IA	IB	IC
280H 2FFH	BANK2	UB											
300H 37FH	BANK3	UC	UB	IB	IA	IB	IC						
380H 3FFH	BANK3	IA											
400H 47FH	BANK4	IB	UC	IC									
480H 4FFH	BANK4	IC											

3.4.20 EMMIE and IF Register

EMMIE Register

Address: 64H, Length: Two bytes, Default Value: 0000H

This register is the interrupt enable register in the EMM mode. Corresponding interrupt enable bit is configured to 1 and IF is cleared in the EMM mode. When this event has occurred, the INTN pin outputs the low level.

Bit	Bit Name	Description
15	OVIIE	Overvoltage and overcurrent interrupt enable. = 1, enable. = 0, disable. Default 0. The same below.
14	SAGIE	Voltage sag interrupt enable.
13	IRegion3IE	Current piecewise status change interrupt enable.
12	Reserved	Reserved.
11	CF4IE	CF4 pulse output interrupt enable.
10	CF3IE	CF3 pulse output interrupt enable.
9	CF2IE	CF2 pulse output interrupt enable.
8	CF1IE	CF1 pulse output interrupt enable.
7	ZXINIE	Channel IN forward zero-crossing interrupt enable.
6	ZXICIE	Channel IC forward zero-crossing interrupt enable.

5	ZXIBIE	Channel IB forward zero-crossing interrupt enable.
4	ZXIAIE	Channel IA forward zero-crossing interrupt enable.
3	ZXUCIE	Channel UC forward zero-crossing interrupt enable.
2	ZXUBIE	Channel UB forward zero-crossing interrupt enable.
1	ZXUAIE	Channel UA forward zero-crossing interrupt enable.
0	WAVUDIE	Sample waveform interrupt enable.

EMMIF Register

Address: 65H, Length: Two bytes

This register is the event status register in the EMM mode. Corresponding IF bit is set to 1 in the EMM mode when some event occurs. When corresponding interrupt enable bit is configured to 1, setting the status bit to 1 will cause the INTN pin outputs the low level.

Bit	Bit Name	Description
15	OVIIF	Overvoltage and overcurrent interrupt flag. =1,some phase is overvoltage or overcurrent,If OVIE = 1, it will cause the INTN pin turn from high to low. Write 1 to clear this bit, clear interrupt and the OVUA, OVUB, OVUC, OIIA, OIIB and OIIC status flag bits in PHASES status register.
14	SAGIF	Voltage sag interrupts flag. =1,some phase voltage sags,.If the SAGIE = 1, it will cause the INTN pin turn from high to low. Write 1 to clear this bit, clear the interrupt and the SAGUA, SAGUB and SAGUC status flag bits in PHASES status register.
13	IRegion3IF	Piecewise status change flag of current piecewise 3. Three-phase four-wire: When any phase of current RMS for three phases A/B/C changes compared to the piecewise status set by IRegion3H/IRegion3L, this bit is set to 1. Three-phase three-wire: When any phase of current RMS for phase A/C changes compared to the piecewise status set by IRegion3H/IRegion3L, this bit is set to 1. Query the IregionS register further, to confirm which phase of current RMS piecewise status changes. If the IRegion3IE = 1, it will cause INTN pin turn from high to low. Write 1 to clear this bit,,and clear the interrupt.
12	Reserved	Reserved.
11	CF4IF	CF4 pulse output flag. Write 1 to clear.If CF4IE = 1, clear the interrupt simultaneously.
10	CF3IF	CF3 pulse output flag. Write 1 to clear.If CF3IE = 1, clear the interrupt simultaneously.
9	CF2IF	CF2 pulse output flag.

		Write 1 to clear.If CF2IE = 1, clear the interrupt simultaneously.
8	CF1IF	CF1 pulse output flag. Write 1 to clear.If CF1IE = 1, clear the interrupt simultaneously.
7	ZXINIF	The channel IN forward zero-crossing flag. Write 1 to clear. If ZXINIE = 1, clear the interrupt simultaneously.
6	ZXICIF	The channel IC forward zero-crossing flag. Write 1 to clear. If ZXINIE = 1, clear the interrupt simultaneously.
5	ZXIBIF	The channel IB forward zero-crossing flag. Write 1 to clear. If ZXIBIE = 1, clear the interrupt simultaneously.
4	ZXIAIF	The channel IA forward zero-crossing flag. Write 1 to clear. If ZXIAIE = 1, clear the interrupt simultaneously.
3	ZXUCIF	The channel UC forward zero-crossing flag. Write 1 to clear. If ZXUCIE = 1, clear the interrupt simultaneously.
2	ZXUBIF	The channel UB forward zero-crossing flag. Write 1 to clear. If ZXUBIE = 1, clear the interrupt simultaneously.
1	ZXUAIF	The channel UA forward zero-crossing flag. Write 1 to clear. If ZXUAIE = 1, clear the interrupt simultaneously.
0	WAVUDIF	Waveform sample flag.8Khz refresh rate. Write 1 to clear. If WAVUDIE = 1, clear interrupt simultaneously.

3.4.21 Power Orientation Register

Address: 66H, Length: Two bytes

The PQSign register is the total active/total reactive/fundamental active/fundamental reactive orientation register. The orientation takes per-phase and the all-phase sum average power signs as the criterion, and is updated with the average power register synchronously with the update cycle 250ms.

Bit	Bit Name	Description
15	FQTSIGN	= 0, the fundamental all-phase sum reactive sign is ＋. = 1, the fundamental all-phase sum reactive sign is －.
14	FQCSIGN	= 0, the fundamental phase C reactive sign is ＋. = 1, the fundamental phase C reactive sign is －.
13	FQBSIGN	= 0, the fundamental phase B reactive sign is ＋. = 1, the fundamental phase B reactive sign is －.
12	FQASIGN	= 0, the fundamental phase A reactive sign is ＋. = 1, the fundamental phase A reactive sign is －.
11	FPTSIGN	= 0, the fundamental all-phase sum active sign is ＋. = 1, the fundamental all-phase sum active sign is －.
10	FPCSIGN	= 0, the fundamental phase C active sign is ＋. = 1, the fundamental phase C active sign is －.
9	FPBSIGN	= 0, the fundamental phase B active sign is ＋.

		= 1, the fundamental phase B active sign is －.
8	FPASIGN	= 0, the fundamental phase A active sign is ＋. = 1, the fundamental phase A active sign is －.
7	QTSIGN	= 0, the all-phase sum reactive sign is ＋. = 1, the all-phase sum reactive sign is －.
6	QCSIGN	= 0, phase C reactive sign is ＋. = 1, phase C reactive sign is －.
5	QBSIGN	= 0, phase B reactive sign is ＋. = 1, phase B reactive sign is －.
4	QASIGN	= 0, phase A reactive sign is ＋. = 1, phase B reactive sign is －.
3	PTSIGN	= 0, the all-phase sum active sign is ＋. = 1, the all-phase sum active sign is －.
2	PCSIGN	=0, phase C active sign is ＋. =1, phase C active sign is －.
1	PBSIGN	=0, phase B active sign is ＋. =1, phase B active sign is －.
0	PASIGN	=0, phase A active sign is ＋. =1, phase A active sign is －.

3.4.22 No-load Status Flag Register

Address: 67H, Length: Two bytes

The Noload register indicates the total active apparent/total reactive/fundamental active apparent/fundamental reactive no-load status of each phase. This register combines with the IStart_PS and IStart_Q register, and the bit NoLoadCFG (EMUCFG.16). The update cycle of this register is 250ms.

Bit	Bit Name	Description
15	Reserved	Reserved
14	FNoQldC	= 0, phase C fundamental reactive power is not no-load. = 1, phase C fundamental reactive power is no-load.
13	FNoQldB	= 0, phase B fundamental reactive power is not no-load. = 1, phase B fundamental reactive power is no-load.
12	FNoQldA	= 0, phase A fundamental reactive power is not no-load. = 1, phase A fundamental reactive power is no-load.
11	Reserved	Reserved
10	FNoPSldC	= 0, phase C fundamental active and apparent power are not no-load. = 1, phase C fundamental active and apparent power are no-load.
9	FNoPSldB	= 0, phase B fundamental active and apparent power are not no-load.

		= 1, phase B fundamental active and apparent power are no-load.
8	FNoPSldA	= 0, phase A fundamental active and apparent power are not no-load. = 1, phase A fundamental active and apparent power are no-load.
7	Reserved	Reserved
6	NoQldC	= 0, phase C reactive power is not no-load. = 1, phase C reactive power of is no-load.
5	NoQldB	= 0, phase B reactive power is not no-load. = 1, phase B reactive power of is no-load.
4	NoQldA	= 0, phase A reactive power is not no-load. = 1, phase A reactive power of is no-load.
3	Reserved	Reserved
2	NoPSldC	= 0, phase C active and apparent power are not no-load. = 1, phase C active and apparent power are no-load.
1	NoPSldB	= 0, phase B active and apparent power are not no-load. = 1, phase B active and apparent power are no-load.
0	NoPSldA	= 0, phase A active and apparent power are not no-load. = 1, phase A active and apparent power are no-load.

3.4.23 Current Piecewise Status Register

Address: 68H, Length: One byte

The IRegionS register indicates the piecewise status of each per-phase currents. This register combines with the current piecewise region setting register IRegionL and IRegionH, as well as IRegionIE and IRegionIF. The update cycle of this register is 250ms.

Bit	Bit Name	Description
3-7	Reserved	Reserved
2	Iregion3SC	= 0, phase C current RMS is in the piecewise region 1. = 1, phase C current RMS is in the piecewise region 2.
1	Iregion3SB	= 0, phase B current RMS is in the piecewise region 1. = 1, phase B current RMS is in the piecewise region 2.
0	Iregion3SA	= 0, phase A current RMS is in the piecewise region 1. = 1, phase A current RMS is in the piecewise region 2.

3.4.24 Phase Voltage and Current Status Register

Address: 69H, Length: One byte

The PHASES register indicates the status of the phase loss of voltage, phase sequence error, voltage sag, overvoltage, and the phase overcurrent status. This register combines with the register and register bit LostVoltage, MODSEL (three-phase four-wire and

three-phase three-wire voltage sequence error criterion are different), SAGCFG, OVLVL, OILVL, SAGIE, SAGIF, OVIIE and OVIIF.

Bit	Bit Name	Description
15	Reserved	Reserved
14	OIIC	= 0, IC is not overcurrent. = 1, IC is overcurrent. When write 1 to clear OVIIF, it will clear this bit simultaneously.The same as OIIB,OIIA,OVUC,OVUB,OVUA.
13	OIIB	= 0, IB is not overcurrent. = 1, IB is overcurrent.
12	OIIA	= 0, IA is not overcurrent. = 1, IA is overcurrent.
11	Reserved	Reserved
10	OVUC	= 0, UC is not overvoltage. = 1, UC is overvoltage.
9	OVUB	= 0, UB is overvoltage. = 1, UB is not overvoltage.
8	OVUA	= 0, UA is overvoltage. = 1, UA is not overvoltage.
7	Reserved	Reserved
6	SAGUC	= 0, UC is not voltage sag. = 1,UC is voltage sag. When write 1 to clear SAGIF, it will clear this bit simultaneously.The same as SAGUB,SAGUA.
5	SAGUB	= 0, UB is not voltage sag. = 1, UB is voltage sag.
4	SAGUA	= 0,UA is not voltage sag. = 1,UA is voltage sag.
3	UPhSqErr	= 0, voltage phase sequence is normal. = 1,voltage phase sequence is error. Criterion of Three-phase Four-wire: ① YUBUA is out of 120°±10°, ② YUCUA is out of 240°±10°, ③ UA < ZXOT (normalized value, the same below), ④ UB < ZXOT, ⑤ UC < ZXOT. If any of above conditions has occurred, it judges the three-phase four-wire voltage phase sequence is error. Criterion of Three-phase three-wire: ① YUCBUAB is out of 300°±10°, ② UAB < ZXOT,

		③ UCB < ZXOT. If any of above conditions has occurred, it judges the three-phase three-wire voltage phase sequence is error.
2	LostVoltSC	= 0, the high 16-bit of the total Voltage RMS UC≥ the threshold of LostVoltage (0x04) , phase C is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UC＜the threshold of LostVoltage (0x04) , phase C is loss of voltage.
1	LostVoltSB	= 0, the high 16-bit of the total Voltage RMS UB≥ the threshold of LostVoltage (0x04) ,phase B is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UB ＜the threshold of LostVoltage (0x04) ,phase B is loss of voltage.
0	LostVoltSA	= 0, the high 16-bit of the total Voltage RMS UA≥ the threshold of LostVoltage (0x04), phase A is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UA＜the threshold of LostVoltage (0x04) ,phase A is loss of voltage.

3.4.25 Checksum Register 1

Address: 6AH, Length: 3 bytes

CHECKSUM1 is the checksum register of the meter module configuration register. The checksum calibration address range is BANK1 EMM calibration register and EMM configuration register 00H-62H.The checksum algorithm is the negated sum of three bytes. If the register length is not enough three bytes, supplement it by zero.

3.4.26 NVM1CFG Register

Address: 70H, Length: 1 byte, Default Value: 0x01.

The NVM1CFG register is used to configure the interrupt enable in the NVM1 mode.

Bit	Bit Name	Description
1-7	Reserved	Reserved
0	NVM1IE	The NVM1 no-voltage RMS measurement interrupt enable.= 1, enable.= 0, disable. It is enabled by default. This interrupt is valid in the NVM1 mode only.

3.4.27 NVM1IF Register

Address: 71H, Length: 1 byte

The NVM1IF register is the NVM1 mode status flag bit.

Bit	Bit Name	Description
1-7	Reserved	Reserved

0	NVM1Done	The NVM1 interrupt flag. The RN8302B receives and responds to GONVM1 command in other modes and the mode is switched successfully,this bit is set to 1. Cleared once the following situation has occurred: ① Cleared after read, ② Cleared when switch to other mode from NVM1. If NVM1IE=1, setting this bit to 1 will cause the interrupt, and INTN will turn from high to low. It will clear the interrupt and INTN is reset to the high level when this bit is cleared,. Default 0, after power-up reset .

3.4.28 NVM2CFG Register

Address: 72H, Length: 2 bytes, Default Value: 0x0F21.

The NVM2CFG register is used to configure the NVM2 mode.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>13-15</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>8-12</td><td>NVM2TNUM [4:0]</td><td>Comparison cycles configuration of the NVM2 current comparison unit.
Cycles = NVM2NUM[4:0]+1,
Default 5’b01111, indicates the comparison cycles are 16 cycles.</td></tr>
<tr><td>6-7</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>4,5</td><td>NVM2TH[1:0]</td><td>NVM2 Comparator Level Setting.
<table>
<tr><th>Code</th><th>Description</th></tr>
<tr><td>2’b00</td><td>Reserved</td></tr>
<tr><td>2’b01</td><td>Comparator level 1, 50mV typical application of current sample Ib</td></tr>
<tr><td>2’b1x (default)</td><td>Comparator level 2, 100mV typical application of current sample Ib</td></tr>
</table></td></tr>
<tr><td>3</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>2</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>1</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>0</td><td>NVM2IE</td><td>NVM2 no-voltage judgment interrupt enable.
= 1, enable.
= 0, disable,
1 default. Valid in the NVM2 mode only.</td></tr>
</table>

3.4.29 NVM2CMP Register

Address: 73H - 75H, Length: 2 bytes, Default Value: 0x0256.

Including: Three registers NVM2CMP A/B/C. It is used for three comparator output processing of NVM2.The default value is 0x0256.Must be initialized as 0x0000 before the normal use.

3.4.30 NVM2IF Register

Address: 76H, Length: 1 byte

NVM2 mode status flag register. Valid in the NVM2 mode only.

Bit	Bit Name	Description
7	CMPC	NVM2 phase C current comparison result. = 1, phase C current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase C current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0]. This bit and CMPB,CMPA,CMP are updated when NVM2DONE is set to 1.
6	CMPB	NVM2 phase B current comparison result. = 1, phase B current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase B current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0].
5	CMPA	NVM2 phase A current comparison result. = 1, phase A current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase A current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0].
4	CMP	NVM2 three-phase current comparison result. = 1, three phase currents are greater than the level configured in NVM2TH[1:0]] within the cycles configured in NVM2TNUM[4:0]. = 0, at least one of three phase currents is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0].
1-3	Reserved	Reserved
0	NVM2Done	NVM2 current comparison end flag.

		Be set to 1 after start up and complete the NVM2 comparison for one time. Meantime, CMP/CMPA/CMPB/CMPC are updated. Cleared once the following situation has occurred, ① Cleared after the read, ② Cleared when switch to other modes (SLM/NVM1/EM) from NVM2 or switch to NVM2 from other modes. =1 will cause INT interrupt when NVM2IE = 1 in NVM2CFG,. When this bit is cleared ,the interrupt is cleared, and INTN is set back high.

3.4.31 Write Enable Register

Address: 80H, Length: 1 byte, Default Value: 0x00.

This register is used to readable and writeable register write protection command.It is the default write protection status after power-up reset and the software reset.

Command	Command Word	Description
WREN	0xE5	Write enable command. After the write enable is valid, all R/W registers are Write Enabled. This register is read as 0x01.
WRDIS	0xDC	The write protection command. After the write protection is valid, all R/W registers are write protection. This register is read as 0x00.
	Others	Reserved.

3.4.32 Operating Mode Switching Register

Address: 81H, Length: 1 byte

This register is used to configure the operating mode. The initial value of this register after the power-up reset reflects the default operating mode after the reset determined by the pin PM. PM = 1, the initial value is 0x03. PM = 0, the initial value is 0x01.After the mode switching, this register value is the current operating mode flag.

Command	Command Word	Description
GOSLM	0x18	If the system is in EMM/NVM1/NVM2 mode and register is write enable, receiving and responding to this command will switch to SLM. After the mode switching is completed, this register = 2'b11. Meantime, WMS[1:0] = 2'b11 in SYSSR (0x8A). Receiving this command in SLM mode,not activated.
GONVM2	0x5C	If the system is in SLM/EMM/NVM1 mode and register is

		write enable, receiving and responding to this command will switch to NVM2 and complete the criterion of the NVM2 current comparison for one time. After the mode switching is completed, this register = 2'b10. Meantime, WMS[1:0] = 2'b10 in SYSSR (0x8A). After the criterion of the current comparison is completed, NVM2DONE=1 in the NVM2IF register. Receiving this command in NVM2 mode,not activated.
GONVM1	0xE1	If the system is in SLM/NVM2 mode and register is write enable, receiving and responding to this command will cause to generate the wake-up reset, then switch to NVM1 mode and start NVM1 current RMS calculation after the reset. If the system is in EMM mode, receiving and responding to this command will switch to NVM1 mode, and start NVM1 current RMS calculation. After the mode switching is completed, this register = 2'b00. Meantime, WMS[1:0] = 2'b00 in SYSSR (0x8A). NVM1Done in the NVM1IF register is set to 1 after 450ms. Receiving this command in NVM1 mode,not activated.
GOEMM	0xA2	If the system is in SLM/NVM2 mode and register is write enable, receiving and responding to this command will cause to generate the wake-up reset, and then switch to EMM mode and start all functions in EMM mode after the reset. If the system is in NVM1 mode, receiving and responding to this command will switch to EMM mode, and start all functions in EMM mode. After the mode switching is completed, this register = 2'b01. Meantime, WMS[1:0] = 2'b01 in SYSSR (0x8A). Receiving this command in EMM mode,not activated.
--	Others	Reserved.

3.4.33 Software Reset Register

Address: 82H, Length: 1 byte, Default Value: 0x00.

Command	Command Word	Description
SOFTRST	0xFA	Software reset command. Writing this command will cause the software reset when the register is write enable.

		After software reset, this register value is reset to 0x00.
	Others	Reserved.

3.4.34 ADC Configuration Register

Address: 83H, Length: 2 bytes, Default Value: 0x0000.

The ADCCFG register is used to configure seven ADCs.

Bit	Bit Name	Description
15	Reserved	Reserved.
14	REFSEL	The ADC reference voltage selection. = 0, select on-chip reference voltage as reference voltage of ADC. = 1, select external REF as reference voltage of ADC. 0, by default.
12,13	PGAIN[1:0]	PGA gain for IN.
10,11	PGAIC[1:0]	PGA gain for IC.
8,9	PGAIB[1:0]	PGA gain for IB.
6,7	PGAIA[1:0]	PGA gain for IA.
4,5	PGAUC1:0]	PGA gain for UC.
2,3	PGAUB[1:0]	PGA gain for UB.
0,1	PGAUA1:0]	PGA gain for UB.. = 2'b00, 1X. = 2'b01, 2X. = 2'b10, 4X. = 2'b11, 8X. 2'b00 by default.Ditto.

3.4.35 Three-phase Four-wire/Three-phase Three-wire Mode Selection Register

Address: 86H, Length: 1 byte, Default Value: 0x00.

The MODSEL register is used to select the three-phase four-wire and three-phase three-wire mode.

Register	Value	Description
MODSEL	0x33	Three-phase three-wire mode enable. Select three-phase three-wire. After it is valid, read as 0x01.
	0x00 (default)	Three-phase four-wire mode enable. Default value. Select three-phase four-wire. After it is valid, read as 0x00.
	Others	Reserved.

3.4.36 System Status Register

Address: 8AH, Length: 2 bytes

The SYSSR register is used to reflect the operating status of RN8302B.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15-14</td><td>WMS[1:0]</td><td>The operating mode status bit.
<table>
<tr><td>WMS[1:0]</td><td>Description</td></tr>
<tr><td>2’b 11</td><td>Current operating mode is SLM.</td></tr>
<tr><td>2’b 10</td><td>Current operating mode is NVM2.</td></tr>
<tr><td>2’b 01</td><td>Current operating mode is EMM.</td></tr>
<tr><td>2’b 00</td><td>Current operating mode is NVM1.</td></tr>
</table></td></tr>
<tr><td>13</td><td>PM1</td><td>PM pin status bit.
= 1, the PM pin inputs is high.
= 0, the PM pin inputs is low.</td></tr>
<tr><td>12</td><td>Reserved</td><td>It is always 1.</td></tr>
<tr><td>11</td><td>MODSEL</td><td>The three-phase three-wire/three-phase four-wire mode status bit.
= 1, the system is in the three-phase three-wire mode.
= 0, the system is in the three-phase four-wire mode.</td></tr>
<tr><td>10</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>9</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>8</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>7</td><td>REG_WE</td><td>Write Enable flag.
=1, the configuration register is write enable.
=0. the configuration register is write protection.</td></tr>
<tr><td>6</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>5</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>4</td><td>WKR_FLAG</td><td>Wake-up reset flag.
=1,the NVM2 or SLM mode is switched to EMM or NVM1, or the power-up reset default mode is EMM or NVM1.
During the reset, this bit is 0. Cleared after read.</td></tr>
<tr><td>3</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>2</td><td>SRST_FLAG</td><td>Software reset flag.
During the software reset, =0.
When the software reset is completed, =1.
Cleared after read, and cleared after the power-up and power-down reset.</td></tr>
<tr><td>1</td><td>RSTN_FLAG</td><td>External pin reset flag.
When the external pin reset is complete, =1.
Cleared after read, and Cleared after the power-up and</td></tr>
</table>

		power-down reset.
0	PWROK_FLAG	3.3V power supply monitoring reset flag. When the 3.3V power-up and power-down is completed, =0. Cleared after read.

3.4.37 Checksum Register 2

Address: 8BH, Length: 2 bytes

The CHECKSUM2 register is the checksum of NVM1, NVM2 and system configuration register. The calculation address range of the checksum includes NVM1, NVM2 and system configuration register 70H, 72H-75H, 83H-86H.The checksum algorithm is the negated sum of three bytes. If the register length is not enough three bytes, supplement it by zero.

3.4.38 SPI Read Check Register

Address: 8CH, Length: 4 bytes

The RData register saves the data read by SPI last time and can be used for the check when SPI reads the data. When the register length read by SPI last time is less than 4 bytes, align the low-bit byte. For example, after it reads the 3-byte register DeviceID, this register is read as 0x00830200.

3.4.39 SPI Write Check Register

Address: 8DH, Length: 3 bytes

The WData register saves the data written by SPI last time and can be used for the check when SPI writes the data. When the register length written by SPI last time is less than 3 bytes, align the low-bit byte.

3.4.40 Waveform Buffer Address Register

Address: 8EH, Length: 2 bytes

The LRBufAddr register indicates the address of the last waveform buffer data when SPI reads the waveform buffer data.

For example, after read the waveform buffer in BURST for one time, this register points to the address that read the buffer last time. When the last read data address out of limit, namely, >4FFH, the LRBufAddr register will not be processed specially, but it still saves the out of limit address.

3.4.41 DeviceID Register

Address: 8FH, Length: 3 bytes
The DeviceID number of RN8302B, which is always 830200H after power-up.

3.5 Reset and Mode Switching

3.5.1 Power-up and Power-down Reset

PM Pin	Mode After Reset	Register
0	EMM	1. All registers are reset. 2. Enable the EMM function, and disable the NVM1 and NVM2 function after the reset.
1	SLM	1. The NVM1 configuration and status register, NVM2 configuration and status register and system configuration and status register are reset. 2. The parameter register, EMM calibration register and EMM configuration and status register are invalid.

3.5.2 External Pin Reset

Operating Mode Before Reset	Operating Mode After Reset	Register
EMM	EMM	1. NVM1CFG, NVM1CMPA, NVM1CMPB and NVM1CMPC (hereafter short for NVM1 configuration register) remain constant. 2. The NVM2 configuration register NVM2CFG remains constant. 3. The system configuration register WREN, ADCCFG and MODSEL remain constant. 4. Other registers are reset.
NVM1	NVM1	Ditto.
NVM2	NVM2	1. The NVM1 configuration register, NVM2 configuration register and system configuration register WREN, ADCCFG and MODSEL remain constant. 2. Enable the NVM2 current comparison functions for one time and refresh the NVM2IF register after the reset.

		3. The parameter register, EMM calibration register and EMM configuration and status register remain inactive. 4. Other registers are reset.

3.5.3 Software Reset

Operating Mode Before Reset	Operating Mode After Reset	Register
EMM	EMM	1. The NVM1 configuration register, NVM2 configuration register and system configuration register ADCCFG and MODSEL remain constant. 2. Other registers are reset, including WREN.
NVM1	NVM1	Ditto.
NVM2	NVM2	1. The NVM1 configuration register, NVM2 configuration register and system configuration register ADCCFG and MODSEL remain constant. 2. Enable the NVM2 current comparison functions for one time and refresh the NVM2IF register after the reset. 3. The parameter register, EMM calibration register and EMM configuration and status register remain inactive. 4. Other registers are reset, including WREN.

3.5.4 Mode Switching and Register

Current Operating Mode	Mode Switching Command	Operating Mode After Switching	Register Change
SLM or NVM2	GOEMM	EMM	1. The wake-up reset occurrs, and the parameter register, EMM calibration register and EMM configuration and status register are reset. 2. Enable the EMM function, and disable the NVM1 and NVM2 function after the reset. The NVM1 RMS remains the reset value. 3. The SYSSR register, operating mode switching register and NVM2IF change correspondingly.

			4. Other registers remain constant.
	GONVM1	NVM1	1. The wake-up reset occurrs, and the parameter register, EMM calibration register and EMM configuration and status register are reset. 2. Enable the NVM1 current RMS measurement function and refresh the NVM1 current RMS register after the reset. The EMM function is disabled, and the EMM parameter register and status register remain the reset value. 3. The SYSSR register, operating mode switching register and NVM2IF change correspondingly. 4. Other registers remain constant.
EMM or NVM1	GOSLM	SLM	1. The parameter register, EMM calibration register and EMM configuration and status register are invalid. 2. The SYSSR register, operating mode switching register and NVM1IF register change correspondingly. 3. Other registers remain constant.
EMM or NVM1	GONVM2	NVM2	1. The parameter register, EMM calibration register and EMM configuration and status register are invalid. 2. Enable the NVM2 current comparison functions for one time and refresh the NVM2IF register. 3. The SYSSR register, operating mode switching register and NVM1IF register change correspondingly. 3. Other registers remain constant.
EMM	GONVM1	NVM1	1. The EMM calibration register and EMM configuration and status register are invalid, but remain the value before the switching. 2. Enable the NVM1 current RMS measurement function and refresh the NVM1 current RMS register. The EMM function is invalid. However, the EMM parameter register remains the value before the switching. 3. The SYSSR register, operating mode switching register and NVM1IF register change correspondingly. 4. Other registers remain constant.
NVM1	GOEMM	EMM	1. Enable the EMM function. The EMM calibration

			register and EMM configuration register are valid, and the EMM parameter register and EMM status register start to refresh. 2. Disable the NVM1 current RMS measurement function. However, the NVM1 current RMS register remains the value before the switching. 3. The SYSSR register and operating mode switching register change correspondingly. 4. Other registers remain constant.
NVM2	GOSLM	SLM	1. The parameter register, EMM calibration register and EMM configuration and status register are invalid. 2. The SYSSR register, operating mode switching register and NVM2IF register change correspondingly. 3. Other registers remain constant.
SLM	GONVM2	NVM2	1. The parameter register, EMM calibration register and EMM configuration and status register are invalid. 2. Enable the NVM2 current comparison functions for one time and refresh the NVM2IF register. 3. The SYSSR register and operating mode switching register change correspondingly. 4. Other registers remain constant.

3.6 Write Protection

In addition to the write enable register, all R/W registers and command registers perform the write protection function.

The default state of the R/W registers after the power-up reset and the software reset is the write protection status. Disable the write protection after the write enable register receives the WREN command. Enable the write protection after it receives the WRDIS command.

The REG_W status bit in the SYSSR register reflects the write protection status.

4 Calibration Method

4.1 General Description

The RN8302B provides abundant calibration means to implement the software calibration, and supports both the power calibration method and the traditional pulse calibration method. For the calibrated instrument, the active and reactive accuracy are up to grade 0.2S.The calibration means of RN8302B include as follows:

- The EC can be adjusted by the HFConst register.
- ADC sample channel gain calibration
- ADC sample channel phase calibration. Of which, the three current channels support the piecewise phase calibration.
- Active, reactive and apparent power gain calibration
- Active and reactive power phase calibration
- Active and reactive power and RMS Offset calibration
- Automatic checksum of the calibration data is provided.

4.2 Power Calibration Method

Compared to the traditional pulse calibration method, the power calibration method is simple and quick. The calibration system is shown in figure, and it is only necessary to provide a high accuracy program controlled power source The accuracy of program controlled power source shall be higher than the level required by Meter Under Calibration(MUC).

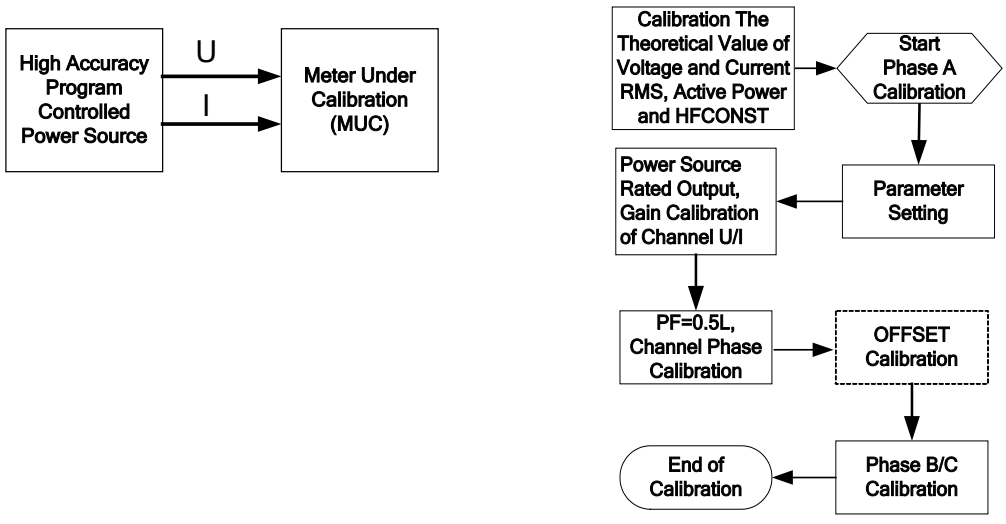


Figure4-1 Calibration Flow

4.2.1 Calibration Flow

The power calibration flow is shown as follows:

1. Calculate the standard U and I register value for the rated input, and calculate the standard active power when PF=1.0 and PF=0.5L, and calculate HFConst of RN8302B according to the EC.
2. Establish the calibration environment and configure the parameters according to the drawing. For example, configure the ADC PGA gain, HFConst and threshold register.
3. For the program controlled power source rated output, read the actual voltage and current RMS of phase A, and calculate the error related to the theoretical value, fill in and compare with the calibrated result, and complete the U and I channel gain calibration of phase A.
4. For the program controlled power source PF=0.5L and rated output, read the active power of phase A, calculate the error related to the theoretical value, calculate the value of the channel phase register according to this error, fill in and compare with the calibrated result, and complete the channel phase calibration of phase A.
5. If the program controlled power source current is no-load, read the no-load RMS and power value, calculate corresponding OFFSET value according to the no-load value, and fill in corresponding OFFSET register value. Complete the OFFSET calibration of phase A (this item is optional).
6. Calibrate the gain, phase and OFFSET of other phases in the same way.
7. The calibration is completed.

4.2.2 Calculation of Standard Voltage/Current and Active Power Value

1. Calculation and Selection of Standard Voltage RMS Register Value

For the rated voltage input, the standard voltage RMS register value shall facilitate MCU to convert into the LCD display value, and within the rational range of the channel gain calibration.

Assume the rated voltage input Un, the voltage RMS at the input pin of the voltage channel is Vu, the theoretical calculation value is U_{theory}, the LCD display value after the MCU conversion is $U_{indicative}$, and the standard voltage RMS register value is $U_{standard}$, then the selection of $U_{standard}$ shall meet the following conditions:

$0.8 < U_{standard}/U_{theory} < 1.2$

$K= U_{standard}/U_{indicative}$, K shall be the integer and facilitate the MCU conversion.

Above first condition ensures the U channel gain calibration is within the rational range, the selection of the second condition K shall facilitate MCU to convert the RMS register value into the LCD display value. If PGA=1, U_{theory} can be calculated by the following formula:

$$U_{thoery}=INT[(Vu/800)*2^{27}]$$

2. Calculation and Selection of Standard Current RMS Register Value

When calculate the rated current input by the same principle, the standard current RMS register value $I_{standard}$.

3. Calculate Standard Active Power Register Value for PF=1.0 and PF=0.5L

For the rated input and PF=1.0, the standard active power value $P = INT(U_{standard} * I_{standard}/2^{23})$.

For the rated input and PF=0.5L, the standard active power value $P_{0.5L} = INT(U_{standard} * I_{standard}/2^{24})$.

4.2.3 HFConst Calibration

Calculate the theoretical HFConst value according to PF=1.0, standard active power value P and EC as follows:

$$HFConst = INT[P*3.6*10^6*fosc / (32*EC*Un*Ib*2^{31})]$$

P: PF=1.0, the standard active power register value calculated by the step 3 above.
fosc: Crystal frequency, it is recommended to connect with 8.192Mhz critical externally.
Un: The rated input voltage.
Ib: The rated input current.
EC: The electrical energy meter constant.
Configure the HFConst1 and HFConst2 register by the calculation result.

4.2.4 Parameter Settings

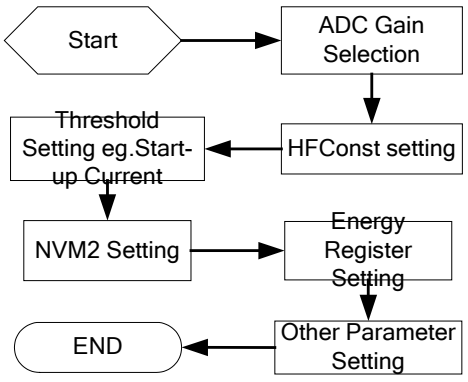


Figure4-2 parameter setting

The parameter setting flow chart is shown in Figure 4-2:

1.Configure the ADCCFG register to select the ADC gain.

2. Set HFCosnt, and fill the theoretical HFConst value calculated in chapter 4.2.3 into the HFConst1 and HFConst2 registers (optional).

3. The threshold register includes the startup current threshold, phase compensation region threshold, loss of voltage threshold, zero-crossing threshold, voltage sage threshold and overvoltage and overcurrent threshold register. Calculate the threshold according to the standard voltage and current RMS calculated in chapter 4.2.2, and fill it into corresponding threshold register. For the concrete calculation method, refer to Chapter 3.4 Configuration and Status Register.

4. For the NVM2 setting, select proper NVM2 level and select the NVM2 cycle

according to the input of the point Ib, to configure the NVM2CFG register.

5. For the energy register setting, configure the cumulative mode of the energy register, select the three-phase four-wire/three-phase three-wire, and select the clear zero type and the cumulative type. For the detailed method, refer to Chapter 3.2.6 Energy Register.

4.2.5 Channel Gain Calibration

For the rated output of the the program controlled power, assume the standard voltage RMS of phase A calculated in section 4.2.2 is UA and the standard current RMS is IA, read the actual voltage RMS register value of phase A is UA' and the actual current RMS register value is IA', then:

The voltage RMS error of phase A is ***ErrUA=（UA'-UA）/UA***.

The current RMS error of phase A is ***ErrIA=（IA'-IA）/IA***.

The U channel gain calibration of phase A can be implemented by configuring the GSUA register. The calculation method of GSUA is shown as follows:

$$USGain = \frac{-ErrUA}{1+ErrUA}$$

If USGain>=0, ***GSUA=INT[USGain*2^{15}]***.

Otherwise, if USGain<0, ***GSUA=INT[2^{16}+USGain*2^{15}]***.

The I channel gain calibration of phase A can be implemented by configuring the GSIA register. The same as that of GSUA.

The calibration error of the rated output voltage and current RMS can be controlled within 0.02% - 0.03% by this method. After the voltage RMS calibration and the current RMS calibration of phase A, the active power/reactive power/apparent power/fundamental related RMS and power gain are calibrated successfully. For HFconst is calculated by the ideal power value, the electrical energy meter error of phase A under the resistive load is calibrated automatically.

4.2.6 Channel Phase Calibration

Change the the program controlled power into PF=0.5L and rated output. Assume the ideal active power of phase A calculated in section 4.2.2 is $PA_{0.5L}$ and the read actual active power is $PA_{0.5L}$', the active power error of phase A caused by phase error is as follows:

ErrPA=（$PA_{0.5L}$' -$PA_{0.5L}$）/$PA_{0.5L}$

This error can be calibrated by configuring the U channel phase calibration register PHSUA or the I channel phase calibration register PHSIA of phase A. Phase Compensation Formula: If the angle difference between the U and I channel of phase A is θ, then:

$$\theta = \text{Arcsin}\frac{-ErrPA}{\sqrt{3}}$$

If θ >0, UA leads IA. If θ <0, UA lags IA.

For 50HZ, there is the relationship 0.017578°/LSB between the register PHSUA and the register PHSIA.

If adjust the PHSUA register, ***PHSUA = 0x80+INT (θ/0.017578°)***.

If adjust the PHSIA register and don't take the piecewise calibration into account, then:

PHSIA_R1[7:0] = 0x80-INT(θ/0.017578°)

This method puts forward high requirement for the phase accuracy and stability of the program controlled power.

4.2.7 OFFSET Calibration

The OFFSET calibration is an effect mean to improve the accuracy of the small signal under the condition that the external noise (PCB noise and transformer noise) is large and it has an effect on the accuracy of the small signal. If the external noise has a slight effect on the accuracy of the small signal (such as 1%Ib), this step can be ignored.

Description of Current OFFSET Calibration:

Take the current RMS of phase A as an example to describe the calculation process of the IA_OS register:

1) Configure the the program controlled power, so that U=Un and the current channel input is no-load.

2) MCU gets the IA register value,stores temporarily.

3) Repeat the step 2 and 3 for 11 times. The first data can be removed, and MCU get the later ten data to average, so as to get IAave.

4) Get the square of IAave for $IAave^2$. Get bit14 - bit29, and get the binary complement code. Fill in IA_OS register bit14 - bit0. Get the sign bit 1, and fill it into bit15 of the IA_OS register.

5) The current RMS offset calibration of phase A is completed.

The calibration process of the current RMS OFFSET and fundamental current RMS for other phases are the same as above.

4.3 Example of Power Calibration Method

Assume to calibrate one MUC of 220v (Un), 1.5A (In) rated input and EC 3200 (EC).The rated voltage Un=220V, and the signal amplitude of the corresponding ADC input pin is Vu=220mv, the rated current Ib=1.5A, and the signal amplitude of the corresponding ADC input pin is Vi=50mv, and the analog channel gain is 1 time.

1、 Calculation and Selection of Standard Voltage RMS Register Value

1） Calculate Theoretical Value of Voltage RMS Register for Rated Input

Bring Vu=220mV according to the formula $\boldsymbol{U_{theory}=INT[(Vu/800)*2^{27}]}$, we get:

U_{theory}= INT[(220/800)*2^{27}]=36909875

2) The reasonable selection range of $U_{standard}$ is 29527900 – 44291850 according to the condition 0.8＜$U_{standard}/U_{theory}$＜1.2.

3) LCD indication value after the MCU conversion is $U_{indication}$=220V, select 44000000 for $U_{standard}$, and MCU can be converted conveniently.

2、 Calculation and Selection of Standard Current RMS Register Value

1) Calculate Theoretical Value of Current RMS Register for Rated Input

Bring Vu=50mV according to the formula $\boldsymbol{I_{theory}=INT[(Vi/800)*2^{27}]}$, we get:

I_{theory}= INT[(50/800)*2^{27}]=8388608

2) The reasonable selection range of $I_{standard}$ is 6710886 - 10066329 according to the condition 0.8＜$I_{standard}/I_{theory}$＜1.2.

3) LCD indication value after the MCU conversion is $I_{indication}$=1.5A, select 7500000 for $I_{standard}$, and MCU can be converted conveniently.

3. Calculate Standard Active Power Register Value for PF=1.0 and PF=0.5L

For the rated input and PF=1.0, the standard active power value is as follows:

$\boldsymbol{P = INT(U_{standard}* I_{standard}/2^{23})}$=44000000*7500000/$2^{23}$=39339066

For the rated input and PF=0.5L, the standard active power value is as follows:

$\boldsymbol{P_{0.5L}= INT(U_{standard}* I_{standard}/2^{24})}$= 39339066/2=19669533

4. Calculation and Configuration of HFConst:

Formula: $\boldsymbol{HFConst = INT[P*3.6*10^6*fosc / (32*EC*Un*Ib*2^{31})]}$

= INT[(39339066*3.6*8.192*10^{12})/ (32*3200*220*1.5*2^{31})]

= 15987=3E73H

Hence, The RN8302B configures HFConst1= HFConst2=3E73H.

5. Parameter Settings

Neglected.

6. Channel Gain Calibration Process

Rated output of the the program controlled power, read the voltage RMS register of phase A. Assume it is 37297350, then ***ErrUA=（UA'-UA）/UA***=(37297350-44000000)/44000000=-0.152333. Write ***-ErrUA/(1+ErrUA)***= 0.1321953*32768=4332 into the register GSUA. In this way, it calibrates the voltage RMS register into 44000000, and the calibration error is controlled within 0.02% - 0.03%.

Read the current RMS register of phase A. Assume it is 8299685, then ***ErrIA=（IA'-IA）/IA***=(8299685-7500000)/7500000= 0.106625 and ***-ErrIA/(1+ErrIA)***= -0.0963515. Write

INT[65536-0.0963515*32768]=F3ABH into the register GISA. In this way, it calibrates the current RMS into 7500000, and the calibration error is controlled within 0.02% - 0.03%.

After the voltage and current RMS calibration of phase A are completed, the active power/reactive power/fundamental related RMS and power are calibrated successfully. For HFconst calculates 3E73H by the standard active power, the electrical energy error of phase A is calibrated automatically.

Phase B and C are calibrated by complying with the same process.

7. Channel Phase Calibration Process

After the channel gain is calibrated, PF is changed into 0.5L, and the active power register value of phase A is read as 19526535, then:

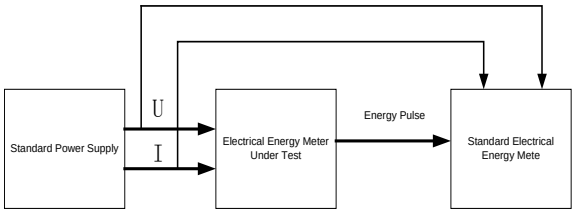
$ErrPA=(PA_{0.5L}' -PA_{0.5L})/PA_{0.5L}$ =(19526535-19669533)/19669533=-0.00727

θ=ArcSin(-(-0.00727)/1.732)=ArcSin0.0042=0.2406°.

PHSUA=128+INT[0.2406/0.017578]=142, convert the hex into 0x8E.

Phase B and C are calibrated by complying with the same process.

4.4 Pulse Calibration Method



If provided with the program controlled power source with general accuracy, but with the high level of the normative meter , they may take the pulse calibration method as shown in the figure left into account.

The calibration flow of the pulse calibration method is shown in Figure 4-3:

The previous several steps of the pulse calibration flow are the same as that of the power calibration flow, and it only calculates the power gain register and phase register value by the normative meter error in the gain calibration and phase calibration node.

According to the PF=1.0 error of the normative meter , for the detailed method to calculate the power gain register value, refer to Chapter 3.4.11.After GPA is

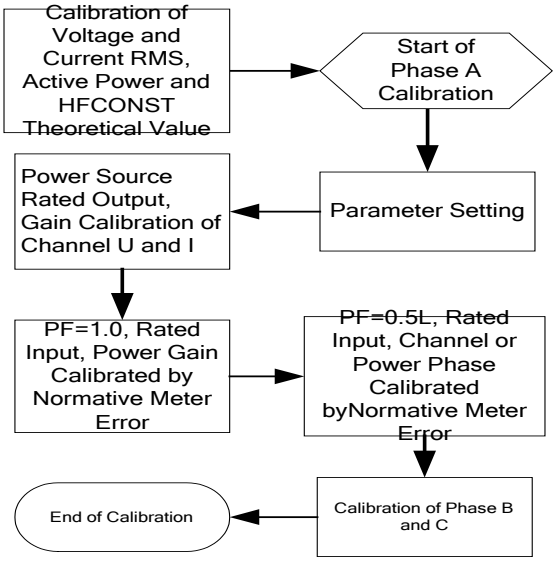


Figure 4-3 Pulse Method Calibration Flow

adjusted, fill in the same value for GQA, GSA, FGPA, FGQA and FGSA.

According to the PF=0.5L error of the normative meter , for the detailed method to calculate the channel phase register value, refer to Chapter 3.4.7.

According to the PF=0.5L error of the normative meter , for the detailed method to calculate the power phase register value, refer to Chapter 3.4.12.

5 Communication Interface

- Support the serial communication interface SPI.Operates in the slave mode.
- SPI Interface Rate: MAX 3.5Mbps
- Transmission Reliability: The SPI frame format includes the checksum bytes.
- The reading waveform buffer supports the BURST 1/4/8/16 mode.
- 3.3V/5V compatible

5.1 SPI Address Space Description

Address AD[10:0] Mapping:
0x000~0x0FF: Measurement parameter register space
0x100~0x1FF: Configuration and status register space
0x200~0x27F: Waveform sample data buffer block space 1
0x280~0x2FF: Waveform sample data buffer block space 2
0x300~0x37F: Waveform sample data buffer block space 3
0x380~0x3FF: Waveform sample data buffer block space 4
0x400~0x47F: Waveform sample data buffer block space 5
0x480~0x4FF: Waveform sample data buffer block space 6

5.2 SPI Interface Signal Description

SCSN: SPI slave device chip select signal,, active at low level, input signal, and external pull-up resistors recommended.

When SCSN changes from high to low, it indicates current chip is selected,and in the communication status. When SCSN changes from low to high, it indicates the communication is completed, and the communication port reset to the idle status.

SCLK: The serial clock input pin, which determines the transmission rate that the data in or out of the SPI interface.

All data transmission operations synchronize with SCLK, RN8302B outputs the data from the SDO pin at the rising edge, and the master outputs the data from the SDI pin at the rising edge. Both RN8302B and the master read the data at the falling edge.

SDI: Serial data input pin. Used to transmit the master data to RN8302B.

SDO: Serial data output pin,Used to output the RN8302B data to the master. When SCSN is high, it is the high impedance state.

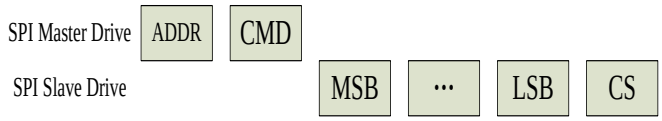
5.3 SPI Frame Format

The SPI frame includes the read register frame, write register frame and BURST read

waveform data buffer frame. Transmission processes of each frames are shown as follows:

Write Operation:

Read Operation:



Where:

ADDR Byte: Includes AD[7:0], refer to the low 8-bit address of the destination address.

CMD Byte: Includes {R/W, AD[10:8], BL[1:0], 2'h0}, where,

R/W=0, read operation, R/W=1, write operation.

AD[10:8], the high 3-bit address of the destination address, namely, the Bank address.

BL[1:0], it is valid only when BURST read waveform data buffer frame only, to indicates the length of the BURST read operation (namely, the number of addresses which is read).

BL[1:0]=2'b00, the BURST read length is 1.

BL[1:0]= 2'b 01, the BURST read length is 4.

BL[1:0]= 2'b 10, the BURST read length is 8.

BL[1:0]= 2'b 11, the BURST read length is 16.

When the address is in the waveform sample data buffer space, BL is valid, and the address takes the increment mode.

When the address is not in the waveform sample data buffer space, BL is invalid. However, its value still participates in the checksum calculation.

During the write operation, BL is invalid. However, its value still participates in the checksum calculation.

MSB LSB Byte: Data block: Send high byte firstly, and then send low byte.

CS Block: The checksum bytes.

For the description of these three types of the SPI frame formats, refer to Table 5-1.

Table 5-1 RN8302B SPI Frame Format

Command Name	ADDR	CMD	DATA	CHECK SUM	Description
Read Register Frame	{REG_ADR[7:0]}	{1'b0, BANK[2:0], 4'b0000} BANK=3'b000,register address is mapped to the measurement parameter register address space. BANK=3'b001, register	RDATA	RN8302B calculates and sends the frame checksu	Read data from the register with the address {BANK[2:0], REG_ADR[7:0]}.

		address is mapped to the configuration and status register address space.		m.	
Write Register Frame	{REG_ADR[7:0]}	{1'b1, BANK[2:0], 4'b0000} BANK=3'b000, register address is mapped to the measurement parameter register address space. BANK=3'b001, register address is mapped to the configuration and status register address space.	WDATA	MCU calculates and sends the write register frame checksum.	Write data into the register with the address {BANK[2:0], REG_ADR[7:0]}.
BURST Reads Waveform Data Buffer Frame	{BUF_ADR[7:0]}	{0, BANK[2:0], BURST_LEN[1:0], 2'b00} BANK=3'b010-3'b100 address is mapped to the waveform buffer RAM address space. BURST_LEN[1:0]=2'b00, single address operation. BURST_LEN[1:0]=2'b01, 4 addresses operation. BURST_LEN[1:0]=2'b10, 8 addresses operation. BURST_LEN[1:0]=2'b11,16 addresses operation.	RBUF_DATA	RN8302B calculates and sends the frame checksum.	Read the data from the waveform buffer area BURST with the initial address {BANK[2:0], REG_ADR[7:0]}.

Checksum Algorithm: ADDR+CMD+DATA single byte negated sum.

5.4 SPI Writes Timing

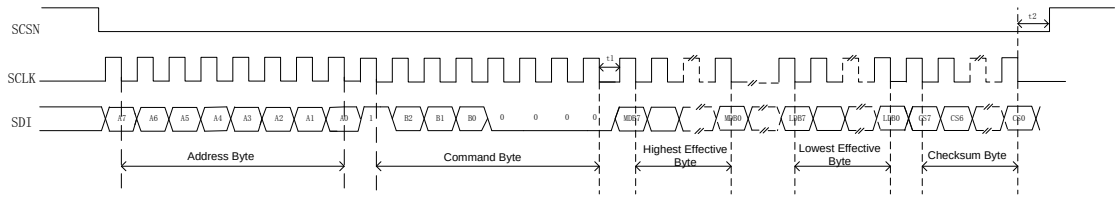


Figure 5-1 SPI Writes Timing

Operating Process:

After SCSN is valid, the master will write the address and the command byte by SPI, and then write the data byte.

Note:

1. Transmit takes byte as the unit. The high bit is front, and the low bit is last.
2. The multi-byte register transmits the high byte firstly, and then transmits the low byte.
3. The master writes data at the High level of SCLK, and the slave equipment reads data at the SCLK low level.
4. The time t11 between the data byte shall be greater than or equal to half of SCLK cycle.
5. After the last byte of LSB is transmitted successfully, complete the data transmission when SCSN changes from high to low. The time t2 between falling edge and rising edge of SCLK shall be greater than or equal to half of SCLK cycle.

Note: It is necessary for the register with the write protection function to write the Write Enable command before the write operation.

5.5 SPI Reads Timing

Operating Process:

The master will write the address and the command byte (8bit, including the register address) by SPI after SCSN is valid, and the slave will output the data in bits from the SDO pin at the falling edge of SCLK after it receives the read command.

Note:

1. Transmit by taking byte as the unit. The high bit is front, and the low bit is last.
2. The multi-byte register transmits the high byte firstly, and then transmits the low byte.
3. The master writes the command byte at the High level of SCLK, and the slave equipment outputs the data from SDO at the High level of SCLK.
4. The time t1 of the data byte shall be greater than or equal to half of SCLK cycle.
5. After the last byte of LSB is transmitted successfully, complete the data transmission when SCSN changes from low to high. The time t2 between the falling edge and the rising edge of SCLK shall be greater than or equal to half of SCLK

cycle.

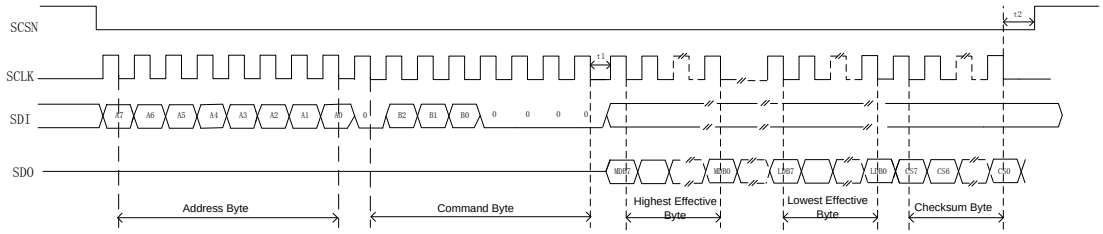


Figure 5-2 SPI Reads Timing

5.6 SPI Interface Reliability Design

The SPI interface reliability design includes the following aspects:

1. Check Function

1) The last byte of the SPI frame structure is the checksum byte of this frame.

2) Provide the checksum CHECKSUM1 (0x6A) of the EMM calibration register and EMM configuration register and the checksum CHECKSUM2 (0x8B) of NVM1, NVM2 and system configuration register.

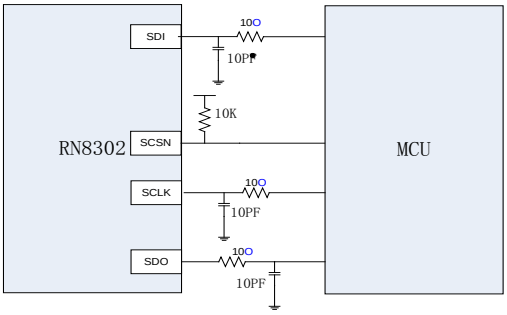
3) Provide the SPI read check register RData (0x8C), and saves the data read by SPI last time.

4)Provide the SPI write check register WData (0x8D), and saves the data written by SPI last time.

2. Write Protection Function

Provide all R/W registers with the write protection function.

3. Application Circuit Design



The SPI transmission signal line may jitter for the interference, so the external resistors and capacitors necessary for filtering .as shown in the figure. The selection of parameters can be determined according to the requirement.

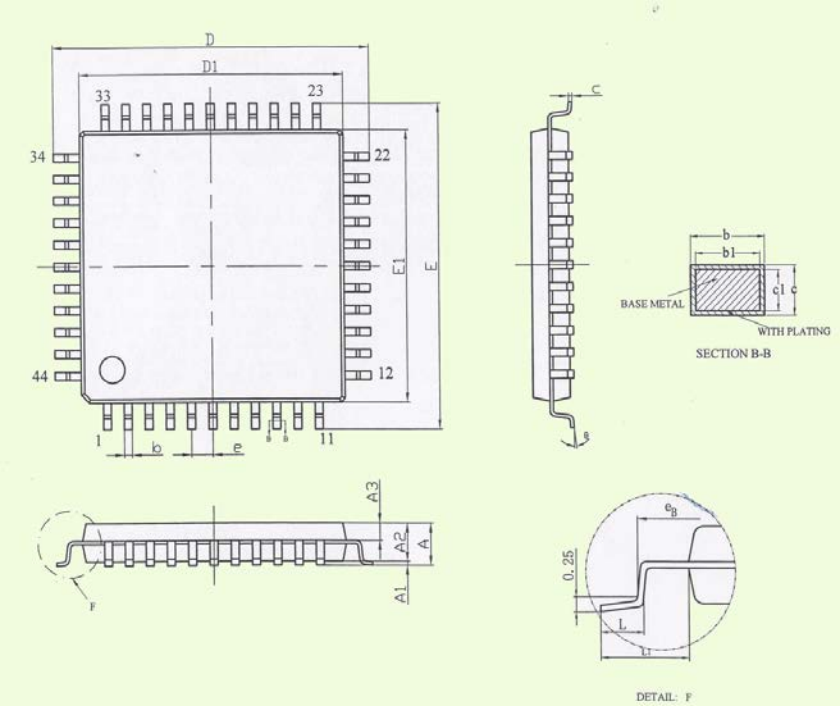
6 Electrical Specifications

Accuracy (DVCC=AVCC=3.3V±5%, Room Temperature)						
Measurement Item	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Unit**	Test Condition and Annotation
Active Electrical Energy Measurement Error	Err		0.1%			Dynamic range of 5000:1 at normal temperature
Reactive Electrical Energy Measurement Error	Err		0.1%			Dynamic range of 5000:1 at normal temperature
Electrical Energy Measurement Bandwidth	BW		7		kHz	fosc=8.192MHz
RMS Measurement Error	RErr		0.2%			Dynamic range of 1000:1 at normal temperature
NVM1 RMS Measurement Error	NRErr		0.5%			Dynamic range of 400:1 at normal temperature
RMS Measurement Error	BW		7		kHz	fosc=8.192MHz
Phase Angle Resolution	YErr		0.02		°	Current channel 50mV input, phase angle 60°120°240°300°
Frequency Measurement Resolution			0.0001		Hz	40Hz - 70Hz
Frequency Measurement Error	FErr		0.02%			40Hz - 70Hz
Calibration Range						
Channel Gain Calibration Coefficient	GS	0		2		
Channel Phase Calibration	PHS	-2.259		2.259	°	fosc=8.192MHz
Analog Inputs						
Maximum Signal Levels	V_{xn}			800	mVp	Peak-peak value,

					p	PGA=1
-3dB Bandwidth	B_{-3dB}		7		kHz	fosc=8.192MHzz
Current Channel Crosstalk			-110		dB	UA=UB=UC=800mVpp
Reference Voltage (DV_{CC}=AV_{CC}=3.3V±5%, Temperature Range: -40℃ - +85℃)						
Output Voltage	V_{ref}		1.25		V	1.25±4%
Temperature Coefficient	T_c		20		ppm/℃	
Clock Input						
Frequency Range of Input Voltage	fxi	4.096	8.192	11	MHz	
XI Input Capacitance	Cxi		15		pf	
XO Output Capacitance	Cxo		15		pf	
Digital Interface						
SPI Interface Rate				3.5M	bps	
SCLK, SCSN and SDI Logic Input Low Level	Vil			1.5	V	
SCLK, SCSN and SDI Logic Input High Level	Vih	2.2			V	
CF1-CF4 and INTN Logic Output High Level	Voh	3				Isource=4mA
CF1-CF4 and INTN Logic Output Low Level	Vol			0.4		Isink=4mA
Power Supply						
Analog Power Supply	AVCC	3.0	3.3	3.6	V	
Digital Power Supply	DVCC	3.0	3.3	3.6	V	
Power dissipated (DV_{CC}=AV_{CC}=3.3V±5%, Room Temperature)						
EMM Current	Idd1		5		mA	fosc=8.192MHz Idd1=AIdd1+DIdd1, the same below
NVM1 Current	Idd2		2		mA	OSCI=8.192MHz
NVM2 Current	Idd3		0.15		mA	
SLM Current	Idd4		2		μA	
ABSOLUTE MAXIMUM RATINGS						
Digital Supply Voltage	DVCC	-0.3	--	+6	V	
Analog Supply Voltage	AVCC	-0.3	--	+6	V	
DV_{cc} to DGND		-0.3	--	+3.7	V	
VO to DGND		-0.3		+3	V	
DVCC to AVCC		-0.3		+0.3	V	

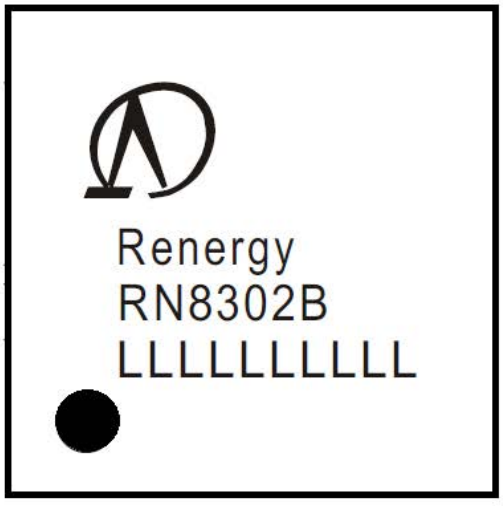
Analog Differential Input		-2		+2	V	
REFV Pin Input		-0.3		AVCC +0.3	V	
Digital Input Voltage to GND	V_{IND}	-0.3	--	DVCC +0.3	V	
Digital Output Voltage to GND	V_{outD}	-0.3	--	DVCC +0.3	V	
Operating Temperature Range	T_A	-40	--	85	℃	
Storage Temperature Range	T_{stg}	-65	--	150	℃	

7 Package Size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.29	—	0.37
b1	0.28	0.30	0.33
c	0.13	—	0.18
c1	0.12	0.127	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
e_B	11.25	—	11.45
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	7°
L/F Carrier Size (MIL)	122*122		160*110
	180*180		205*205

8 Package Information



Line1: Company Trademark
Line2: Corporate name
Line3: Product Name
Line4: Product Lot number
The Product Lot number consists of 10 characters including number and letter.
The first 5 characters shows production code of WAFER, in which:

The 1st character shows the wafer out year, showed by numbers 1 to 9 and letters which A indicates 2010 and the like, pls see details in follower "Year Code Table".

The 2nd character shows the wafer out month, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower "Month Code Table".

The 3rd to 5th characters show the serial number of wafer lot (begin with 001 and increase by one).

The 6th character is reserved.

The 7th and 8th characters shows the chip packaging company and production line.

The 9th character shows the month for chip packaging, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower "Month Code Table".

The 10th character shows the date for chip packaging, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower "Date Code Table".

Lower left quarter: PIN1 flag

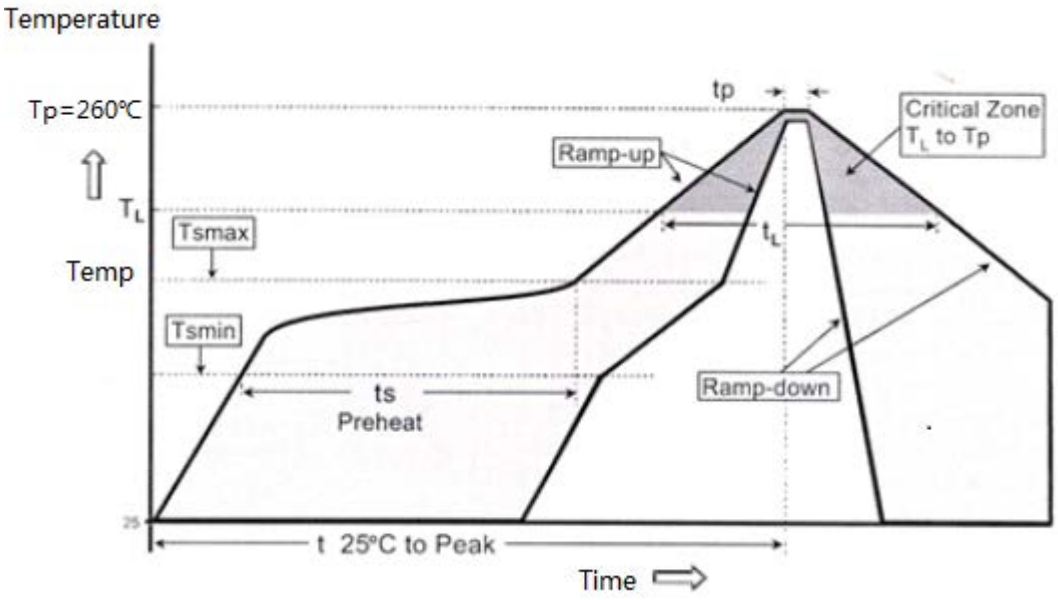
Year Code Table										
Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Code	1	2	3	4	5	6	7	8	9	A
Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Code	B	C	D	E	F	G	H	J	K	L
Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	
Code	M	N	P	R	S	T	U	V	W	

Month Code Table												
Month	1	2	3	4	5	6	7	8	9	10	11	12
Code	1	2	3	4	5	6	7	8	9	A	B	C

Date Code Table										
Date	1	2	3	4	5	6	7	8	9	10
Code	1	2	3	4	5	6	7	8	9	A

Date	11	12	13	14	15	16	17	18	19	20
Code	B	C	D	E	F	G	H	J	K	L
Date	21	22	23	24	25	26	27	28	29	30
Code	M	N	P	R	S	T	U	V	W	X
Date	31									
Code	Y									

9 Temperature Setting Conditions of SMT



parameter	value
TL Tp (TL to Tp)	217℃ 260℃ Max 3℃/second
Ts min Ts max Time（max-min）（ts）	150℃ 200℃ 60-180 second
Ts max - (Ts max to TL)	Max 3℃/ second