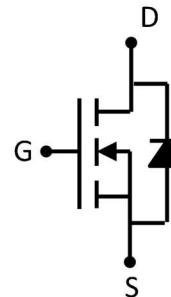


Feature

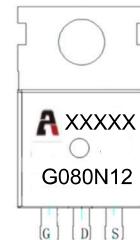
- 120V,106A
- $R_{DS(ON)} < 8.0 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$ (TYP:6.5m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic diSgram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G080N12	APG080N12	TO-220	-	-	1000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a = 25^\circ\text{C}$)	I_D	106	A
Continuous Drain Current ($T_a = 100^\circ\text{C}$)	I_D	67	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	424	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	480	mJ
Power Dissipation	P_D	147	W
Thermal Resistance from Junction to Case	R_{eJC}	0.85	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^\circ C$ unless otherwise noted)

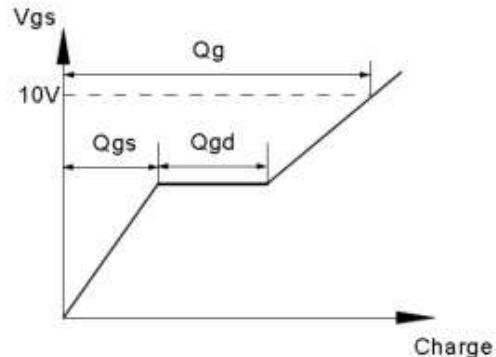
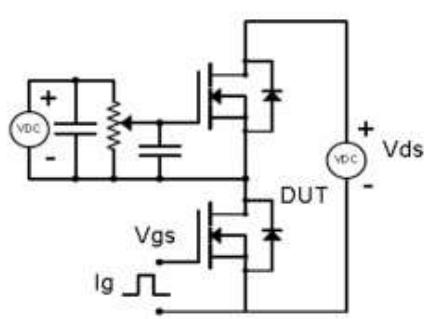
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	120	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 120V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.0	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 40A$	-	6.5	8.0	$m\Omega$
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 60V, V_{GS} = 0V, f = 1MHz$	-	3770	-	pF
Output Capacitance	C_{oss}		-	352	-	
Reverse Transfer Capacitance	C_{rss}		-	17	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 50A,$ $V_{GS} = 10V, R_G = 3\Omega$	-	22	-	ns
Turn-on rise time	t_r		-	18	-	
Turn-off delay time	$t_{d(off)}$		-	49	-	
Turn-off fall time	t_f		-	19	-	
Total Gate Charge	Q_g	$V_{DS} = 50V, I_D = 50A,$ $V_{GS} = 10V$	-	56	-	nC
Gate-Source Charge	Q_{gs}		-	12	-	
Gate-Drain Charge	Q_{gd}		-	14	-	
Reverse Recovery Charge	Q_{rr}	$I_F = 30A, di/dt = 100A/\mu s$	-	102	-	nC
Reverse Recovery Time	T_{rr}	$I_F = 30A, di/dt = 100A/\mu s$	-	66	-	ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{GS} = 0V, I_S = 50A$	-	-	1.3	V
Diode Forward current ⁽⁴⁾	I_S		-	-	106	A

Notes:

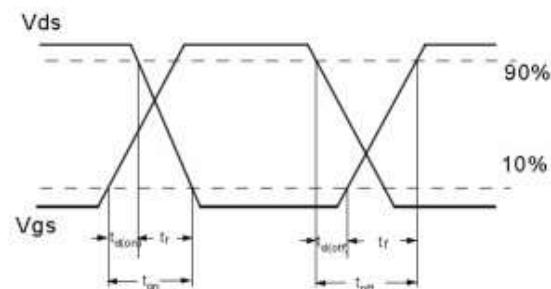
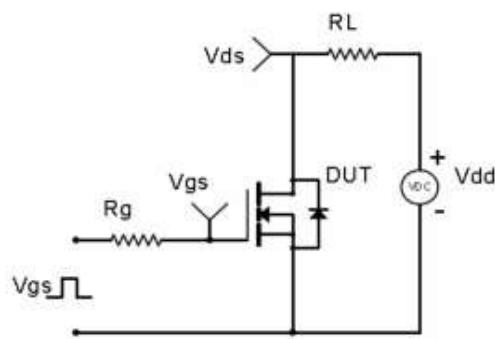
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^\circ C, V_{DD} = 50V, R_G = 25\Omega, L = 0.5Mh$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

Test Circuit & Waveform

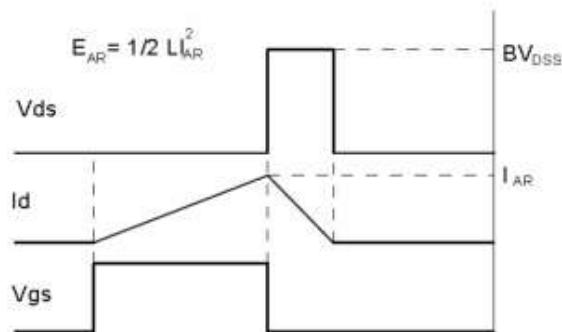
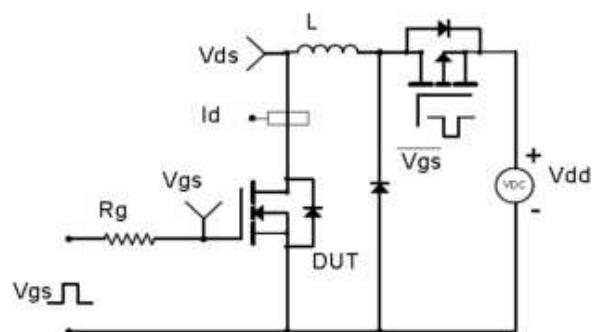
Gate Charge Test Circuit & Waveform



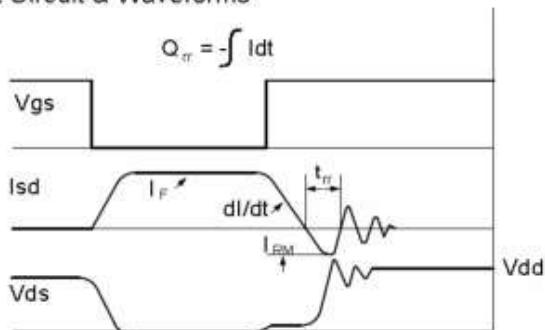
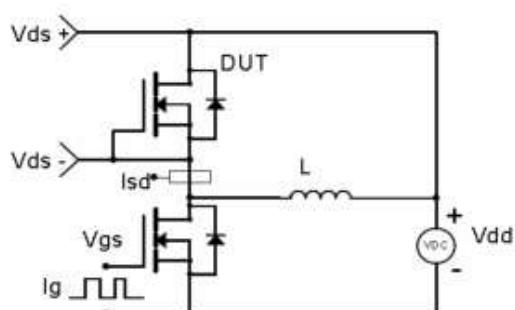
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Performance Characteristics

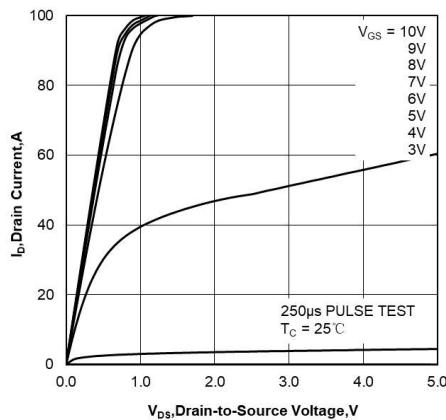


Figure 1. Output Characteristics

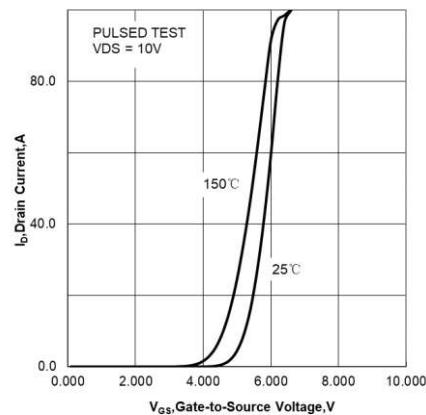


Figure 2. Transfer Characteristics

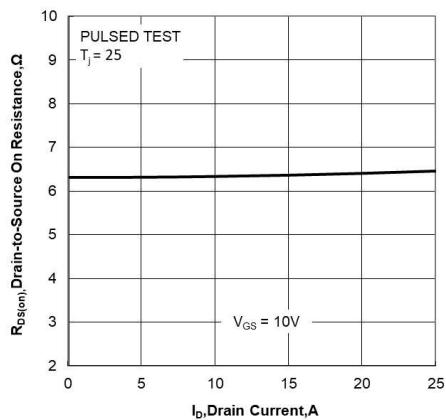


Figure 3. Drain-to-Source On Resistance
vs Drain Current

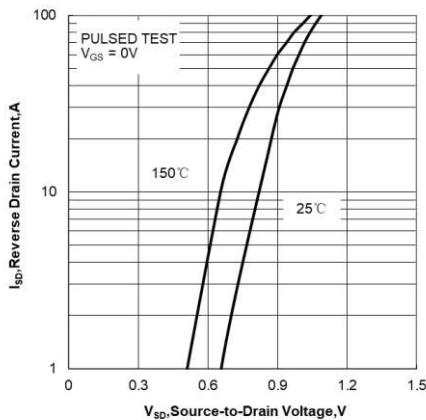


Figure 4. Body Diode Forward Voltage
vs Source Current and Temperature

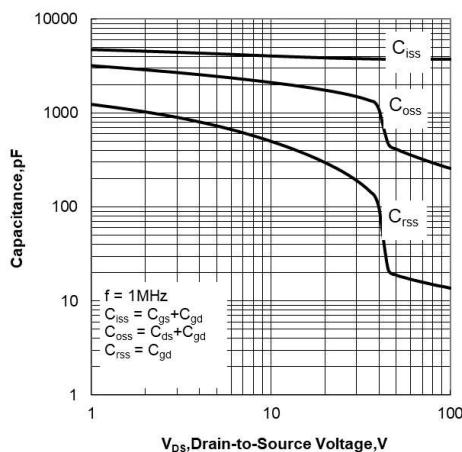


Figure 5. Capacitance Characteristics

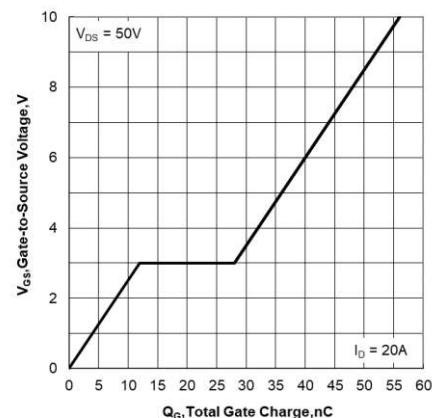
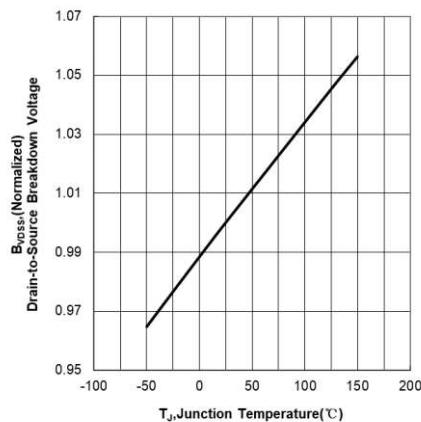


Figure 6. Gate Charge Characteristics

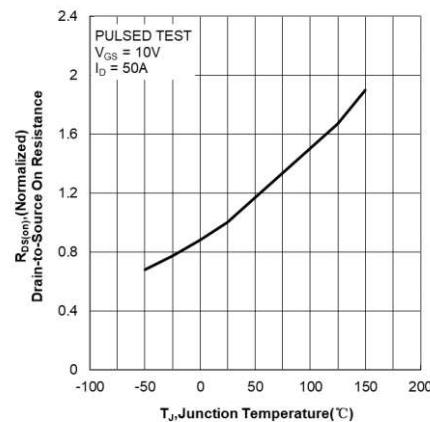
APG080N12

N-Channel Enhancement Mosfet

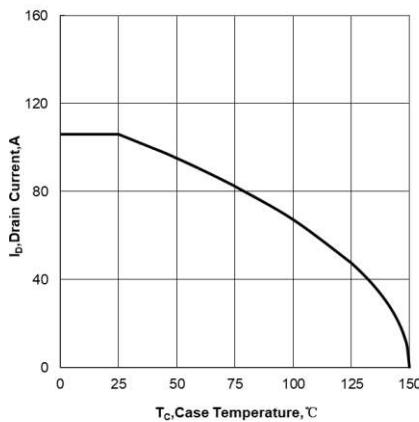
AllPOWER
DATA SHEET



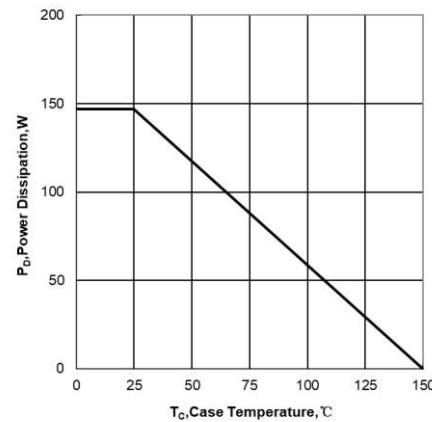
**Figure 7. Normalized Breakdown Voltage
vs Junction Temperature**



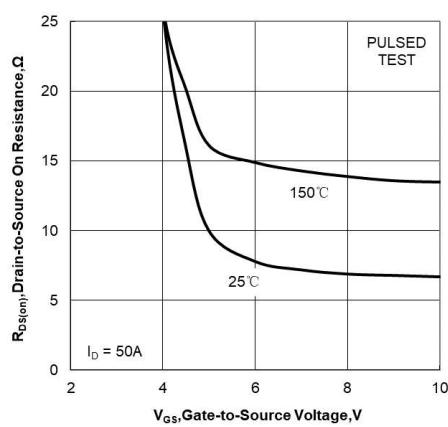
**Figure 8. Normalized On Resistance vs
Junction Temperature**



**Figure 9. Maximum Continuous Drain Current
vs Case Temperature**



**Figure 10. Maximum Power Dissipation
vs Case Temperature**



**Figure 11. Drain-to-Source On Resistance vs Gate
Voltage and Drain Current**

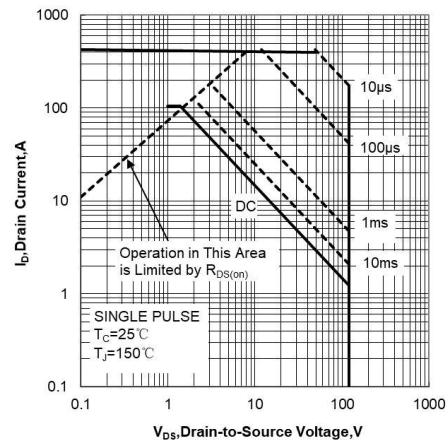


Figure 12. Maximum Safe Operating Area

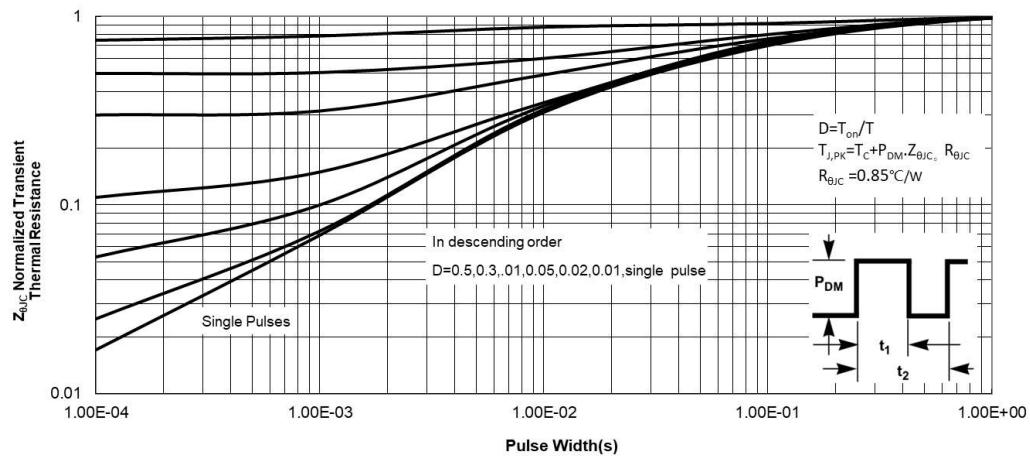


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-220 Package Information

