NUP4202W1

ESD Protection Diode, Low Clamping Voltage

The NUP4202W1 surge protection is designed to protect high speed data lines from ESD, EFT, and lightning.

Features
- Low Clamping Voltage
- Stand−Off Voltage: 5 V
- Low Leakage
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4 ESD Protection
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications
- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI) and HDMI
- Monitors and Flat Panel Displays
- MP3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μS @ T_A = 25°C (Note 1)	P_{pk}	500	W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Air (ESD) IEC 61000−4−2 Contact (ESD)	ESD	16000 400 20000 20000	V
IEC 61000−4−4 (5/50 ns)	EFT	40	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Nonrepetitive current pulse per Figure 5 (Pin 5 to Pin 2).

See Application Note AND8308/D for further description of survivability specs.
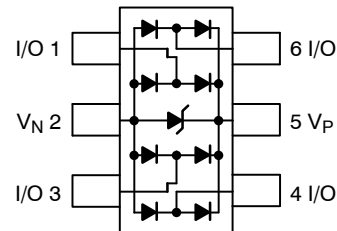
SC−88 LOW CAPACITANCE DIODE SURGE PROTECTION ARRAY
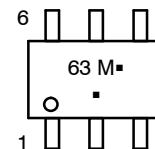**500 WATTS PEAK POWER**
6 VOLTS

PIN CONFIGURATION AND SCHEMATIC

SC−88
CASE 419B
PLASTIC

MARKING DIAGRAM

63 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NUP4202W1T2G	SC−88 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP4202W1

ELECTRICAL CHARACTERISTICS
($T_A = 25°C$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and f = 1.0 MHz
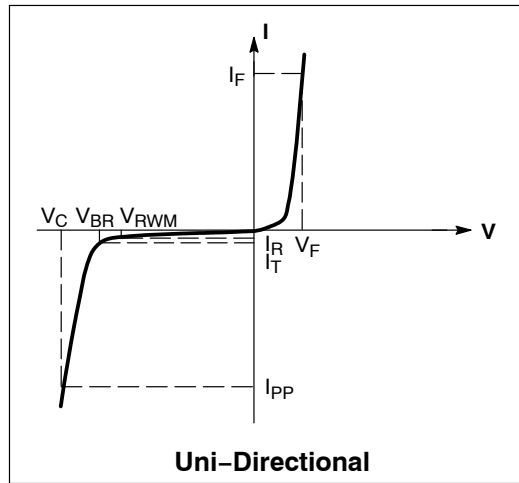
*See Application Note AND8308/D for detailed explanations of datasheet parameters.

Uni−Directional

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 2)			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 3)	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V			5.0	μA
Clamping Voltage	V_C	I_{PP} = 5 A (Note 4)		8.5	12.5	V
Clamping Voltage	V_C	I_{PP} = 8 A (Note 4)		8.9	20	V
Maximum Peak Pulse Current	I_{PP}	8x20 μs Waveform (Note 4)			28	A
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		3.0	5.0	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		1.5	3.0	pF
Clamping Voltage	V_C	@ I_{PP} = 1 A (Notes 5 and 6)		14.5		V
Clamping Voltage	V_C	Per IEC 61000−4−2 (Note 7)	Figure 1 and 2			V

2. Rurge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. Nonrepetitive current pulse per Figure 5 (Pin 5 to Pin 2).
5. Nonrepetitive current pulse per Figure 5 (Any I/O Pins).
6. Surge current waveform per Figure 5.
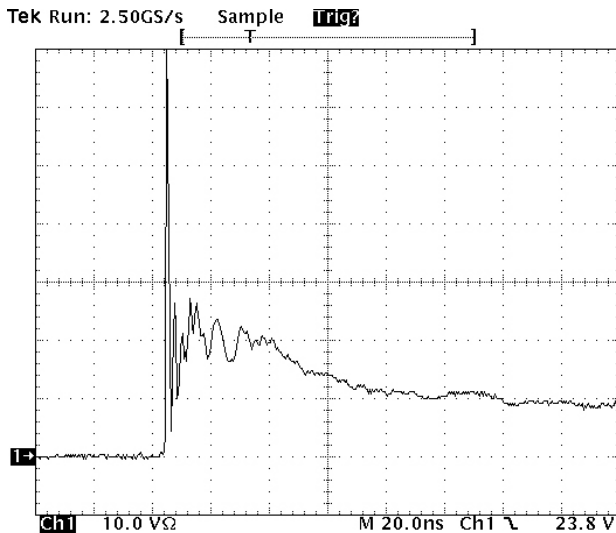7. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

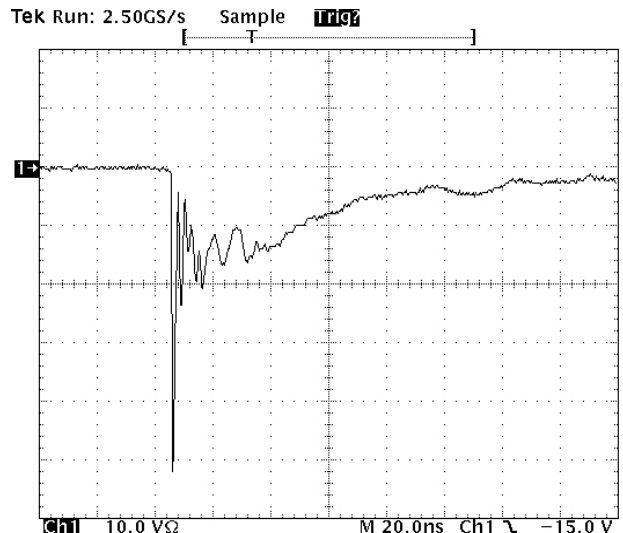**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2**

Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Volt-age (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000−4−2 Waveform

Figure 3. IEC61000−4−2 Spec
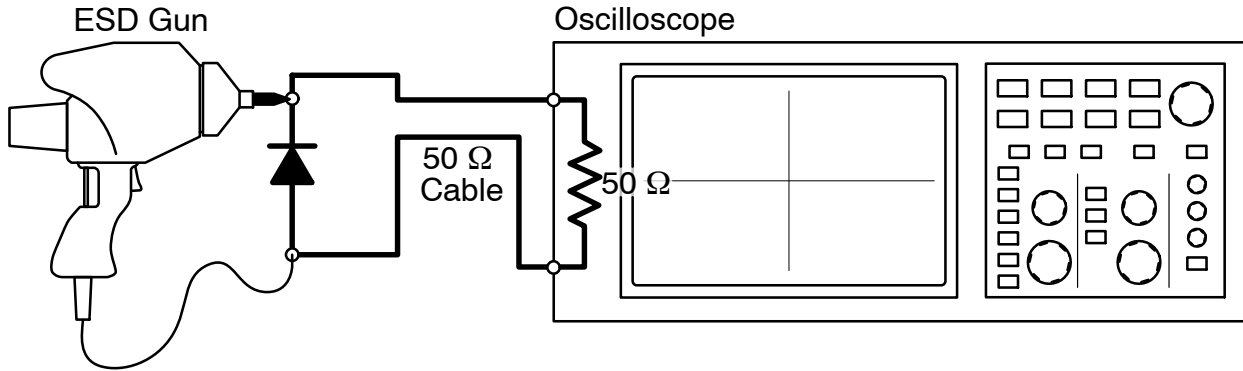
Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.
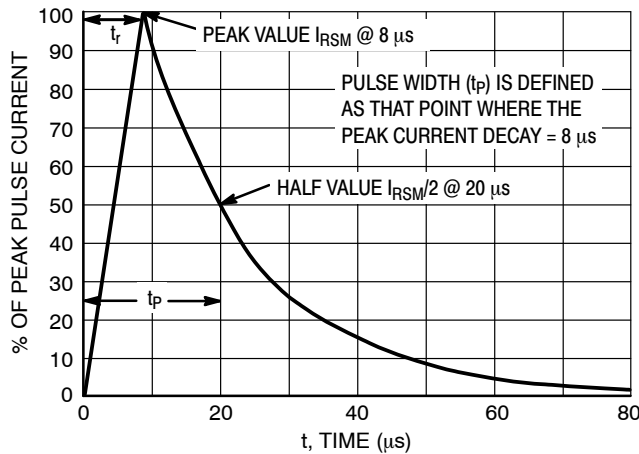
Figure 5. 8 X 20 μs Pulse Waveform

NUP4202W1

TYPICAL PERFORMANCE CURVES
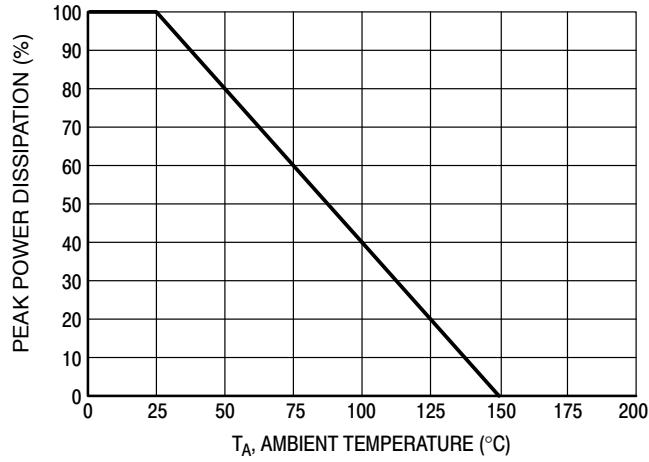
(T_J = 25°C unless otherwise noted)
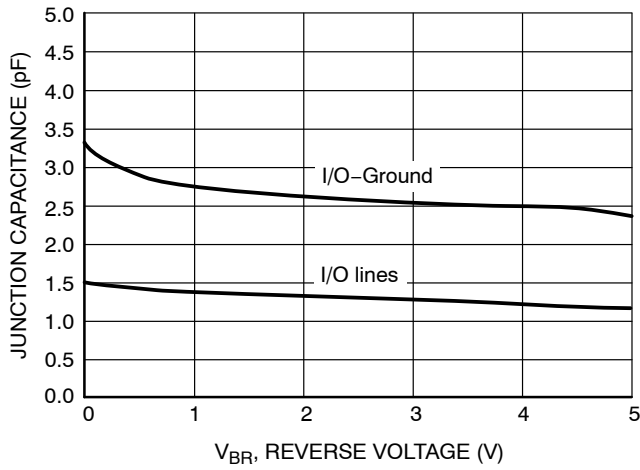

Figure 6. Pulse Derating Curve
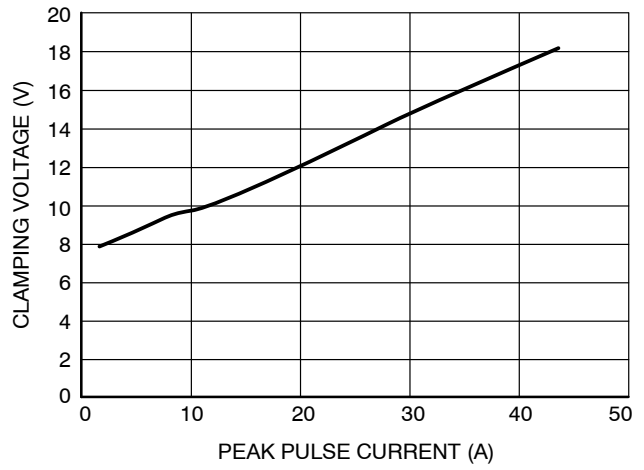

Figure 7. Junction Capacitance vs Reverse Voltage

**Figure 8. Clamping Voltage vs. Peak Pulse Current
(8 x 20 μs Waveform)**

APPLICATIONS INFORMATION

The new NUP4202W1 is a low capacitance surge protection diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4202W1 offers surge rated, low capacitance steering diodes and a surge protection diode integrated in a single package (SC−88). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The surge protection device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

NUP4202W1 Configuration Options

The NUP4202W1 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC} + V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

Protection of four data lines and the power supply using V_{CC} as reference.
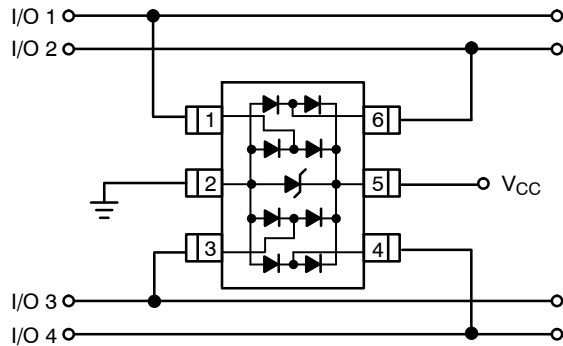
For this configuration, connect pin 5 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. The internal surge protection diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

Protection of four data lines with bias and power supply isolation resistor.
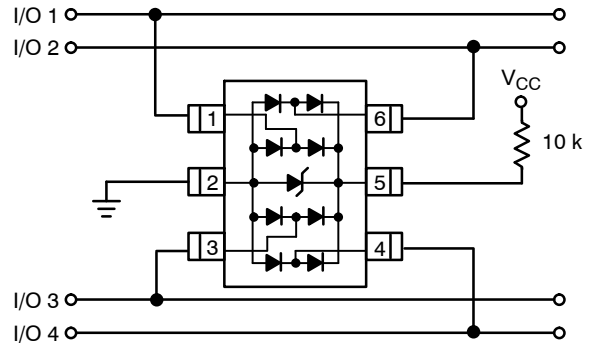
The NUP4202W1 can be isolated from the power supply by connecting a series resistor between pin 5 and V_{CC}. A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal surge protection and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal surge protection diode as reference.
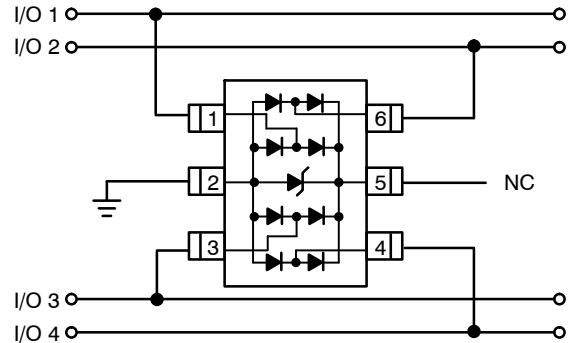
In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal surge protection can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the surge protection plus one diode drop ($V_c = V_f + V_{RWM}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:
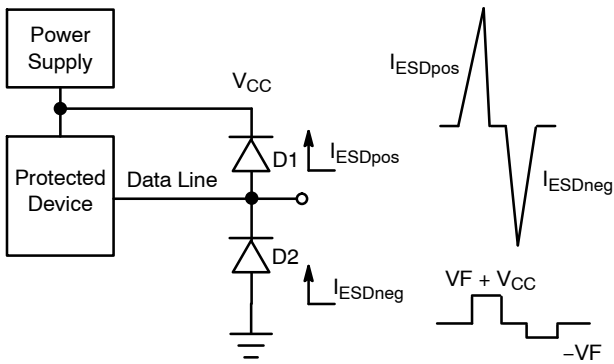
Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:
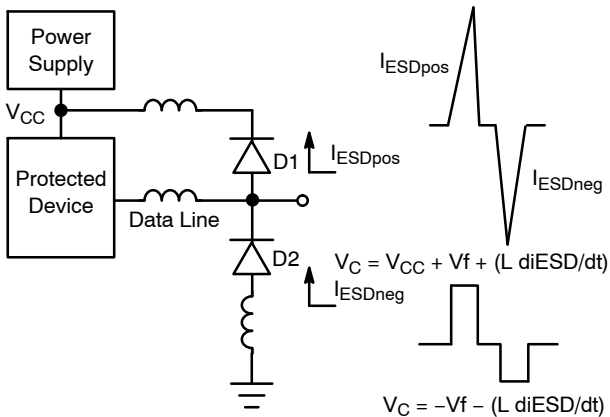
For positive pulse conditions:

$Vc = V_{CC} + Vf_{D1}$

For negative pulse conditions:

$Vc = -Vf_{D2}$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.

An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$Vc = V_{CC} + Vf + (L \, d_{iESD}/dt)$

For negative pulse conditions:

$Vc = -Vf - (L \, d_{iESD}/dt)$

As shown in the formulas, the clamping voltage (Vc) not only depends on the Vf of the steering diodes but also on the L d_{iESD}/dt factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic inductance will provide significant benefits in transient immunity.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.
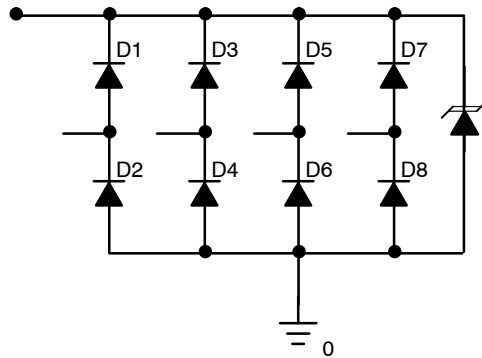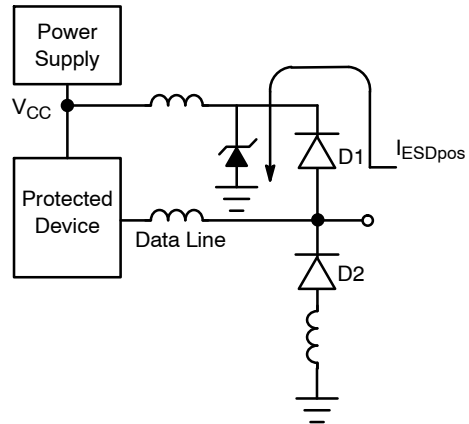

Figure 9. NUP4202W1 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the surge protection diode as shown below.

The resulting clamping voltage on the protected IC will be:

$Vc = V_F + V_{RWM}$.

The clamping voltage of the surge protection diode is provided in Figure 8 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.
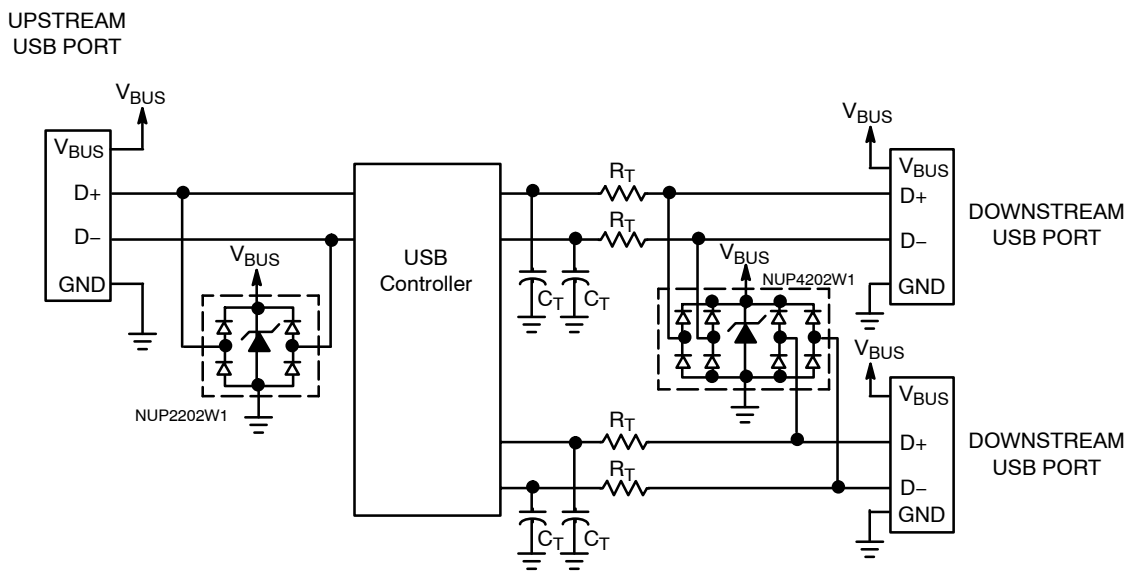
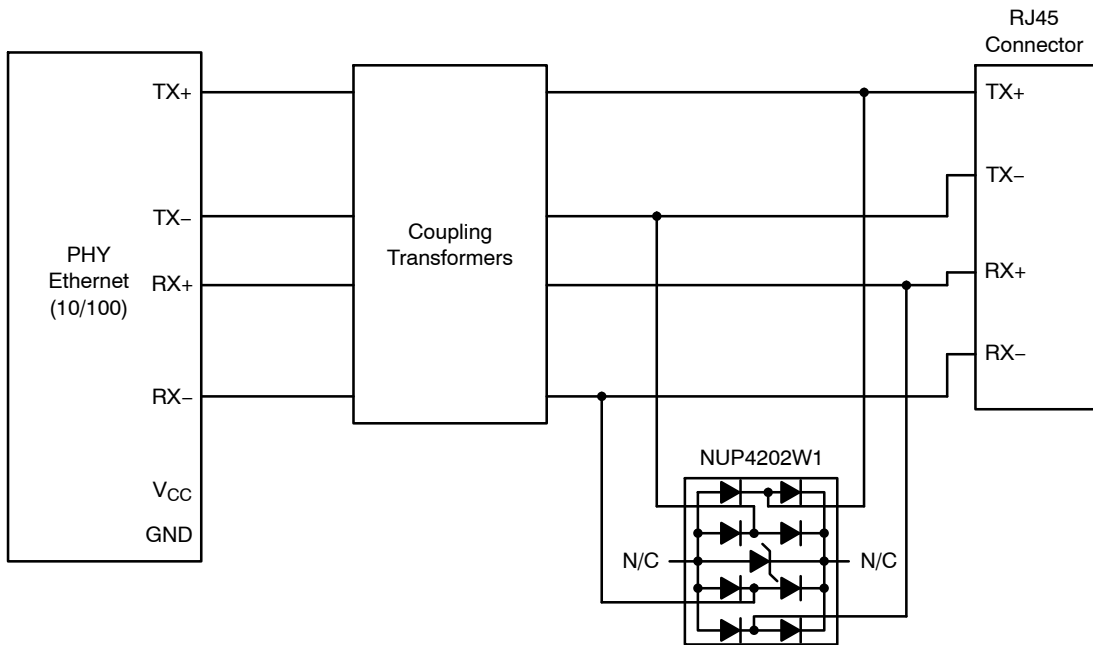## TYPICAL APPLICATIONS

Figure 10. ESD Protection for USB Port

Figure 11. Protection for Ethernet 10/100 (Differential Mode)
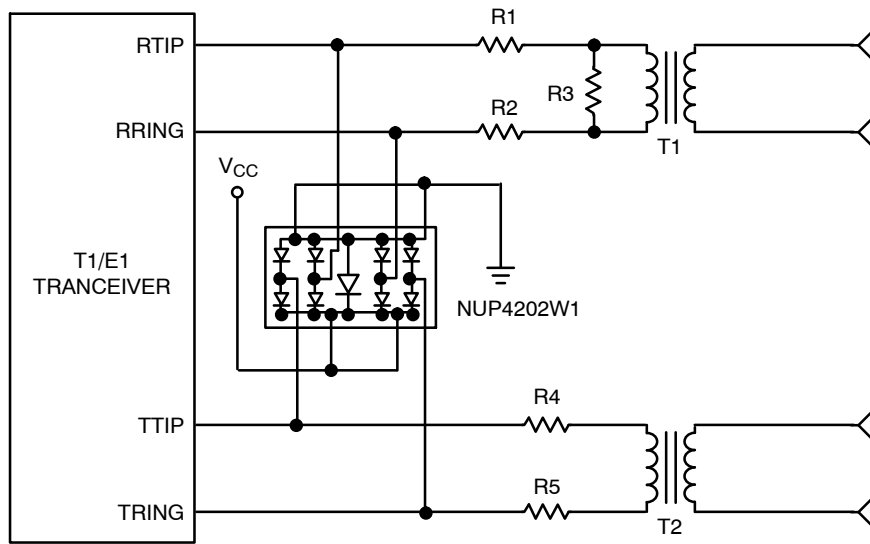
NUP4202W1

Figure 12. TI/E1 Interface Protection

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

1
SCALE 2:1

DATE 11 DEC 2012

TOP VIEW

2X | aaa | H | D

2X | bbb | H | D

2X 3 TIPS

aaa | C

⊕ | ddd Ⓜ | C | A−B | D

H

GAGE PLANE

DETAIL A

L2

L

SIDE VIEW

6X | ccc | C

A2

A

A1

C SEATING PLANE

DETAIL A

END VIEW

c
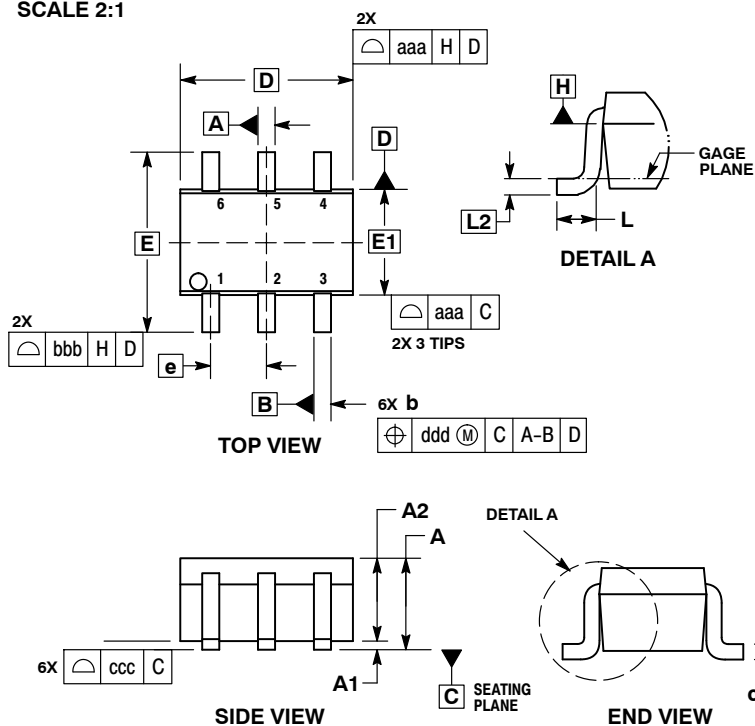
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

6X
0.30

6X
0.66

2.50

0.65
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

6

XXXM▪

1

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 2 OF 2

PUBLICATION ORDERING INFORMATION

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