Genesys Logic, Inc.

GL3224

USB 3.1 Gen 1 Dual/Single LUN Memory Card Reader Controller

Datasheet

Revision 1.11
Dec. 25, 2019

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Revision History

Revision	Date	Description
1.00	01/14/2014	First formal release
1.01	01/15/2014	1. Remove CF, xD description in Chapter.2 p.7 2. Modify pin description in p.14
1.02	06/18/2014	Update SPI FLASH MEMORY SUPPORT LIST in Ch6, p22.
1.03	06/24/2014	Revise PACKAGE DIMENSION in Ch7, p23,24
1.04	05/07/2015	Modify Ch2 Features
1.05	08/05/2015	Update Table 5.4 Reset Timing, p.20
1.06	10/21/2015	Update CH7 Package Dimension, p.23,24
1.07	05/03/2016	Update CH2 Features
1.08	07/21/2017	Update CH6 SPI Flash Memory Support List
1.09	07/20/2018	1. Rename USB 3.0 to USB 3.1 Gen 1 2. Update CH1 General Description 3. Update CH2 Features 4. Update Table 3.1 - QFN48 Pin Description 5. Remove Table 5.6 - e•MMC Clock Frequency
1.10	01/04/2019	Update CH2 Features
1.11	12/25/2019	1. Add CH5.5 IC ESD/LU Level 2. Add CH5.6 Thermal information

Table of Contents

List of Figures

List of Tables

CHAPTER 1 GENERAL DESCRIPTION

The GL3224 is an USB 3.1 Gen1 Dual/Single LUN card reader controller, it provides 2 LUNs (Logic Unit Number) which can support various types of memory cards, such as Secure Digital™(SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), MS PRO Micro in one chip. It also supports SDXC and Memory Stick XC high density memory cards (capacity up to 2TB) and high speed SD 3.0 UHS-I memory cards.

The GL3224 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB port. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce system BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.1 Specification rev. 1.0 (USB 3.1 Gen 1)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Read In (1) / Bulk Data Write Out (2)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- Integrated USB building blocks
  - USB2.0 transceiver macrocell (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficient DMA hardware engine improves transfer rate between USB and flash card interfaces
- Support Ssecure Digital™ v1.0/ v1.1/ v2.0/ SDHC/ SDXC (Capacity up to 2TB)
- Support Secure Digital™ v3.01 UHS-I (Ultra High Speed): SDR12/ SDR25/ SDR50/ DDR50/ SDR104
- Support MultiMediaCard™ (MMC)
  - MMC specification v3.x/ v4.0/ v4.1/ v4.2
  - x1/ x4/ x8 bit data bus
- Support HUAWEI Nano Memory Card
- Support Memory Stick™/ Memory Stick PRO™/ Memory Stick PRO Duo™/ Memory Stick PRO Duo Mark2™/ Memory Stick Micro™ (M2)/ Memory Stick PRO-HG™/ Memory Stick PRO-HG Duo™/ Memory Stick PRO-HG Duo HX™
  - Compliant with Memory Stick Series Specification: MS v1.43, MS PRO v1.05, MS Micro v1.04 (MS HG Micro v1.00), MS PRO-HG Duo 1.03, MS XC Duo v1.00, MS XC-HG Duo v1.00, MS XC Micro v1.00 and MS XC-HG Micro v1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB interface
- On-Chip power MOSFETs for all flash media cards power source
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On board 25 MHz Crystal driver circuit
- Support USB 2.0 LPM (Link Power Management)
- Support USB 3.1 Gen 1 LTM (Latency Tolerance Messaging)
- Support USB 3.1 Gen 1 U1/U2/U3 low power link state
- Pass the USB-IF Test Procedure for SuperSpeed product (TID: 340890039)
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8.1 (Submission ID: 1620543)
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8 (Submission ID: 1620537)
- Pass WHQL (Windows Hardware Quality Lab) test for Windows 7 (Submission ID: 1620861)
- Support two SD3.0 interfaces with UHS-I: SDR12/ SDR25/ SDR50/ DDR50/ SDR104 bus mode
- Support programmable disable MMC interface
- Support programmable various LUN (Logic Unit Number): 2 LUNs and 1 LUN
- Support programmable SSC (Spread Spectrum Clocking), clock rate in SD, MS memory card interface for

better EMI test effect.

- Support programmable LED behavior, Read Only option for specific application
- Support power-saving mode to disconnect USB bus by card remove for better power management
- Support selective-suspend for entering suspend mode when data transfer pending after several seconds.
- Support Over-Current protection mechanism
- Available in QFN 48 pin package (7x7mm) for 2 LUNs SD 3.0
- Available in QFN 32 pin package (5x5mm) for 1 LUN SD3.0

CHAPTER 3 PIN ASSIGNMENT

3.1 QFN 48 Pinout

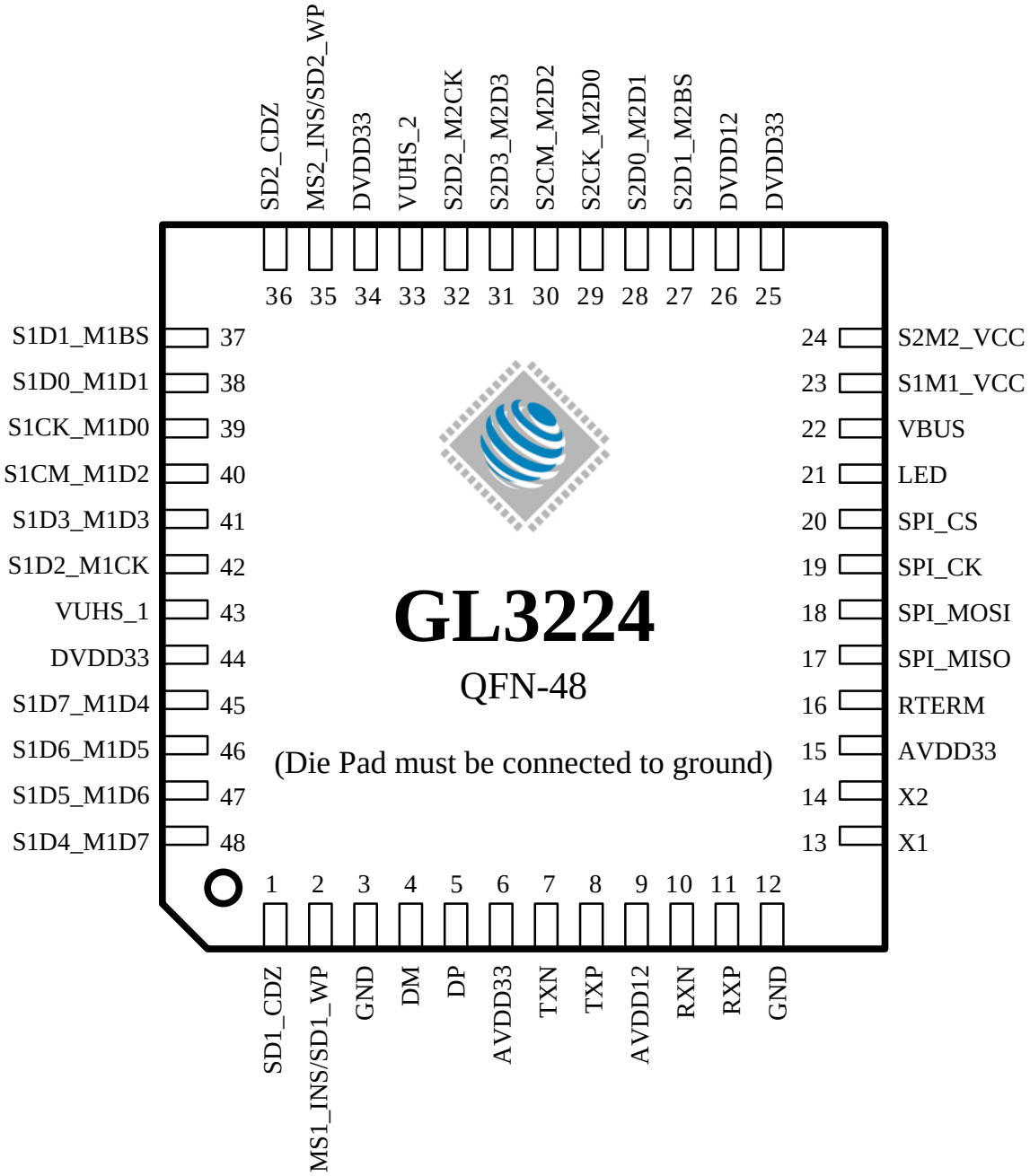


Figure 3.1 - QFN 48 Pinout Diagram

3.2 QFN 32 Pinout

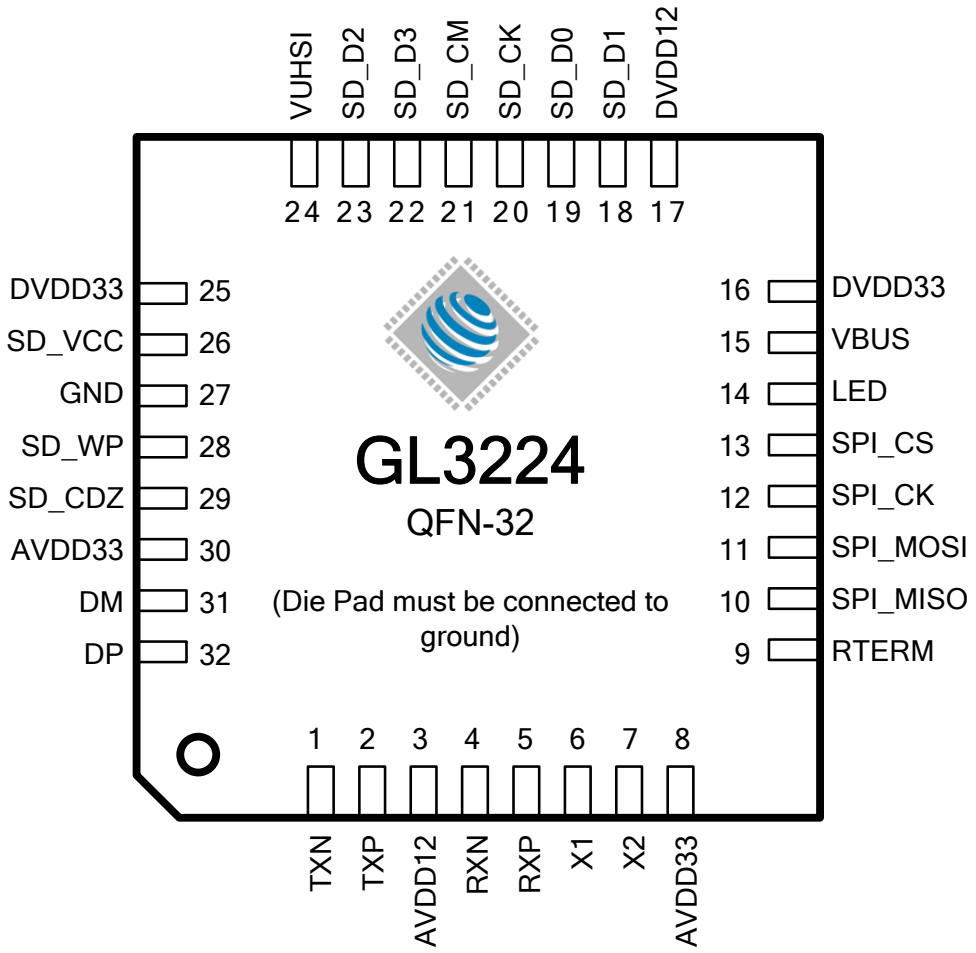


Figure 3.2 - QFN 32 Pinout Diagram

3.3 Pin Description

Table 3.1 - QFN 48 Pin Description

Pin Name	QFN 48	Type	Description
Power/Ground			
AVDD12	9	P	Analog 1.2V power source
AVDD33	6, 15	P	Analog 3.3V power source
DVDD12	26	P	Digital 1.2V power source
DVDD33	25, 34, 44	P	Digital 3.3V power source
VBUS	22	P	5V power source
VUHS_1	43	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3224 and no need of external power input
VUHS_2	33	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3224 and no need of external power input
S1M1_VCC	23	P	SD/MS card power
S2M2_VCC	24	P	SD/MS card power
GND	3, 12	P	Ground
USB PHY Interface			
DP	5	A	USB 2.0 D+
DM	4	A	USB 2.0 D-
TXN	7	A	USB 3.1 Gen 1 TX-
TXP	8	A	USB 3.1 Gen 1 TX+
RXN	10	A	USB 3.1 Gen 1 RX-
RXP	11	A	USB 3.1 Gen 1 RX+
RTERM	16	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be laid between RTERM and GND
X1	13	I	25MHz x'TAL input. It can be connected to external 25MHz clock input
X2	14	B	25MHz x'TAL output
Memory Card Interface			
MS1_INS/SD1_WP	2	I, pu	SD write protect 0: write enable 1: write protection
			MS insertion detect 0: Card insert 1: No card
MS2_INS/SD2_WP	35	I, pu	SD write protect 0: write enable 1: write protection
			MS insertion detect 0: Card insert 1: No card

SD1_CDZ	1	I, pu	SD card detect 0: Card insert 1: No card
SD2_CDZ	36	I, pu	SD card detect 0: Card insert 1: No card
S2D1_M2BS	27	B	SD data pin
		O	MS/MSP bus state
S2D0_M2D1	28	B	SD data pin
		B	MS/MSP data signal
S2CK_M2D0	29	O	SD clock
		B	MS/MSP data signal
S2CM_M2D2	30	B,pu	SD command/response
		B	MS/MSP data signal
S2D3_M2D3	31	B	SD data pin
		B	MS/MSP data signal
S2D2_M2CK	32	B	SD data pin
		O	MS clock
S1D1_M1BS	37	B	SD data pin
		O	MS/MSP bus state
S1D0_M1D1	38	B	SD data pin
		B	MS/MSP data signal
S1CK_M1D0	39	O	SD clock
		B	MS/MSP data signal
S1CM_M1D2	40	B,pu	SD command/response
		B	MS/MSP data signal
S1D3_M1D3	41	B	SD data pin
		B	MS/MSP data signal
S1D2_M1CK	42	B	SD data pin
		O	MS clock
S1D7_M1D4	45	B	SD data pin
		B	MS/MSP data signal
S1D6_M1D5	46	B	SD data pin
		B	MS/MSP data signal

S1D5_M1D6	47	B	SD data pin
		B	MS/MSP data signal
S1D4_M1D7	48	B	SD data pin
		B	MS/MSP data signal
Others			
LED	21	O	Memory card access LED
SPI_CS	20	O	SPI interface: chip select
SPI_CK	19	O	SPI interface: clock
SPI_MISO	17	I	SPI interface: connect to SPI flash data output
SPI_MOSI	18	O	SPI interface: connect to SPI flash data input

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

Table 3.2 - QFN 32 Pin Description

Pin Name	Pin NO.	Type	Description
Power/Ground			
AVDD12	3	P	Analog 1.2V power source
AVDD33	8,30	P	Analog 3.3V power source
DVDD12	17	P	Digital 1.2V power source
DVDD33	16,25	P	Digital 3.3V power source
VBUS	15	P	5V power source
VUHSI	24	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3224 and no need of external power input
SD_VCC	26	P	SD card power
GND	27	P	Ground
USB PHY Interface			
DP	32	A	USB 2.0 D+
DM	31	A	USB 2.0 D-
TXN	1	A	USB 3.1 Gen 1 TX-
TXP	2	A	USB 3.1 Gen 1 TX+
RXN	4	A	USB 3.1 Gen 1 RX-
RXP	5	A	USB 3.1 Gen 1 RX+
RTERM	9	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be laid between RREF and GND
X1	6	I	25MHz XTAL input. It can be connected to external 25MHz clock input
X2	7	B	25MHz XTAL output
Memory Card Interface			
SD_WP	28	I, pu	SD write protect 0: write enable 1: write protection
SD_CDZ	29	I, pu	SD card detect 0: Card insert 1: No card
SD_D1	18	B	SD data pin
SD_D0	19	B	SD data pin
SD_CK	20	O	SD clock
SD_CM	21	B,pu	SD command/response
SD_D3	22	B	SD data pin
SD_D2	23	B	SD data pin

Others			
LED	14	O	Memory card access LED
SPI_CS	13	O	SPI interface: chip select
SPI_CK	12	O	SPI interface: clock
SPI_MISO	10	I	SPI interface: Connect to SPI flash data output
SPI_MOSI	11	O	SPI interface: Connect to SPI flash data input

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

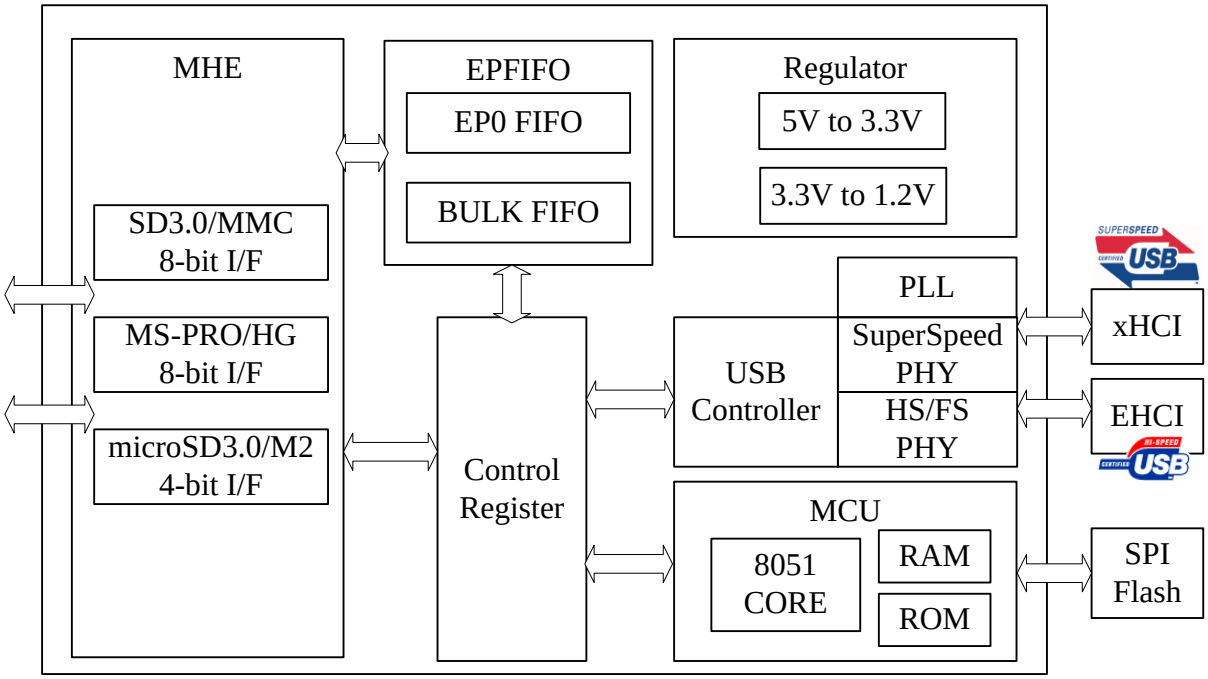


Figure 4.1 - QFN 48 Functional Block Diagram

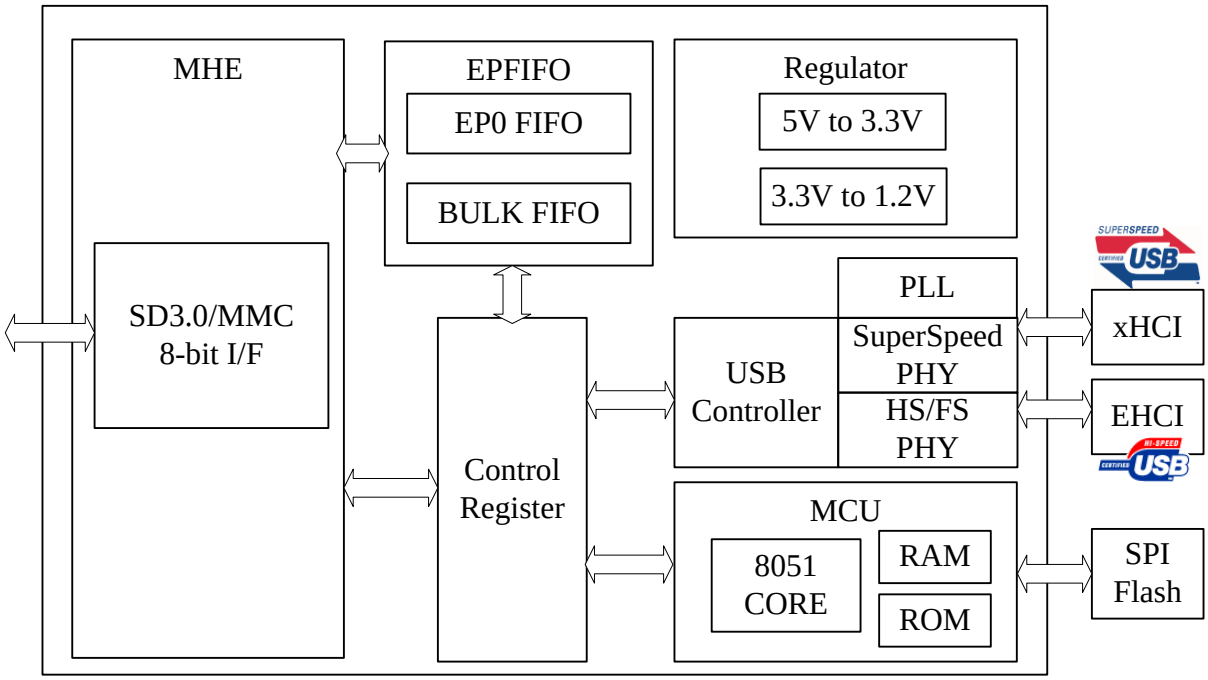


Figure 4.2 - QFN 32 Functional Block Diagram

4.1 Super Speed and HS/FS PHY

The transceiver macro cell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.1 GEN 1 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: SD/MMC/MS/MS PRO/MS PRO-HG

4.6 Regulator

- **5V to 3.3V** 3.3V Power source
- **3.3V to 1.2V** 1.2V Power source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10		10	μA
V_{OH}	Output High Voltage	DVDD = 3.3V	2.8			V
V_{OL}	Output Low Voltage				0.4	V
I_{OH}	Output Current High			8		mA
I_{OL}	Output Current Low			8		mA
C_{IN}	Input Pin Capacitance			5		pF
I_{NORMAL}	HS mode			43		mA
	SS mode	U0 state		120		mA
		U1 state		27		mA
		U2 state		13		mA
I_{ACTIVE}	HS mode			65		mA
	SS mode	U0 state		147		mA
I_{RESET}				40		mA

I_{SUS}	Suspend current	1.5K pull-up included		0.85		mA
	SS Suspend current	U3 state		0.7		mA
R_{pu}	Reset Pad pull-up			46		KΩ
	SD_CDZ, SD_WP, MS_INS, GPIO Pad pull-up			46		KΩ
	SD_CMD pull-up			15		KΩ
	SD_CLK, D[3:0] Pad pull-up			15		KΩ
R_{pd}	SD_CMD pull-down			15		KΩ
	SD_CLK, D[3:0] Pad pull-down			15		KΩ
R_{IMP}	SD_CMD, SD_CLK, D[3:0] impedances			50		Ω

5.4 AC Characteristics of Reset Timing

5.4.1 Reset Timing

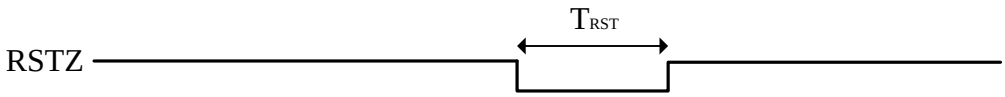


Figure 5.1 - Timing Diagram of Reset Width

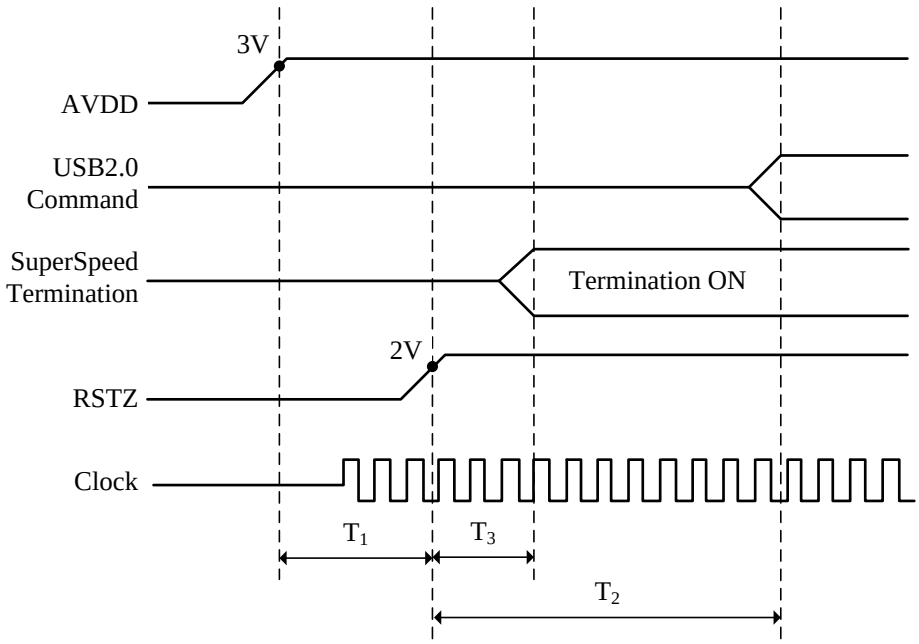


Figure 5.2 - Timing Diagram of Power Good to USB Command Receive Ready

Table 5.4 - Reset Timing

Parameter	Description	Min.	Min.	Unit
T_{RST}	Chip reset sense timing width	2		us
T1	AVDD power up to reset de-assert	500		us
T2	Reset de-assert to respond USB command ready		95	ms
T3	Reset de-assert to SuperSpeed termination on		12	ms

5.4.2 SD/MMC Card Clock Frequency

Table 5.5 - SD/MMC Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	400	KHz
F_{DS}	Clock frequency Default Speed Mode	25	MHz
F_{HS}	SD Clock frequency High Speed Mode	50	MHz
F_{HS}	MMC Clock frequency High Speed Mode	52	MHz
F_{SDR25}	Clock frequency Ultra High Speed Mode: SDR25	50	MHz
F_{DDR50}	Clock frequency Ultra High Speed Mode: DDR50	50	MHz
F_{SDR50}	Clock frequency Ultra High Speed Mode: SDR50	100	MHz
F_{SDR104}	Clock frequency Ultra High Speed Mode: SDR104	208	MHz

5.4.3 MS Card Clock Frequency

Table 5.6 - MS Card Clock Frequency

Parameter	Description	Max.	Unit
F_{DS}	Clock frequency Default Speed Mode	20	MHz
F_{MSP}	Clock frequency MS PRO 4bit Mode	40	MHz
F_{MSPHG}	Clock frequency MS PRO HG 8bit Mode	60	MHz

5.5 IC ESD/LU Level

Table 5.7 - IC ESD/LU Level

Test Mode and Trigger Mode	Value
ESD HBM	± 4KV
ESD CDM	± 500V
ESD MM	± 200V
Latch-up	± 500mA

5.6 Thermal information

Table 5.8 - Thermal information (QFN48)

Ambient Temp (T_a)	Power (P)	Thermal Resistance (Θ_{ja})	Thermal Resistance (Θ_{jc})	Junction Temp (T_j)	Case Temp (T_c)
70℃	0.750W	33.23°C/W	5.31°C/W	94.9°C	90.9°C

Table 5.9 - Thermal information (QFN32)

Ambient Temp (T_a)	Power (P)	Thermal Resistance (Θ_{ja})	Thermal Resistance (Θ_{jc})	Junction Temp (T_j)	Case Temp (T_c)
70℃	0.750W	35.9°C/W	6.1°C/W	96.9°C	92.3°C

CHAPTER 6 SPI FLASH MEMORY SUPPORT LIST

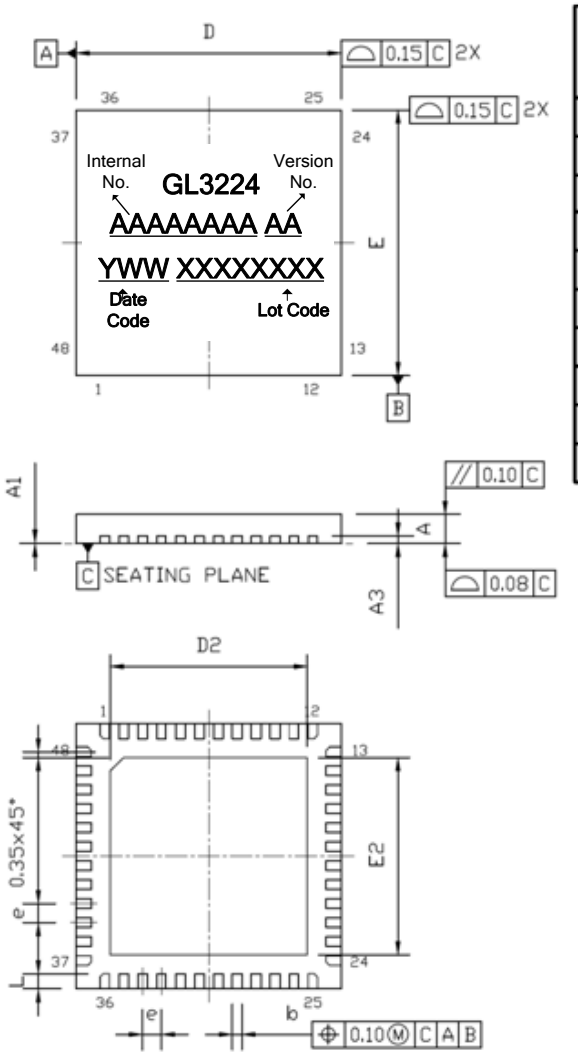
Table 6.1 - SPI Flash Memory Support List

Vendor	Model
GigaDevice	GD25Q512
	GD25Q010
	GD25Q040
PMC	PM25LD512C
	PM25LD010
	PM25LD010C
	PM25LD020
	PM25LD020C
WINBON	W25X05CL
	W25X10CL
	W25X10BV
	W25X20CL
	W25X20BV
EON	EN25Q40
MXIC	MX25L1006E
ESMT	F25L01PA-86PG
	F25L01PA-100PG
Giantec	GT25F512
FMSH	FM25F005
	FM25F01

Note :

- GL3224 support Page-Program SPI Flash Memory only, does not support Byte-program SPI Flash Memory
- The density of SPI Flash Memory shall be larger than or equal to 512Kbit.
- Firmware file (xxxx.bin) which Genesys Logic provided is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW to SPI Flash vendor for pre-loading or Flash ROM writer usage, please contact to GL technical support team.

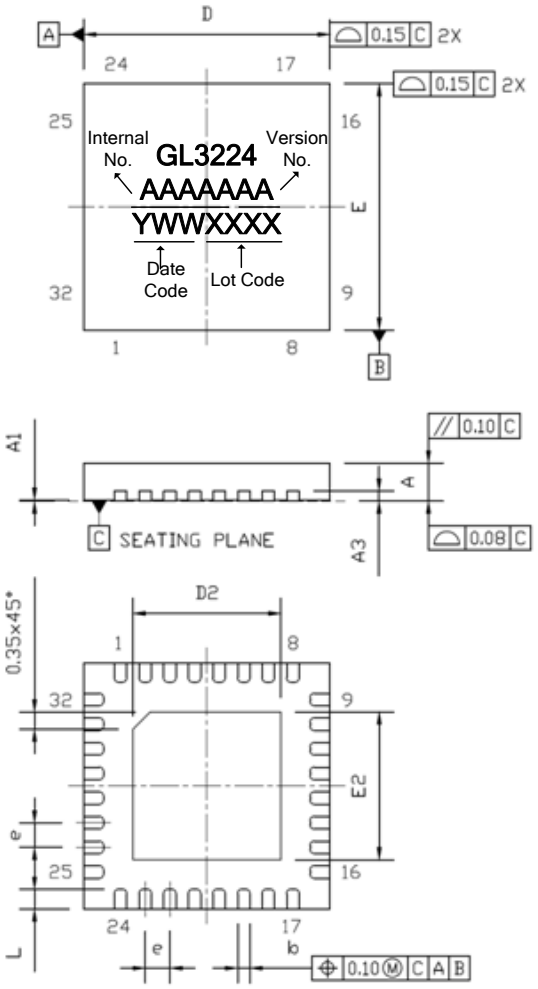
CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	7.00 (275.6) BSC		
D2	5.10 (200.8)	5.20 (204.7)	5.30 (208.7)
E	7.00 (275.6) BSC		
E2	5.10 (200.8)	5.20 (204.7)	5.30 (208.7)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.1 - QFN 48 Pin Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	5.00 (196.9) BSC		
D2	2.60 (102.4)	3.00 (118.1)	3.30 (129.9)
E	5.00 (196.9) BSC		
E2	2.60 (102.4)	3.00 (118.1)	3.30 (129.9)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.2 - QFN 32 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3224-ONYXX	QFN 48	Green Package + CU Wire	XX	Available
GL3224-OIYXX	QFN 32	Green Package + CU Wire	XX	Available