AiP74AVC8T245
8-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2019-03-A1	2019-03	New
2021-12-A2	2021-12	Modify Ordering Information
2022-02-A3	2022-02	Modify ambient temperature to -40℃~+105℃ and add electrical characteristics of -40℃~+105℃
2022-04-A4	2022-04	Add TSSOP24 reel packing specifications

1、General Description

The AiP74AVC8T245 is an 8-bit, dual supply transceiver that enables bidirectional level translation. It features two 8-bit input-output ports (An and Bn), a direction control input (DIR), a output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V,1.2V,1.5V,1.8V,2.5V and 3.3V).Pins An, $\overline{OE}$ and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both An and Bn are in the high-impedance OFF-state.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 0.8V to 3.6V
  $V_{CC(B)}$: 0.8V to 3.6V
- Maximum data rates:
  380 Mbit/s (≥1.8V to 3.3V translation)
  260 Mbit/s (≥1.1V to 3.3V translation)
  260 Mbit/s (≥1.1V to 2.5V translation)
  210 Mbit/s (≥1.1V to 1.8V translation)
  150 Mbit/s (≥1.1V to 1.5V translation)
  100 Mbit/s (≥1.1V to 1.2V translation)
- Suspend mode
- Inputs accept voltages up to 3.6V
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40℃ to +105℃
- Packaging information: TSSOP24/DHVQFN24

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74AVC8T245 TA24.TB	TSSOP24	74AVC8T245	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74AVC8T245 QE24.TR	DHVQFN24	74AVC8T245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 5.5mm×3.5mm Pin spacing:0.5mm
AiP74AVC8T245 TA24.TR	TSSOP24	74AVC8T245	3000 PCS/reel	6000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

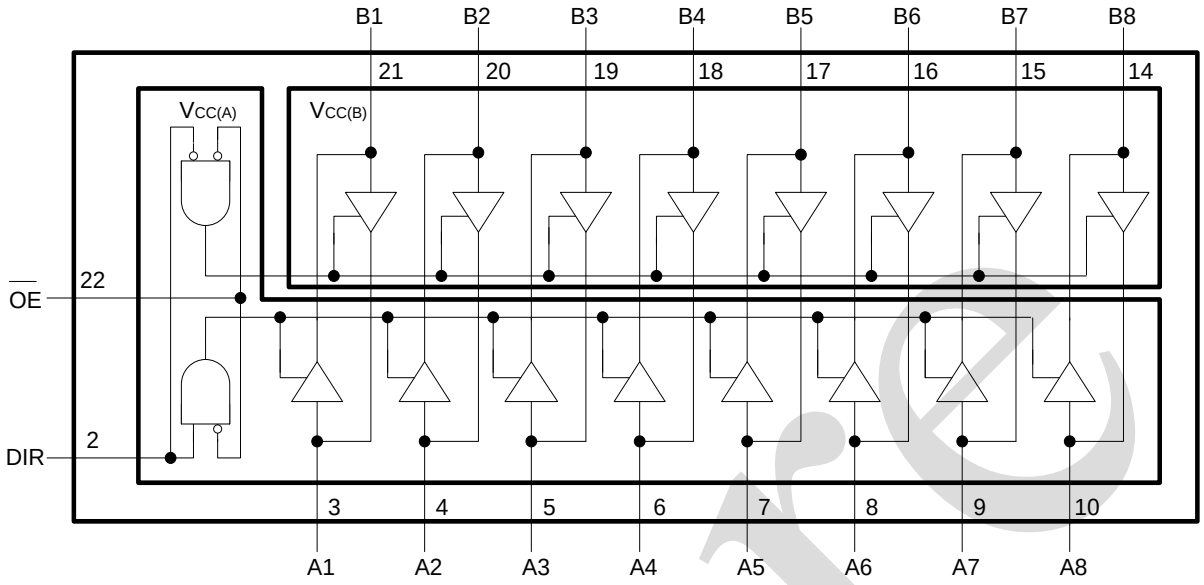


Figure 1. Logic symbol

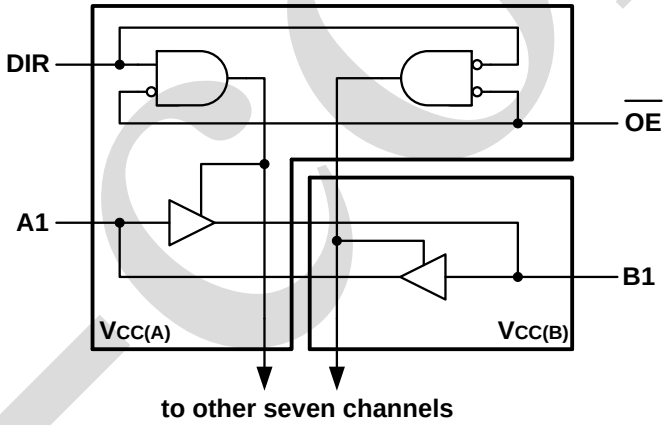
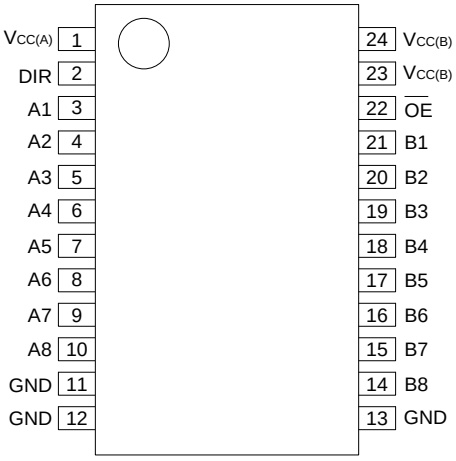
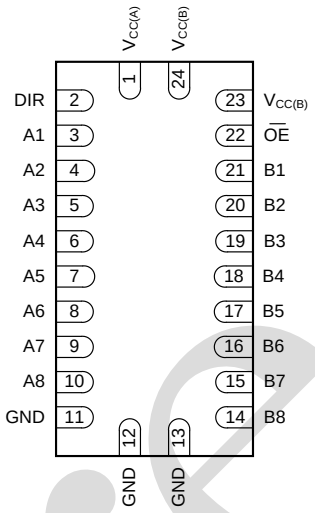


Figure 2. Logic diagram

2.2、Pin Configurations



TSSOP24



DHVQFN24

2.3、Pin Description

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A (An, $\overline{OE}$ and DIR inputs are referenced to $V_{CC(A)}$)
2	DIR	direction control
3,4,5,6,7,8,9,10	A1 to A8	data input or output
11	GND[1]	ground (0V)
12	GND[1]	ground (0V)
13	GND[1]	ground (0V)
21,20,19,18,17,16,15,14	B1 to B8	data input or output
22	$\overline{OE}$	output enable input (active LOW)
23	$V_{CC(B)}$	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$)
24	$V_{CC(B)}$	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$)

Note: All GND pins must be connected to ground (0V).

2.4、Function Table[1]

Supply voltage	Input		Input/output[3]	
$V_{CC(A)}$,$V_{CC(B)}$	$\overline{OE}$[2]	DIR[2]	An[2]	Bn
0.8V to 3.6V	L	L	An=Bn	input
0.8V to 3.6V	L	H	input	Bn=An
0.8V to 3.6V	H	X	Z	Z
GND[3]	X	X	Z	Z

Note:

[1]H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2]The An, DIR and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

[3]If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+4.6	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+4.6	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+4.6	V
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output voltage	V_O	Active mode[1][2][3]	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode[1]	-0.5	+4.6	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA
ground current	I_{GND}	per GND pin	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-[4]	-	500	mW
Soldering temperature	T_L	10s	250		℃

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO}+0.5V should not exceed 4.6V.

[4] For TSSOP24 package: P_{tot} derates linearly at 5.5mW/K above 60℃.
For DHVQFN24 package: P_{tot} derates linearly at 4.5mW/K above 60℃.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	0.8	-	3.6	V
supply voltage B	$V_{CC(B)}$	-	0.8	-	3.6	V
input voltage	V_I	-	0	-	3.6	V
output voltage	V_O	Active mode[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	3.6	V
ambient temperature	T_{amb}	-	-40	-	+105	℃
input transition rise and fall rate	Δt/ΔV	V_{CCI}=0.8V to 3.6V[2]	-	-	5	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)[1][2]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-1.5mA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V	-	0.69	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=1.5mA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V	-	0.07	-	V
input leakage current	I_I	DIR, $\overline{OE}$ input; V_I=0V to 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V		-	±0.025	±0.25	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=$V_{CC(B)}$=3.6V[3]		-	±0.5	±2.5	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V[3]		-	±0.5	±2.5	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V[3]		-	±0.5	±2.5	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0.8V to 3.6V		-	±0.1	±1	uA
		B port; V_I or V_O=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0.8V to 3.6V		-	±0.1	±1	uA
input capacitance	C_I	DIR, $\overline{OE}$ input; V_I=0V or 3.3V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V		-	1.5	-	pF
input/output capacitance	$C_{I/O}$	A and B port; V_O=3.3V or 0V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V		-	4.3	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)[1][2]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input	V_{CCI}=0.8V	0.70V_{CCI}	-	-	V
			V_{CCI}=1.1V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.6	-	-	V
			V_{CCI}=3.0V to 3.6V	2	-	-	V
		DIR, $\overline{OE}$ input	$V_{CC(A)}$=0.8V	0.70$V_{CC(A)}$	-	-	V
			$V_{CC(A)}$=1.1V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			$V_{CC(A)}$=2.3V to 2.7V	1.6	-	-	V
			$V_{CC(A)}$=3.0V to 3.6V	2	-	-	V
LOW-level input voltage	V_{IL}	data input	V_{CCI}=0.8V	-	-	0.30V_{CCI}	V
			V_{CCI}=1.1V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
		DIR, $\overline{OE}$ input	$V_{CC(A)}$=0.8V	-	-	0.30$V_{CC(A)}$	V
			$V_{CC(A)}$=1.1V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			$V_{CC(A)}$=2.3V to 2.7V	-	-	0.7	V

			$V_{CC(A)}$=3.0V to 3.6V	-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V	V_{CCO}-0.1	-	-	V
			I_O=-3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V	0.85	-	-	V
			I_O=-6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V	1.05	-	-	V
			I_O=-8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V	1.2	-	-	V
			I_O=-9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V	1.75			V
			I_O=-12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V	2.3	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V	-	-	0.1	V
			I_O=3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V	-	-	0.25	V
			I_O=6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V	-	-	0.35	V
			I_O=8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V	-	-	0.45	V
			I_O=9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V	-	-	0.55	V
			I_O=12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V	-	-	0.7	V
input leakage current	I_I	DIR, $\overline{OE}$ input;V_I=0V or 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V		-	-	±1	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=$V_{CC(B)}$=3.6V[3]		-	-	±5	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V[3]		-	-	±5	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V[3]		-	-	±5	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V;$V_{CC(B)}$=0.8V to 3.6V		-	-	±5	uA
		B port; V_I or V_O=0V to 3.6V; $V_{CC(B)}$=0V;$V_{CC(A)}$=0.8V to 3.6V		-	-	±5	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V	-	-	10	uA
			$V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V	-	-	8	uA
			$V_{CC(A)}$=3.6V;$V_{CC(B)}$=0V	-	-	8	uA

			$V_{CC(A)}$=0V;$V_{CC(B)}$=3.6V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V	-	-	10	uA
			$V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V	-	-	8	uA
			$V_{CC(A)}$=3.6V;$V_{CC(B)}$=0V	-2	-	-	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=3.6V	-	-	8	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A;V_I=0V or V_{CCI}; $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V		-	-	20	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A;V_I=0V or V_{CCI}; $V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V		-	-	16	uA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)[1][2]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input	V_{CCI}=0.8V	0.70V_{CCI}	-	-	V
			V_{CCI}=1.1V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.6	-	-	V
			V_{CCI}=3.0V to 3.6V	2	-	-	V
		DIR, $\overline{OE}$ input	$V_{CC(A)}$=0.8V	0.70$V_{CC(A)}$	-	-	V
			$V_{CC(A)}$=1.1V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			$V_{CC(A)}$=2.3V to 2.7V	1.6	-	-	V
			$V_{CC(A)}$=3.0V to 3.6V	2	-	-	V
LOW-level input voltage	V_{IL}	data input	V_{CCI}=0.8V	-	-	0.30V_{CCI}	V
			V_{CCI}=1.1V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
		DIR, $\overline{OE}$ input	$V_{CC(A)}$=0.8V	-	-	0.30$V_{CC(A)}$	V
			$V_{CC(A)}$=1.1V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			$V_{CC(A)}$=2.3V to 2.7V	-	-	0.7	V
			$V_{CC(A)}$=3.0V to 3.6V	-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V	V_{CCO}-0.1	-	-	V
			I_O=-3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V	0.85	-	-	V
			I_O=-6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V	1.05	-	-	V

			I_O=-8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V	1.2	-	-	V
			I_O=-9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V	1.75			V
			I_O=-12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V	2.3	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V	-	-	0.1	V
			I_O=3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V	-	-	0.25	V
			I_O=6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V	-	-	0.35	V
			I_O=8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V	-	-	0.45	V
			I_O=9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V	-	-	0.55	V
			I_O=12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V	-	-	0.7	V
input leakage current	I_I	DIR, $\overline{OE}$ input;V_I=0V or 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V		-	-	±5	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=$V_{CC(B)}$=3.6V[3]		-	-	±30	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V[3]		-	-	±30	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V[3]		-	-	±30	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V;$V_{CC(B)}$=0.8V to 3.6V		-	-	±30	uA
		B port; V_I or V_O=0V to 3.6V; $V_{CC(B)}$=0V;$V_{CC(A)}$=0.8V to 3.6V		-	-	±30	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V	-	-	55	uA
			$V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V	-	-	50	uA
			$V_{CC(A)}$=3.6V;$V_{CC(B)}$=0V	-	-	50	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=3.6V	-12	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V	-	-	55	uA
			$V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V	-	-	50	uA
			$V_{CC(A)}$=3.6V;$V_{CC(B)}$=0V	-12	-	-	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=3.6V	-	-	50	uA

		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A;V_I=0V or V_{CCI}; $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V	-	-	70	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A;V_I=0V or V_{CCI}; $V_{CC(A)}$=1.1V to 3.6V; $V_{CC(B)}$=1.1V to 3.6V	-	-	65	uA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

3.3.4、Typical total supply current ($I_{CC(A)}$+$I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0V	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	0.1	0.1	0.1	0.1	0.1	0.1	uA
0.8V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	uA
1.2V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	uA
1.5V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	uA
1.8V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	uA
2.5V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	uA
3.3V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	uA

3.3.5、AC Characteristics 1

($V_{CC(A)}$=0.8V and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	An to Bn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		Bn to An	14.4	12.4	12.1	11.9	11.8	11.8	ns
disable time	t_{dis}	$\overline{OE}$ to An	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{OE}$ to Bn	17.6	10.0	9.0	9.1	8.7	9.3	ns
enable time	t_{en}	$\overline{OE}$ to An	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{OE}$ to Bn	22.2	11.1	9.8	9.4	9.4	9.6	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.6、AC Characteristics 2

($V_{CC(B)}$=0.8V and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	An to Bn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		Bn to An	14.4	7.0	6.2	6.0	5.9	6.0	ns
disable time	t_{dis}	$\overline{OE}$ to An	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{OE}$ to Bn	17.6	14.2	13.7	13.6	13.3	13.1	ns
enable time	t_{en}	$\overline{OE}$ to An	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{OE}$ to Bn	22.2	17.7	17.2	17.0	16.8	16.7	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.7、AC Characteristics 3

($V_{CC(A)}$=$V_{CC(B)}$ and T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}$=$V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
power dissipation capacitance	C_{PD}	A port: (direction An to Bn);output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction An to Bn);output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction Bn to An);output enabled	9	9	10	10	11	13	pF
		A port: (direction Bn to An);output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction An to Bn);output enabled	9	9	10	10	11	13	pF
		B port: (direction An to Bn);output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction Bn to An);output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		B port: (direction Bn to An);output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF

Note:

C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs.

f_i=10MHz; V_I=GND to V_{CC}; $t_r=t_f$=1ns; C_L=0pF; $R_L=\infty\Omega$.

3.3.8、DC Characteristics 4

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$ 1.2V±0.1V		1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.1V to 1.3V													
propagation delay	t_{pd}	An to Bn	0.5	9.0	0.5	6.7	0.5	5.8	0.5	4.9	0.5	4.8	ns
		Bn to An	0.5	9.0	0.5	8.5	0.5	8.3	0.5	8.0	0.5	7.8	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	ns
		$\overline{OE}$ to Bn	0.5	12.3	0.5	9.5	0.5	9.4	0.5	8.0	0.5	8.9	ns
enable time	t_{en}	$\overline{OE}$ to An	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	ns
		$\overline{OE}$ to Bn	1.1	14.2	1.1	10.4	1.1	9.0	1.0	7.7	1.0	7.3	ns
$V_{CC(A)}$=1.4V to 1.6V													
propagation delay	t_{pd}	An to Bn	0.5	8.5	0.5	5.6	0.5	4.7	0.5	4.4	0.5	4.1	ns
		Bn to An	0.5	6.7	0.5	5.6	0.5	5.3	0.5	5.2	0.5	5.0	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
enable time	t_{en}	$\overline{OE}$ to An	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
		$\overline{OE}$ to Bn	1.1	12.8	1.1	8.1	1.1	7.1	1.0	5.6	1.0	5.2	ns
$V_{CC(A)}$=1.65V to 1.95V													
propagation delay	t_{pd}	An to Bn	0.5	8.3	0.5	5.3	0.5	4.5	0.5	3.8	0.5	3.5	ns
		Bn to An	0.5	5.8	0.5	4.7	0.5	4.5	0.5	4.3	0.5	4.1	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
		$\overline{OE}$ to Bn	0.5	10.9	0.5	7.8	0.5	6.9	0.5	6.0	0.5	5.8	ns
enable time	t_{en}	$\overline{OE}$ to An	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		$\overline{OE}$ to Bn	1.1	12.4	1.1	8.2	1.0	6.7	0.5	5.1	0.5	4.5	ns
$V_{CC(A)}$=2.3V to 2.7V													
propagation delay	t_{pd}	An to Bn	0.5	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		Bn to An	0.5	4.9	0.5	4.4	0.5	3.8	0.5	3.3	0.5	3.1	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
		$\overline{OE}$ to Bn	0.5	10.4	0.5	7.1	0.5	6.3	0.5	5.1	0.5	5.2	ns
enable time	t_{en}	$\overline{OE}$ to An	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
		$\overline{OE}$ to Bn	1.1	11.9	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4.0	ns
$V_{CC(A)}$=3.0V to 3.6V													
propagation delay	t_{pd}	An to Bn	0.5	7.8	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		Bn to An	0.5	4.8	0.5	4.1	0.5	3.5	0.5	2.9	0.5	2.7	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	ns
		$\overline{OE}$ to Bn	0.5	10.1	0.5	6.9	0.5	6.0	0.5	4.8	0.5	5.0	ns
enable time	t_{en}	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.1	11.7	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

3.3.9、DC Characteristics 5

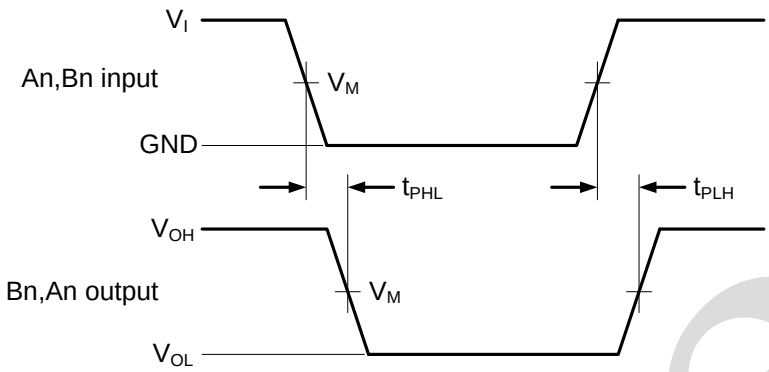
(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.2V±0.1V		1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.1V to 1.3V													
propagation delay	t_{pd}	An to Bn	0.5	9.9	0.5	7.4	0.5	6.4	0.5	5.4	0.5	5.3	ns
		Bn to An	0.5	9.9	0.5	9.4	0.5	9.2	0.5	8.8	0.5	8.6	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	ns
		$\overline{OE}$ to Bn	0.5	13.6	0.5	10.5	0.5	10.4	0.5	8.8	0.5	9.8	ns
enable time	t_{en}	$\overline{OE}$ to An	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	ns
		$\overline{OE}$ to Bn	1.1	15.7	1.1	11.5	1.1	9.9	1.0	8.5	1.0	8.1	ns
$V_{CC(A)}$=1.4V to 1.6V													
propagation delay	t_{pd}	An to Bn	0.5	9.4	0.5	6.2	0.5	5.2	0.5	4.9	0.5	4.6	ns
		Bn to An	0.5	7.4	0.5	6.2	0.5	5.9	0.5	5.8	0.5	5.5	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	ns
		$\overline{OE}$ to Bn	0.5	12.4	0.5	9.3	0.5	8.4	0.5	8.0	0.5	8.6	ns
enable time	t_{en}	$\overline{OE}$ to An	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	ns
		$\overline{OE}$ to Bn	1.1	14.1	1.1	9.0	1.1	7.9	1.0	6.2	1.0	5.8	ns
$V_{CC(A)}$=1.65V to 1.95V													
propagation delay	t_{pd}	An to Bn	0.5	9.2	0.5	5.9	0.5	5.0	0.5	4.2	0.5	3.9	ns
		Bn to An	0.5	6.4	0.5	5.2	0.5	5.0	0.5	4.8	0.5	4.6	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	ns
		$\overline{OE}$ to Bn	0.5	12.0	0.5	8.6	0.5	7.6	0.5	6.6	0.5	6.4	ns
enable time	t_{en}	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	1.1	13.7	1.1	9.1	1.0	7.4	0.5	5.7	0.5	5.0	ns
$V_{CC(A)}$=2.3V to 2.7V													
propagation delay	t_{pd}	An to Bn	0.5	8.8	0.5	5.8	0.5	4.8	0.5	3.7	0.5	3.2	ns
		Bn to An	0.5	5.4	0.5	4.9	0.5	4.2	0.5	3.7	0.5	3.5	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	0.5	11.5	0.5	7.9	0.5	7.0	0.5	5.7	0.5	5.8	ns
enable time	t_{en}	$\overline{OE}$ to An	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		$\overline{OE}$ to Bn	1.1	13.1	1.1	8.7	0.5	7.1	0.5	5.1	0.5	4.4	ns
$V_{CC(A)}$=3.0V to 3.6V													
propagation delay	t_{pd}	An to Bn	0.5	8.6	0.5	5.5	0.5	4.6	0.5	3.5	0.5	3.0	ns
		Bn to An	0.5	5.3	0.5	4.6	0.5	3.9	0.5	3.2	0.5	3.0	ns
disable time	t_{dis}	$\overline{OE}$ to An	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	7.6	0.5	6.6	0.5	5.3	0.5	5.5	ns
enable time	t_{en}	$\overline{OE}$ to An	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	ns
		$\overline{OE}$ to Bn	1.1	12.9	1.1	8.6	0.5	6.9	0.5	5.0	0.5	4.3	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

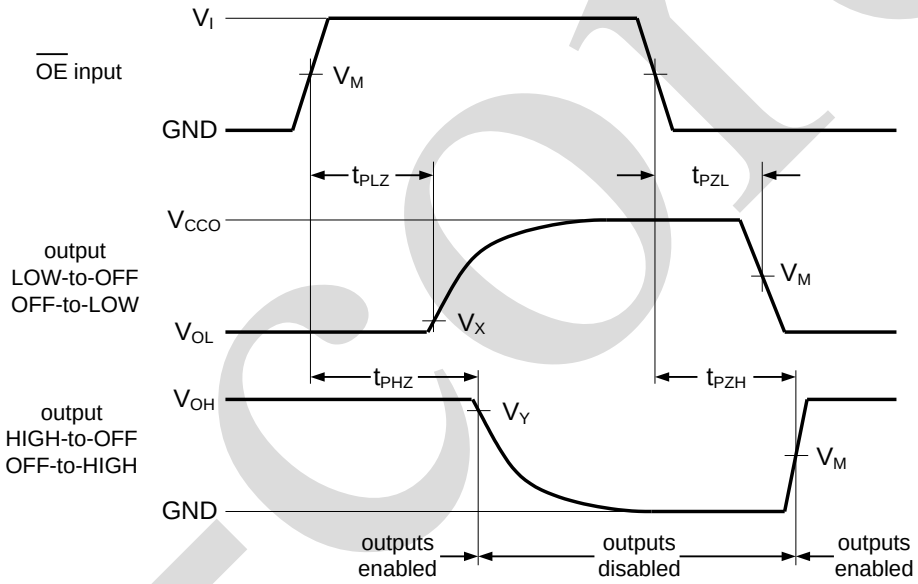
4、Testing Circuit

4.1、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times

4.2、Measurement Points

Supply voltage	**Input[1]**	**Output[2]**		
$V_{CC(A)}$,$V_{CC(B)}$	**V_M**	**V_M**	**V_X**	**V_Y**
0.8V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 3.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

4.3、AC Testing Circuit

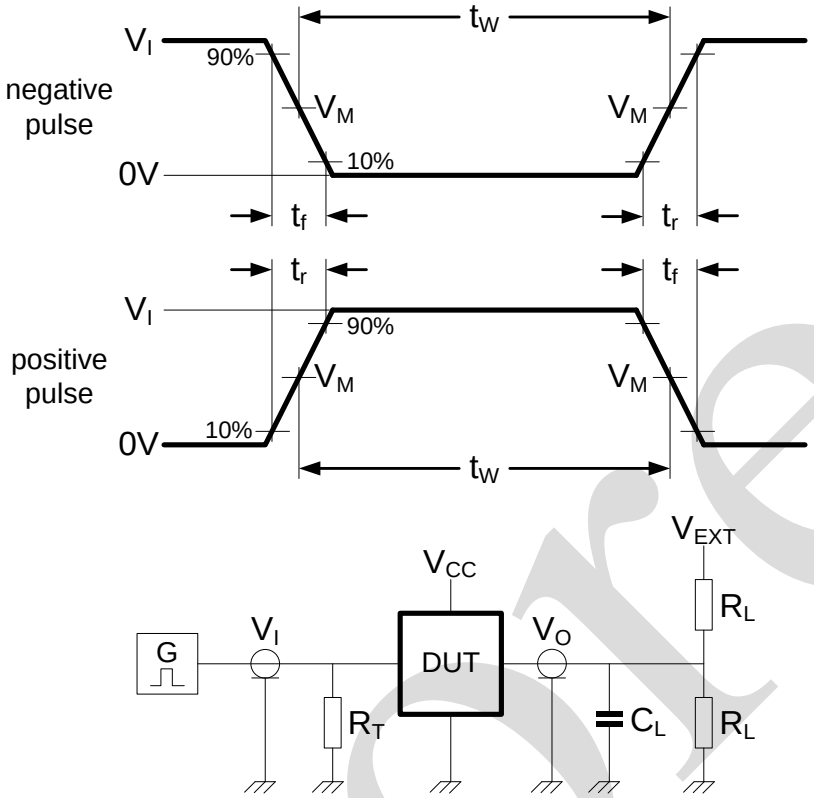


Figure 5. Load circuitry for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$,$V_{CC(B)}$	V_I[1]	Δt/ΔV[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
0.8V to 1.6V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$
1.65V to 2.7V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$
3.0V to 3.6V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$

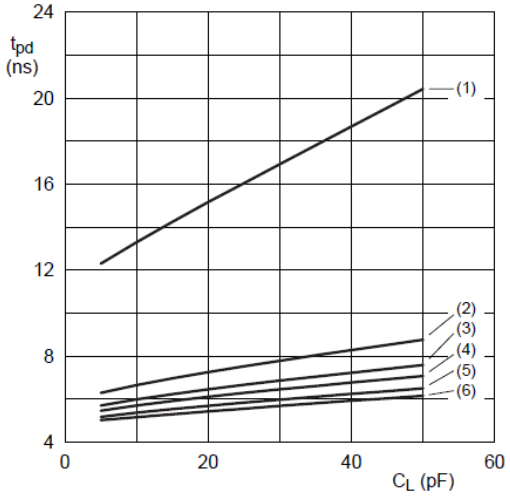
Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] dV/dt≥1.0V/ns.

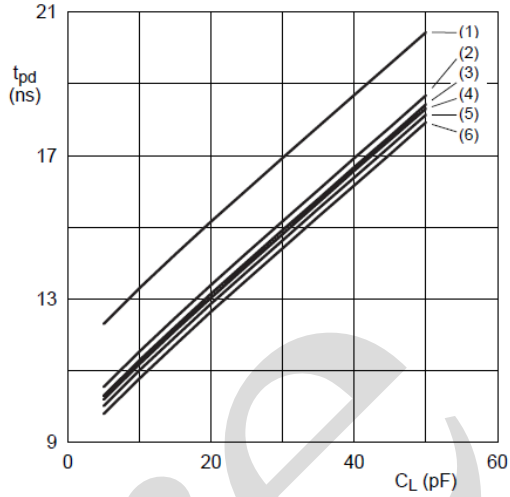
[3] V_{CCO} is the supply voltage associated with the output port.

5、Characteristic Curve



a. Propagation delay (An to Bn); $V_{CC(A)}$=0.8V

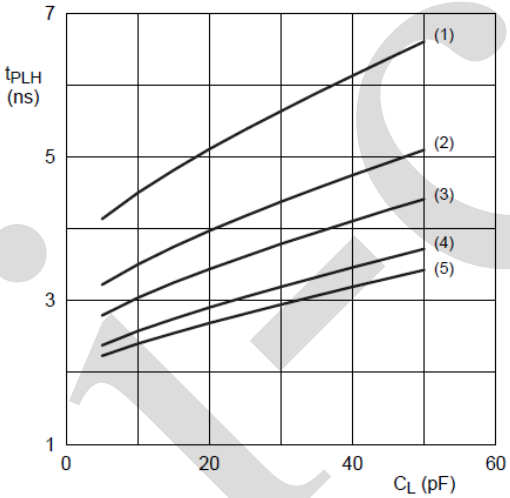
(1) $V_{CC(B)}$=0.8V.
(2) $V_{CC(B)}$=1.2V.
(3) $V_{CC(B)}$=1.5V.
(4) $V_{CC(B)}$=1.8V.
(5) $V_{CC(B)}$=2.5V.
(6) $V_{CC(B)}$=3.3V.



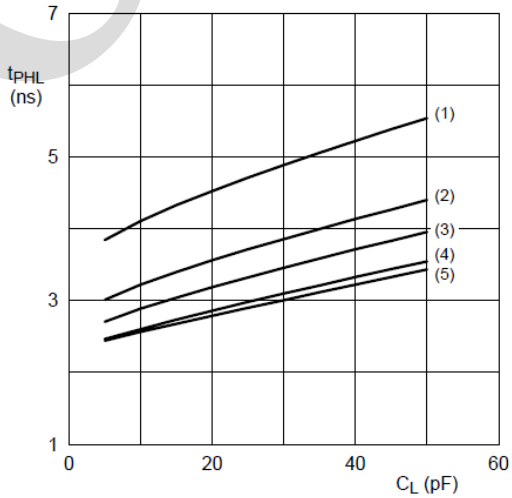
b. Propagation delay (An to Bn); $V_{CC(B)}$=0.8V

(1) $V_{CC(A)}$=0.8V.
(2) $V_{CC(A)}$=1.2V.
(3) $V_{CC(A)}$=1.5V.
(4) $V_{CC(A)}$=1.8V.
(5) $V_{CC(A)}$=2.5V.
(6) $V_{CC(A)}$=3.3V.

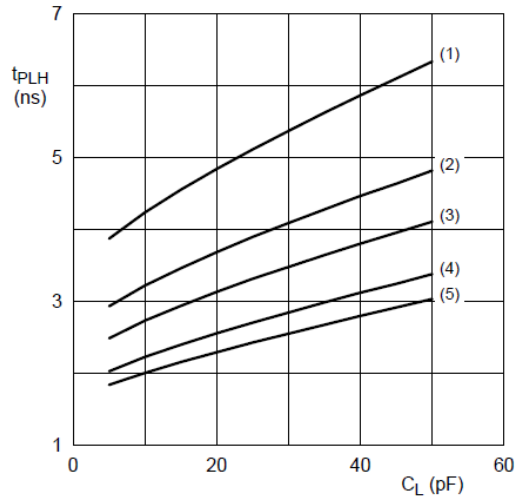
Figure 6. Typical propagation delay versus load capacitance; T_{amb}=25℃



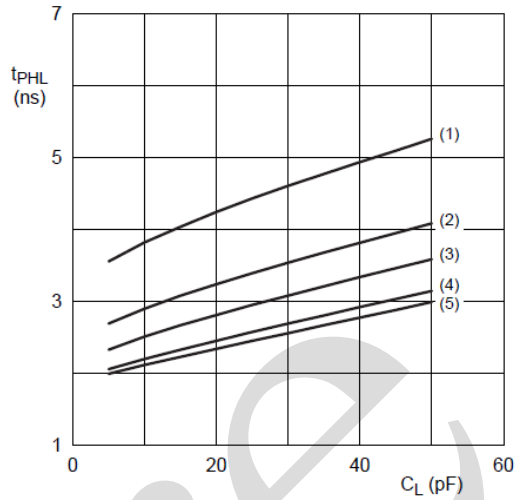
a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$=1.2V



b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$=1.2V



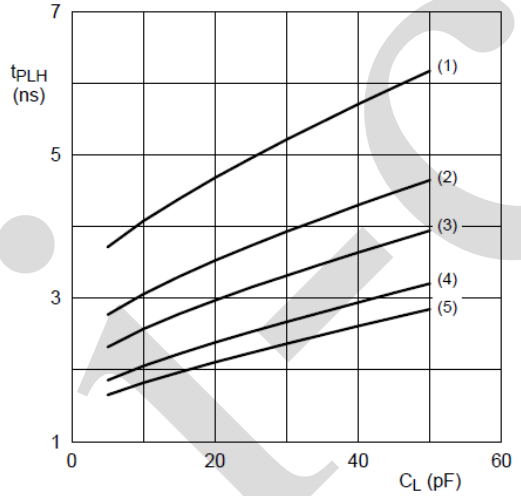
c. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$=1.5V



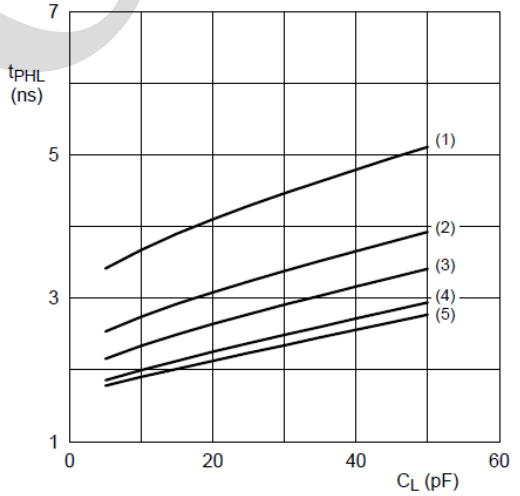
d. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$=1.5V

(1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.

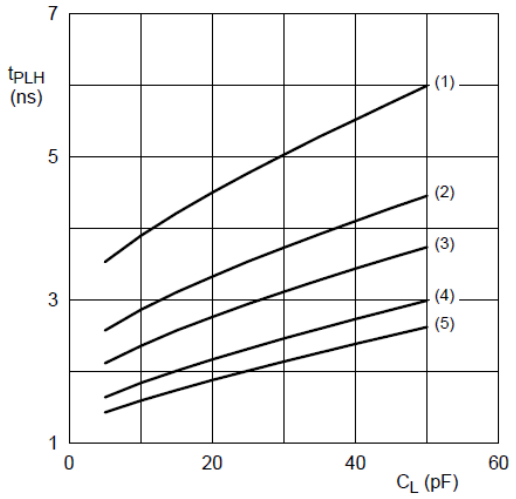
Figure 7. Typical propagation delay versus load capacitance; T_{amb}=25℃



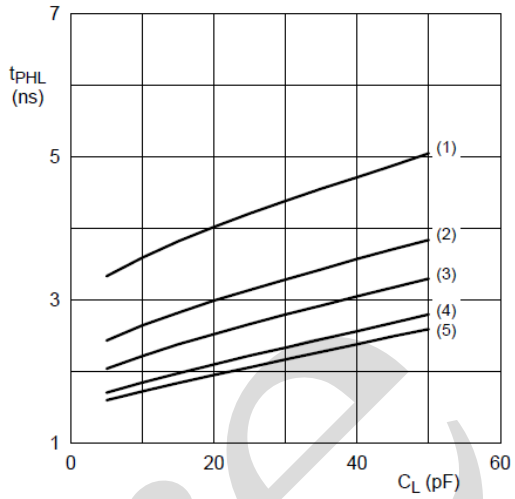
a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$=1.8V



b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$=1.8V



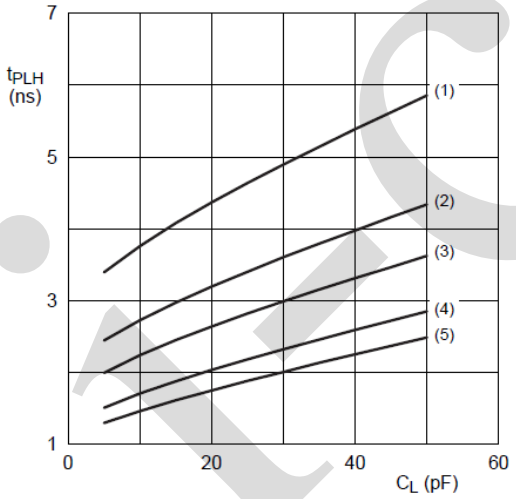
c. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$=2.5V



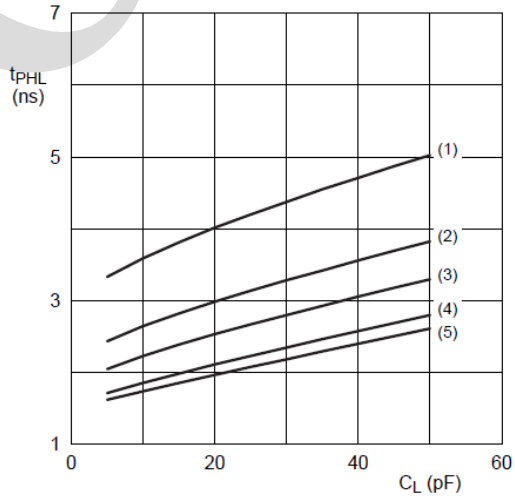
d. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$=2.5V

(1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.

Figure 8. Typical propagation delay versus load capacitance; T_{amb}=25℃



a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$=3.3V



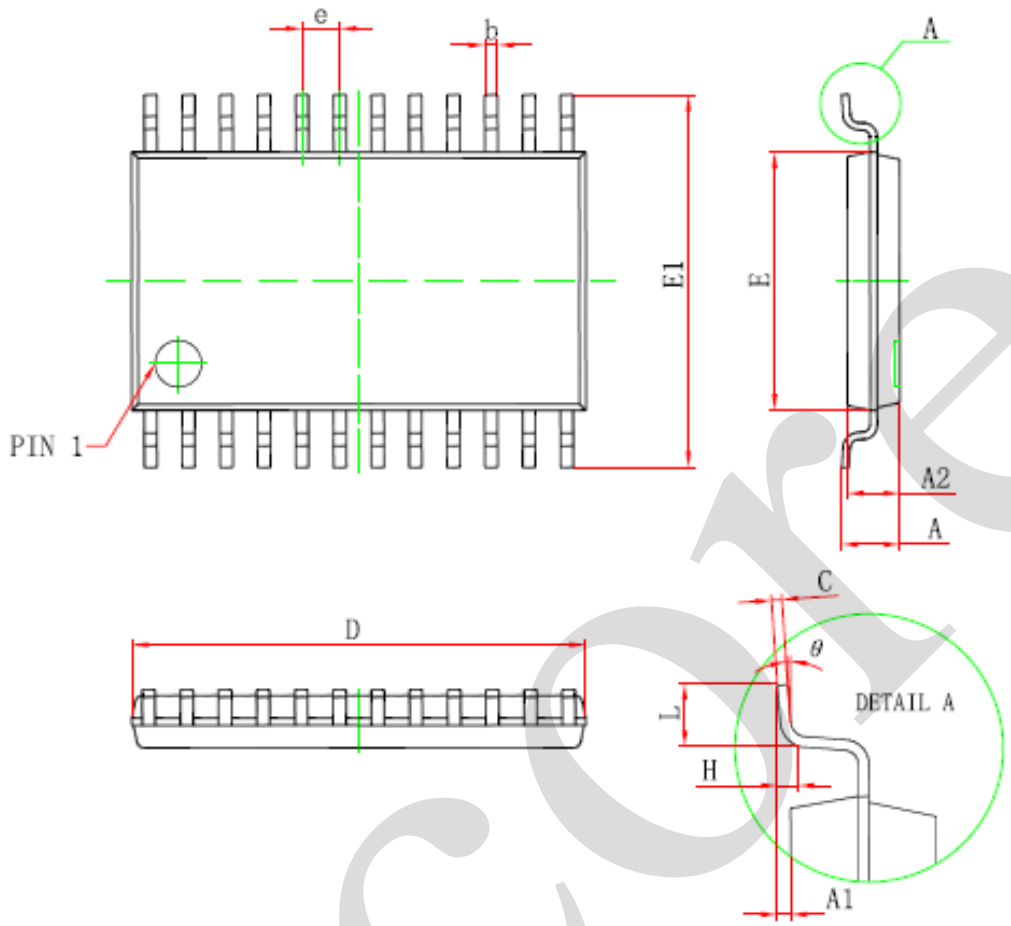
b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$=3.3V

(1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.

Figure 9. Typical propagation delay versus load capacitance; T_{amb}=25℃

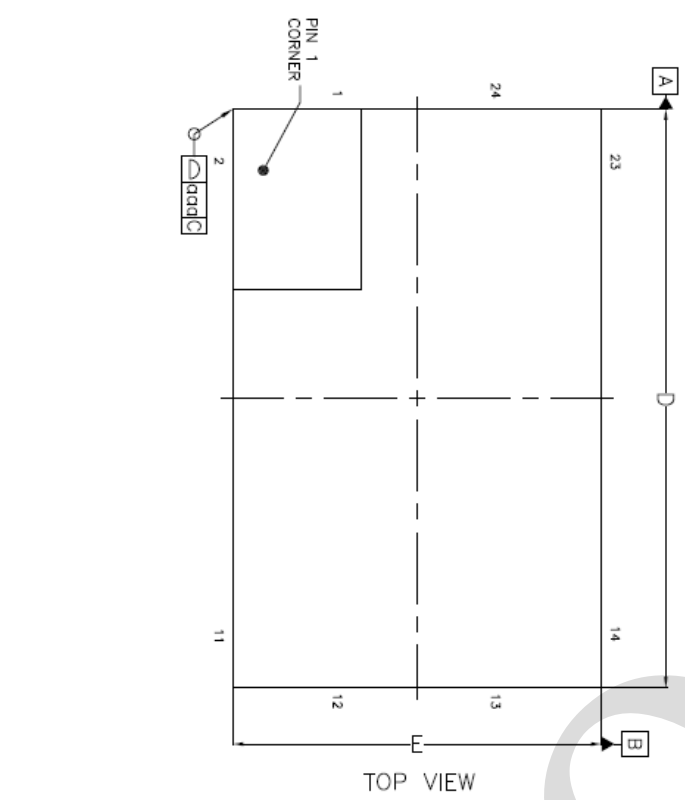
6、Package Information

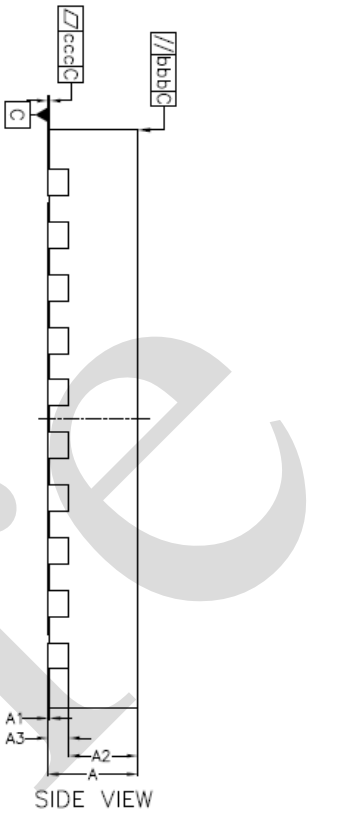
6.1、TSSOP24

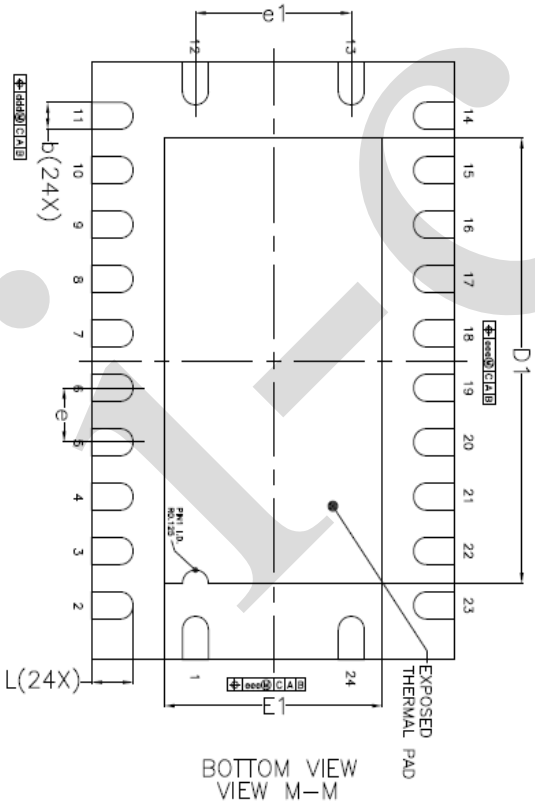


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65（BSC）		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

6.2、DHVQFN24







DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	1.00
STAND OFF		A1	0.00	0.02	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	5.40	5.50	5.60
	Y	E	3.40	3.50	3.60
LEAD PITCH		e	0.50 BSC		
		e1	1.50 BSC		
LEAD WIDTH		b	0.18	0.25	0.30
LEAD LENGTH		L	0.30	0.40	0.50
EP SIZE		D1	3.95	4.10	4.25
		E1	1.95	2.10	2.25
Tolerance of form and position					
aaa			0.1		
bbb			0.1		
ccc			0.05		
ddd			0.1		
eee			0.1		

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.