

**FH3210PS****N-Channel SGT Power MOSFET****◆ General Description**

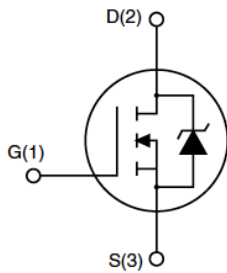
This N channel SGT MOSFET has been designed to very low on-state resistance and superior  $E_{AS}$  performance, especially for BMS and Motor driving applications.

**◆ Features**

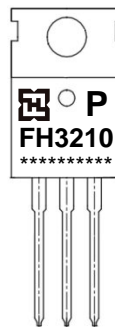
- $R_{DS(ON)} \leq 5.4m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**◆ Applications**

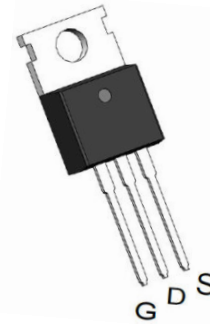
- Power Management
- DC/DC Converter
- Load Switch



Schematic diagram

**TO-220**

Marking and pin assignment



TO-220 top view

**Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

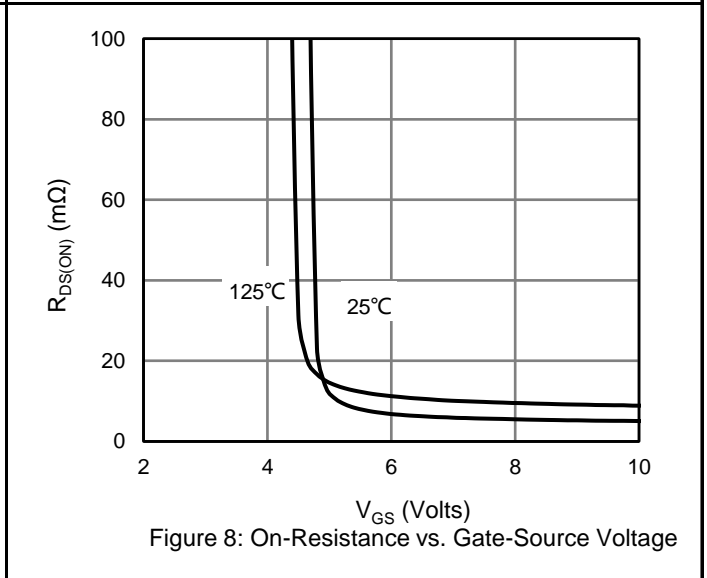
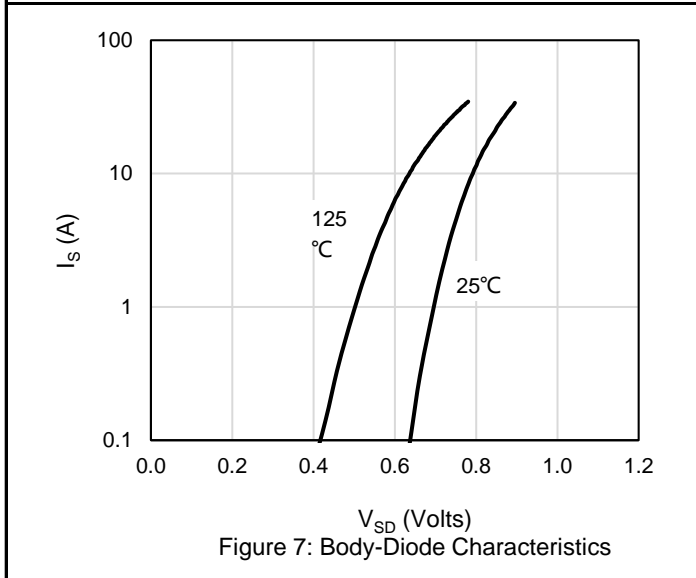
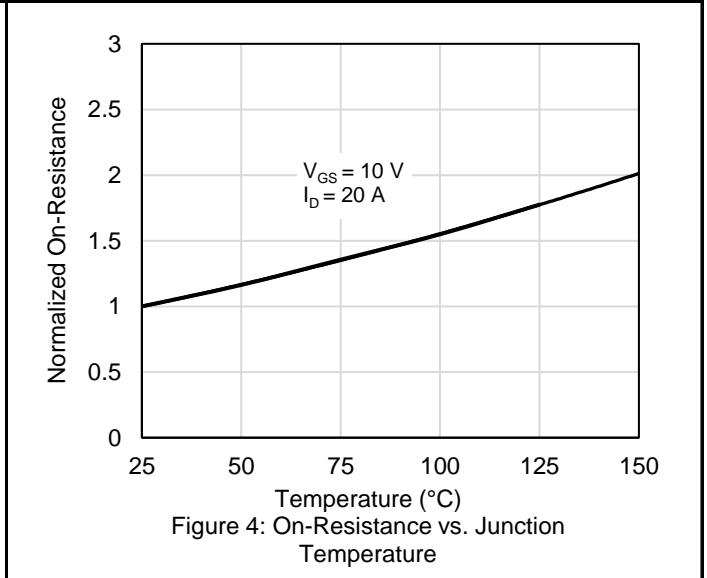
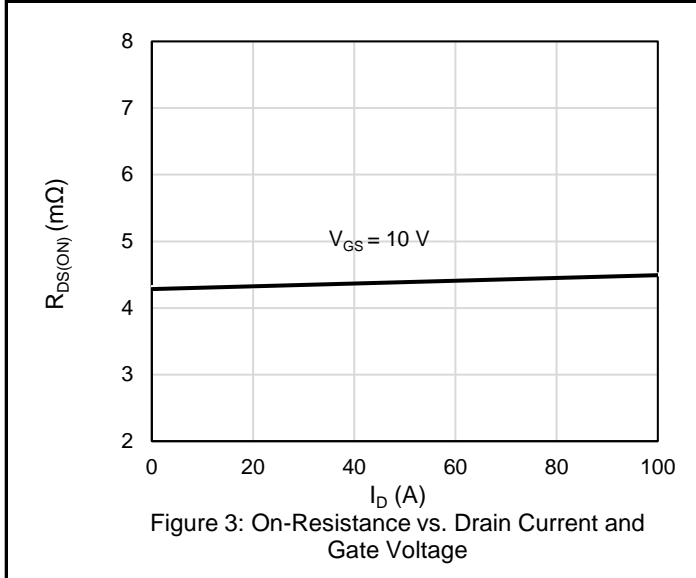
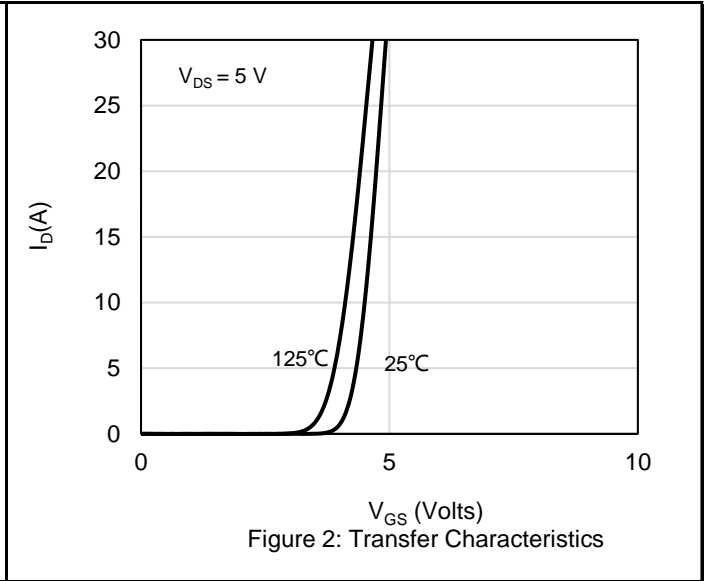
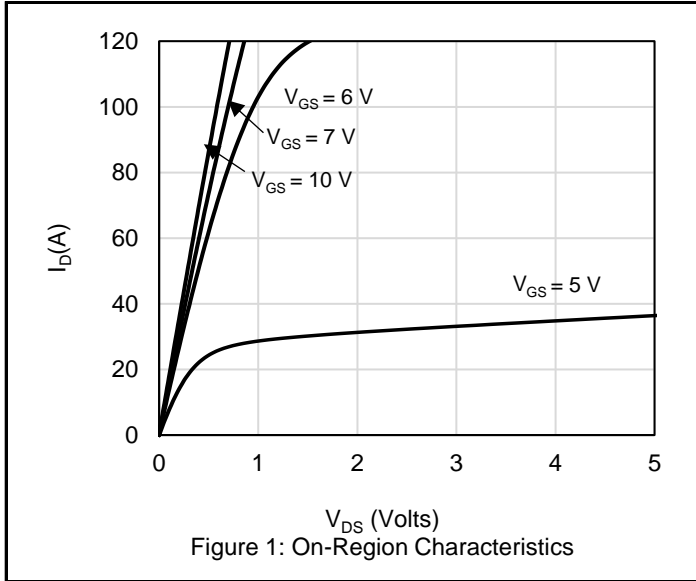
Symbol	Parameter	Value	Units
$V_{DS}$	Drain-Source Voltage	100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) <sup>(Note 1)</sup>	120	A
	Drain Current - Continuous ( $T_C = 100^\circ\text{C}$ )	84	A
$I_{DM}$	Drain Current - Pulsed <sup>(Note 2)</sup>	440	A
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(Note 3)</sup>	225	mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	192	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Steady-State	0.65	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Steady State <sup>(Note 4)</sup>	55	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V},$			1	$\mu\text{A}$
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(TH)}$	Gate Threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(ON)}$	Drain-Source on-state resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		4.5	5.4	m $\Omega$
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $F = 1\text{ MHz}$		3244		pF
$C_{OSS}$	Output Capacitance			1077		pF
$C_{RSS}$	Reverse Transfer Capacitance			52		pF
$R_G$	Gate Resistance	$F = 1\text{ MHz}$		3.5		$\Omega$
<b>Switching Characteristics</b>						
$T_{D(ON)}$	Turn On Delay Time	$V_{DD} = 50\text{ V}, R_L = 2.5\ \Omega,$ $V_{GS} = 10\text{ V}, R_G = 6\ \Omega$		22		nS
$T_R$	Rise Time			36		nS
$T_{D(OFF)}$	Turn Off Delay Time			49		nS
$T_F$	Fall Time			31.5		nS
$Q_G$	Total Gate Charge	$V_{DD} = 50\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$		51.3		nC
$Q_{GS}$	Gate-Source Charge			15.2		nC
$Q_{GD}$	Gate-Drain Charge			13.1		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Body-Diode Forward Current				120	A
$I_{SM}$	Maximum Pulsed Body-Diode Forward Current <sup>(NOTE 1)</sup>				440	A
$V_{SD}$	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$		0.7	1	V
$T_{RR}$	Reverse recovery time	$V_{DD} = 50\text{ V}, I_D = 15\text{ A},$ $di/dt = 100\text{ A}/\mu\text{S}$		58		ns
$Q_{RR}$	Reverse recovery charge			90.0		nC
$I_{RRM}$	Peak Reverse Recovery Current			2.6		A

**Notes:**

1. The max drain current rating is package limited
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3.  $L = 0.5\text{ mH}, V_{DD} = 50\text{ V}, I_{AS} = 30\text{ A}, R_G = 25\ \Omega,$  Starting  $T_J = 25^\circ\text{C}$
4. Mount on minimum PCB layout

Electrical Characteristics Diagrams



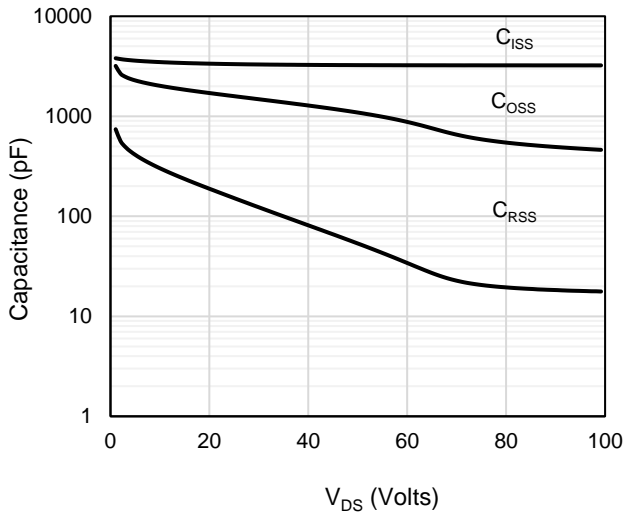


Figure 9: Capacitance Characteristics

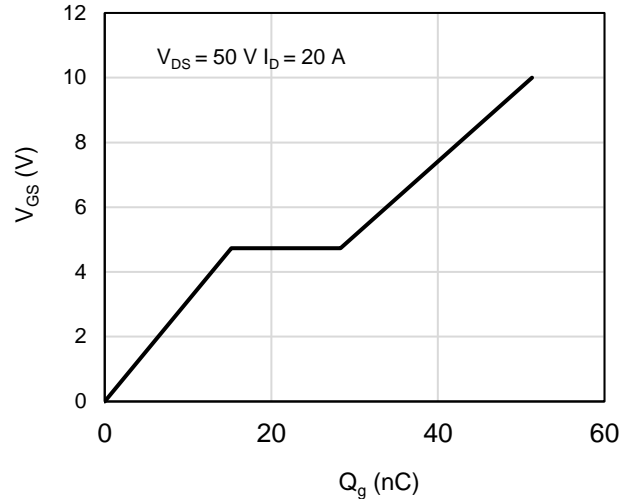


Figure 10: Gate-Charge Characteristics

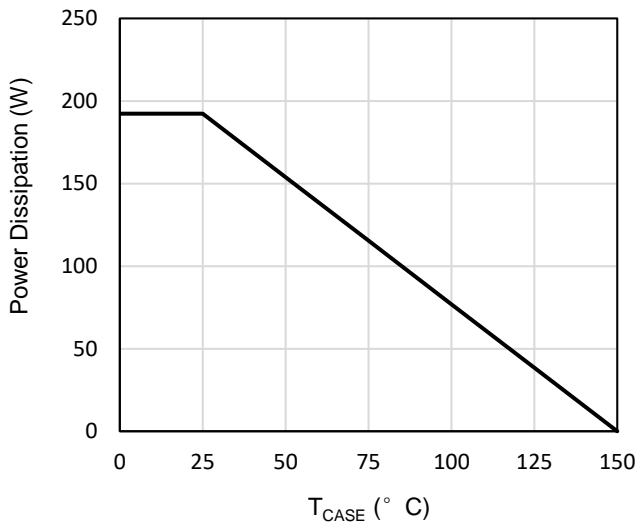


Figure 11: Power De-rating

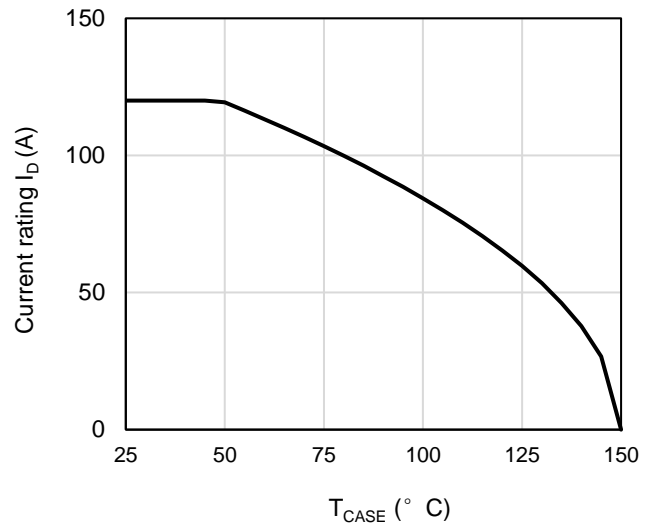


Figure 12: Current De-rating

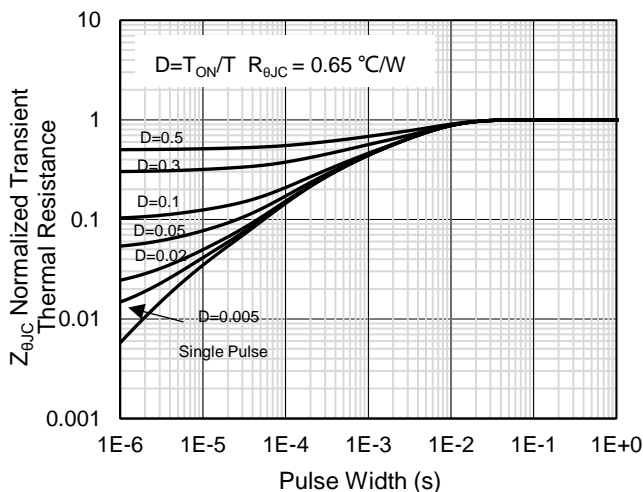


Figure 13: Normalized Maximum Transient Thermal Impedance

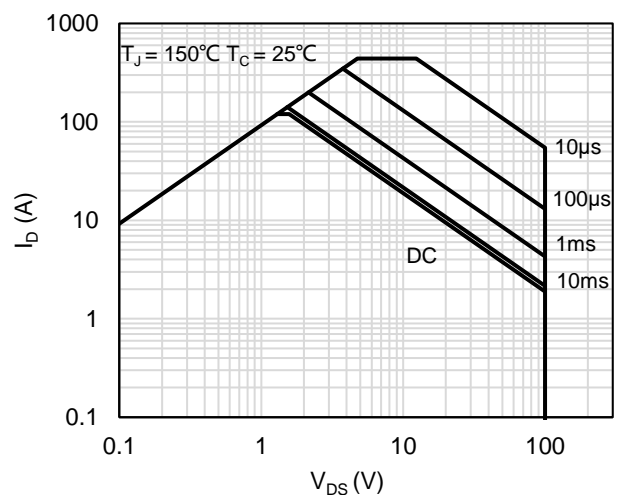
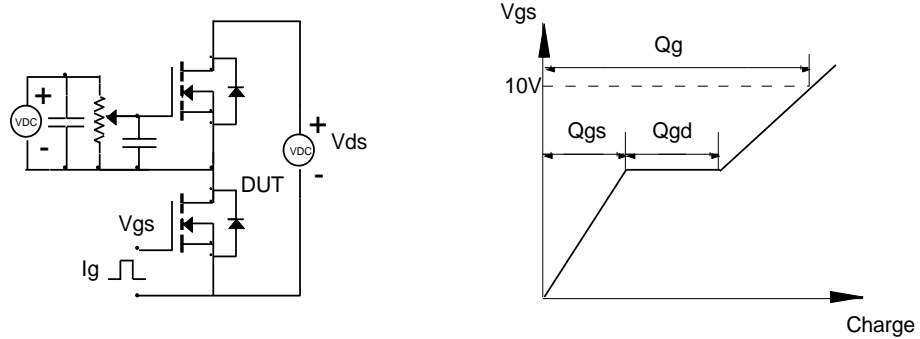


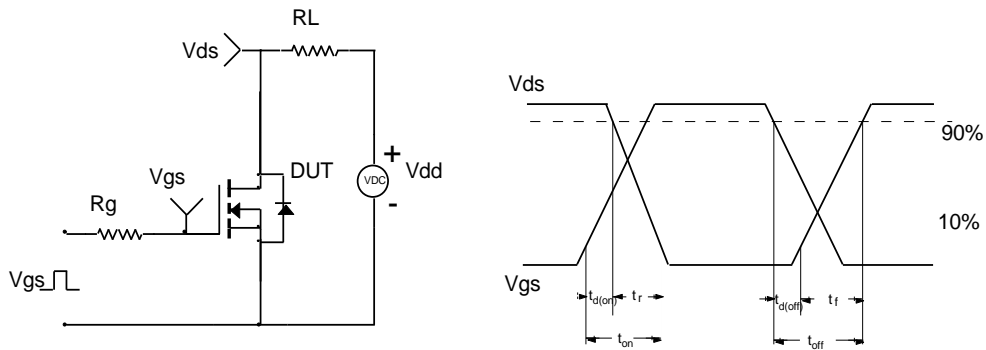
Figure 14: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

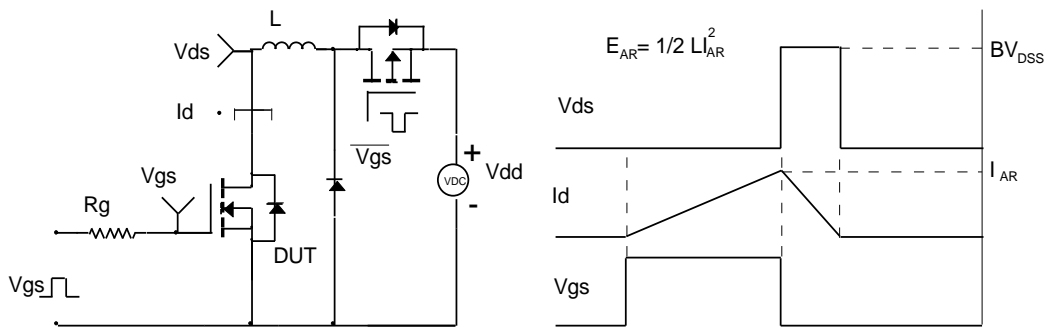
Gate Charge Test Circuit & Waveform



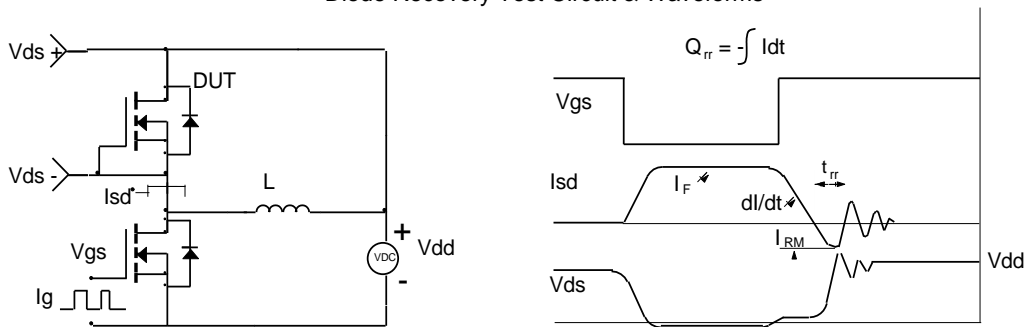
Resistive Switching Test Circuit & Waveforms



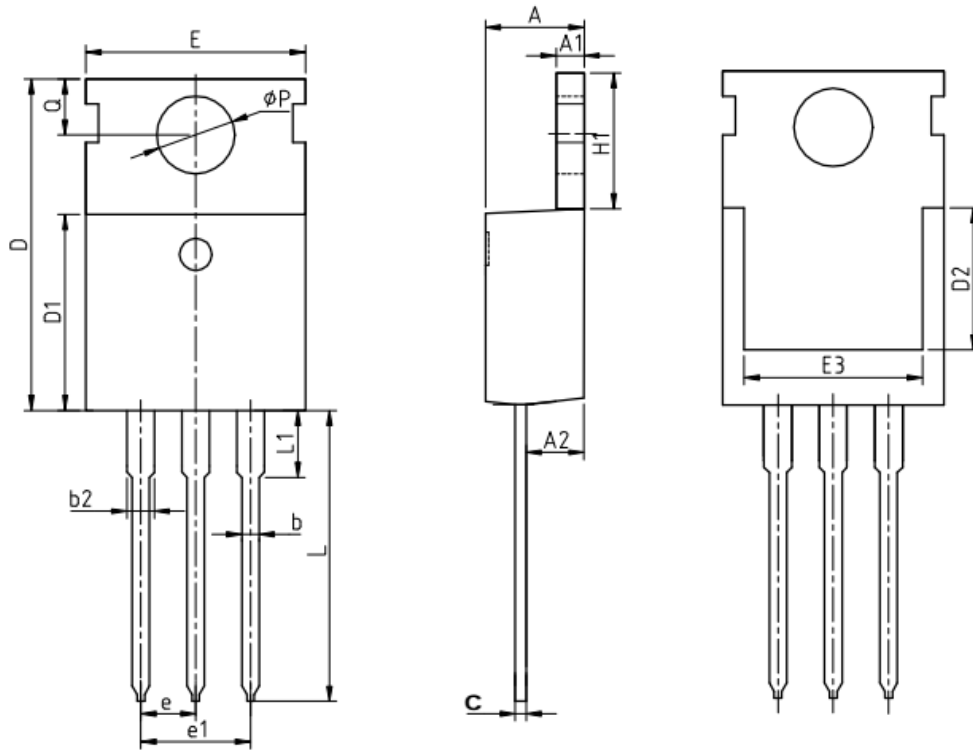
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Information : TO-220



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.15	1.30	1.45
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.40	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
φP	3.40	3.60	3.80
Q	2.60	2.80	3.00