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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY9BD10T Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The CY9BD10T Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and competitive cost.

These series are based on the Arm® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs, and Communication Interfaces (USB, CAN, UART, CSIO, I^2C, LIN, Ethernet-MAC).

The products which are described in this datasheet are placed into TYPE 2 product categories in "FM3 Family Peripheral Manual".

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p1
- Up to 144 MHz Frequency Operation
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Up to 1 MB
- Built-in Flash Accelerator System with 16 KB trace buffer memory
  The read access to Flash memory can be achieved without wait cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
- Security function for code protection

[SRAM]

This Series contain a total of up to 128 KB on-chip SRAM. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 64 KB
- SRAM1: Up to 64 KB

USB Interface (Max 2 channels)

USB interface is composed of Device and Host.
PLL for USB/Ethernet is built-in, USB clock or Ethernet clock can be generated by multiplication of Main clock.

[USB device]

- USB2.0 Full-Speed supported
- Max 6 EndPoint supported
  - EndPoint 0 is control transfer
  - EndPoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
  - EndPoint 3 to 5 can be selected Bulk-transfer or Interrupt-transfer
  - EndPoint 1 to 5 is comprised Double Buffers
    - Endpoint 0, 2 to 5: 64 bytes
    - Endpoint 1: 256 bytes

[USB host]

- USB2.0 Full/Low-speed supported
- Bulk-transfer, interrupt-transfer and Isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet-length supported
- Wake-up function supported

CAN Interface (Max 2 channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Ethernet - MAC (Max 2 channels)

- Compliant with IEEE802.3 specification
- 10 Mbps / 100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
  - MII: Max 1 channel
  - RMII: Max 2 channels
- Full-Duplex and Half-Duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 KB Transmit FIFO and 2 KB Receive FIFO.
- Compliant IEEE1588-2008 (PTP)

PLL for USB/Ethernet is built-in, USB clock or Ethernet clock can be generated by multiplication of Main clock.

Multi-function Serial Interface (Max 8 channels)

- 4 channels with 16 steps × 9-bit FIFO (ch.4 to ch.7), 4 channels without FIFO (ch.0 to ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13 to 16-bit length)
- LIN break delimiter generate (can be changed 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I^2C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

External Bus Interface

- Supports SRAM, NOR and NAND Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 MB
- Supports Address/Data multiplex
- Supports external RDY input

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 32 channels)

[12-bit A/D Converter]

- Successive Approximation Register type
- Built-in 3 unit
- Conversion time: 1.0 µs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

Base Timer (Max 16 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activation compare × 3ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from Low Power Consumption mode.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP mode.

General Purpose I/O Port

This series can use its pins as General Purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up 154 fast General Purpose I/O Ports @ 176 pin Package
- Some pin is 5 V tolerant I/O.
  See "Pin Description" to confirm the corresponding pins.

External Interrupt Controller Unit

- Up to 32 external interrupt input pin
- Include one non-maskable interrupt (NMI)

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Five clock sources (2 external oscillator, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 50 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low Power Mode

Three Low Power Consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply

Four Power Supplies

■ Wide range voltage:	VCC	= 2.7 V to 5.5 V
■ I/O voltage for USB ch.0:	USBVCC0	= 3.0 V to 3.6 V (when USB ch.0 is used) = 2.7 V to 5.5 V (when GPIO is used)
■ I/O voltage for USB ch.1:	USBVCC1	= 3.0 V to 3.6 V (when USB ch.1 is used) = 2.7 V to 5.5 V (when GPIO is used)
■ I/O voltage for Ethernet:	ETHVCC	= 3.0 V to 5.5 V (when Ethernet is used) = 2.7 V to 5.5 V (when GPIO is used)

Contents

1. Product Lineup

Memory Size

Product name	CY9BFD16S CY9BFD16T	CY9BFD17S CY9BFD17T	CY9BFD18S CY9BFD18T
On-chip Flash memory	512 KB	768 KB	1 MB
On-chip RAM	64 KB	96 KB	128 KB

Function

Product name			CY9BFD16S CY9BFD17S CY9BFD18S	CY9BFD16T CY9BFD17T CY9BFD18T
Pin count			144	176/192
CPU			Cortex-M3	
	Freq.		144 MHz	
Power supply voltage range			VCC: 2.7 V to 5.5 V (USBVCC0: 3.0 V to 3.6 V) (USBVCC1: 3.0 V to 3.6 V) (ETHVCC: 3.0 V to 5.5 V)	
USB2.0 (Device/Host)			2ch. (Max)	
CAN			2ch. (Max)	
Ethernet-MAC			2ch. (Max) MII: 1ch. / RMII: 2ch.(Max)	
DMAC			8ch.	
External Bus Interface			Addr: 19-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash	Addr: 25-bit (Max) R/Wdata :8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max) ch.4 to ch.7: FIFO (16 steps × 9-bit) ch.0 to ch.3: No FIFO	
Base Timer (PWC/ Reload timer/PWM/PPG)			16ch. (Max)	
MF-Timer	A/D activation compare	3ch.	3 units (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC			3ch. (Max)	
Dual Timer			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			32 pins (Max)+ NMI × 1	
I/O ports			122 pins (Max)	154 pins (Max)
12-bit A/D converter			24ch. (3 units)	32ch. (3 units)
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Internal CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

Package \ Product name	CY9BFD16S CY9BFD17S CY9BFD18S	CY9BFD16T CY9BFD17T CY9BFD18T
LQFP: LQS144 (0.5mm pitch)	❍	-
LQFP: LQP176 (0.5mm pitch)	-	❍
BGA: LBE192 (0.8mm pitch)	-	❍

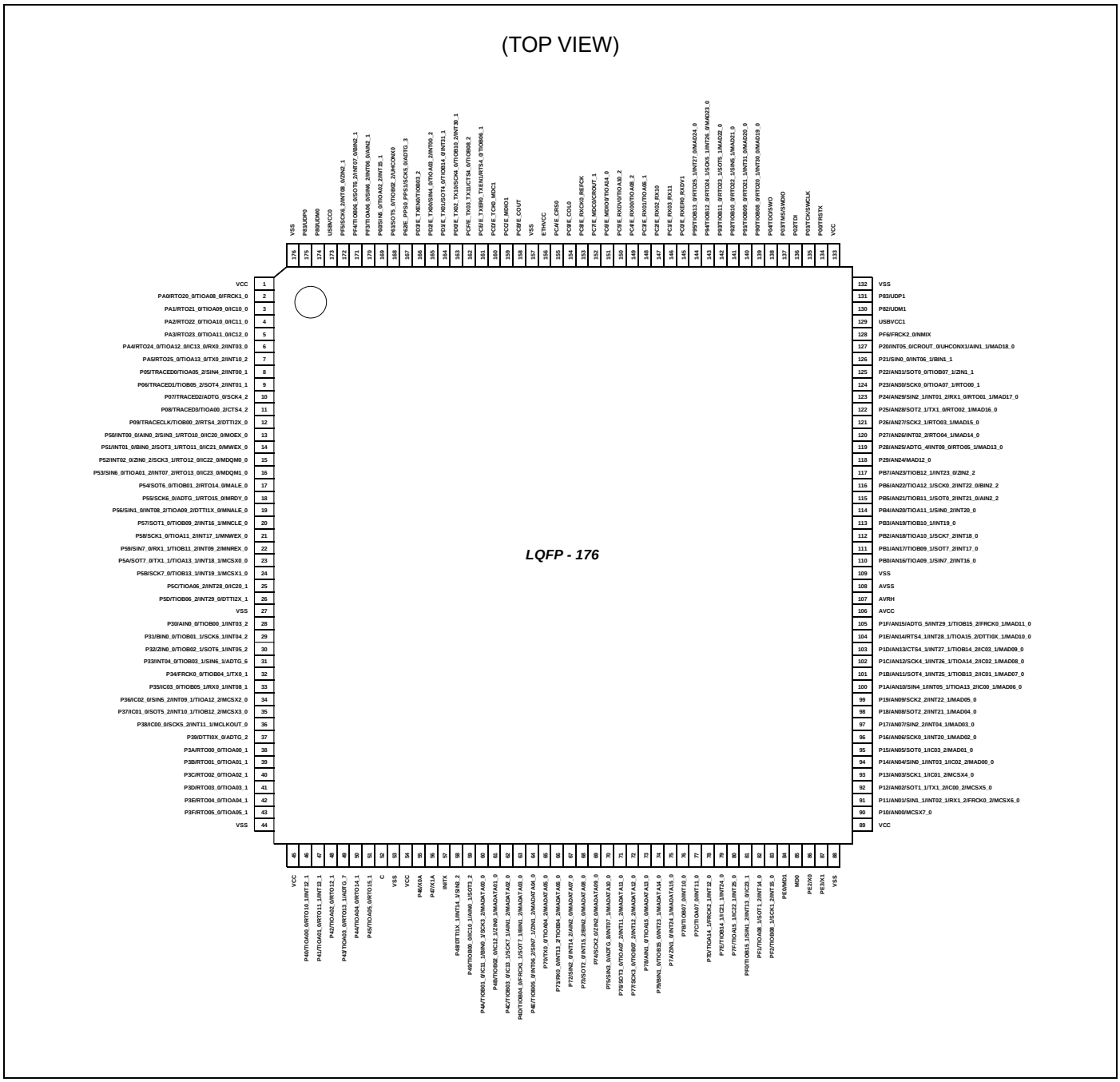
❍: Supported

Note:

- *See "14. Package Dimensions" for detailed information on each package.*

3. Pin Assignment

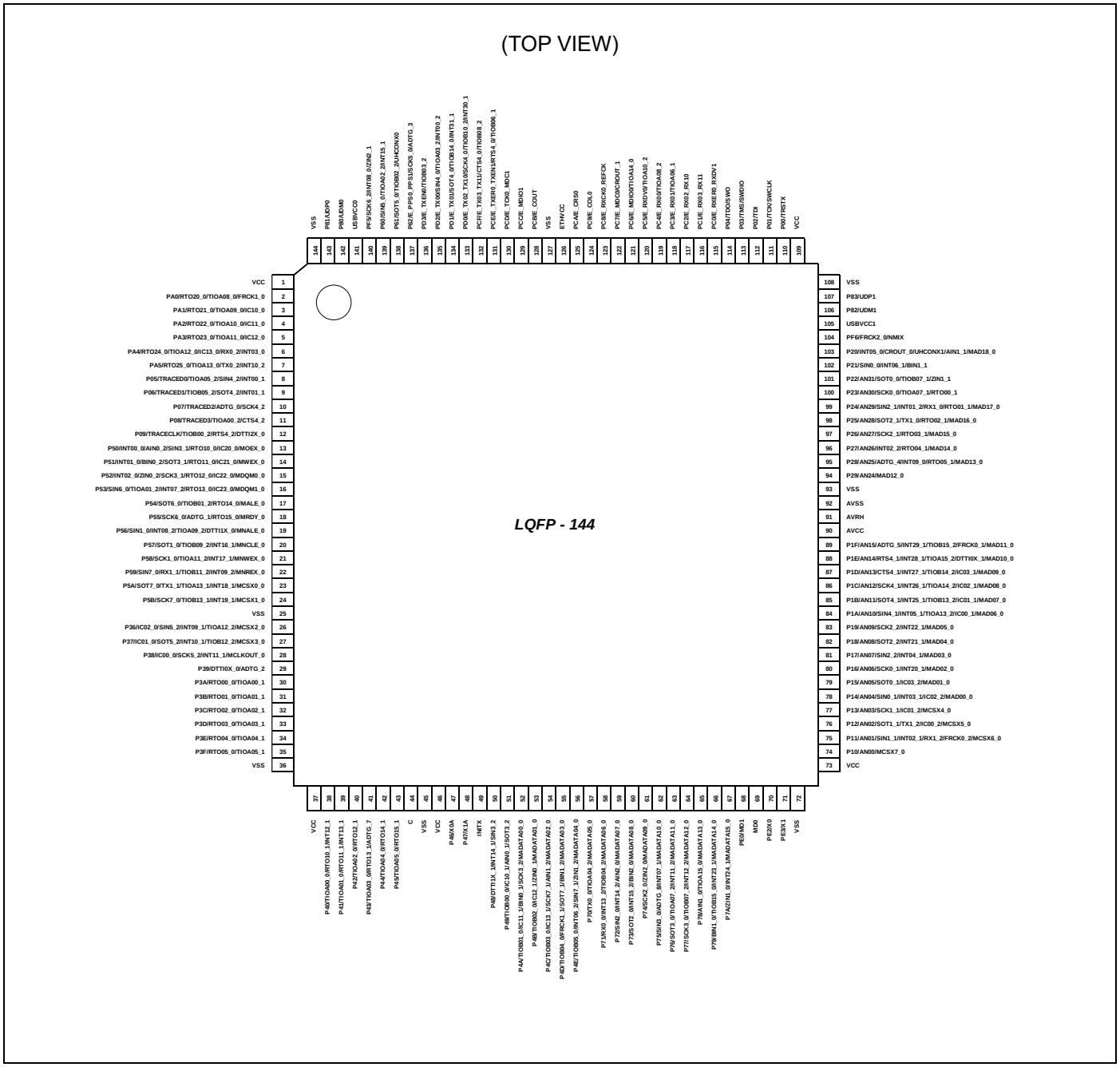
LQP176



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*
  TIOA09_0, TIOA09_1, and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "Base Timer" in "7. Handling Devices" for details.

LQS144



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR to select the pin.*
  TIOA09_0 and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "Base Timer" in "7. Handling Devices" for details.

LBE192

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		UDP0	UDM0	USB VCC0	VSS	PCD	PCB	VSS	ETH VCC	PC8	VSS	TCK	VCC	
B	VSS	PA0	PF5	PF3	P61	PD1	PCA	PC1	P95	P92	TDO	TMS	TRSTX	VSS
C	VCC	PA1	PA2	PF4	P60	PD2	PCC	PC5	PC0	P93	P90	TDI	PF6	UDP1
D	PA5	PA4	P05	P06	PA3	PD3	PCE	PC6	PC2	P94	P91	P21	P20	UDM1
E	VSS	P07	P08	P09	P50	P62	PCF	PC7	PC3	P25	P24	P23	P22	USB VCC1
F	P51	P52	P53	P54	P55	P56	PD0	PC9	PC4	P29	P28	P27	P26	VSS
G	VSS	P57	P58	P59	P5A	P5B	VSS	VSS	PB7	PB6	PB5	PB4	PB3	AVSS
H	P5C	P5D	P30	P31	P32	P33	VSS	VSS	P1F	P1E	PB2	PB1	PB0	AVRH
J	VSS	P37	P36	P35	P34	P70	VSS	P76	P1D	P1C	P1B	P1A	P19	AVCC
K	P38	P39	P3A	P3B	P4A	P4E	VSS	P74	P7B	P7F	P18	P16	P15	P17
L	P3C	P3D	P3E	P43	P49	P4D	VSS	P73	P7A	P7E	P14	P13	P12	VSS
M	VSS	P3F	P42	P44	P48	P4C	VSS	P72	P79	PF0	PF2	P11	P10	VCC
N	VCC	P40	P41	P45	INITX	P4B	VSS	P71	P78	P7D	PF1	MD0	MD1	VSS
P		C	VSS	VCC	X0A	X1A	VSS	P75	P77	P7C	VSS	X0	X1	

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*
  TIOA09_0, TIOA09_1, and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "Base Timer" in "7. Handling Devices" for details.

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
1	1	C1	VCC	-	
2	2	B2	PA0 RTO20_0 TIOA08_0 FRCK1_0	G	I
3	3	C2	PA1 RTO21_0 TIOA09_0 IC10_0	G	I
4	4	C3	PA2 RTO22_0 TIOA10_0 IC11_0	G	I
5	5	D5	PA3 RTO23_0 TIOA11_0 IC12_0	G	I
6	6	D2	PA4 RTO24_0 TIOA12_0 RX0_2 IC13_0 INT03_0	G	H
7	7	D1	PA5 RTO25_0 TX0_2 TIOA13_0 INT10_2	G	H
8	8	D3	P05 TRACED0 TIOA05_2 SIN4_2 INT00_1	E	F
9	9	D4	P06 TRACED1 TIOB05_2 SOT4_2 INT01_1	E	F

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
10	10	E2	P07	E	G
			TRACED2		
			ADTG_0		
			SCK4_2		
11	11	E3	P08	E	G
			TRACED3		
			TIOA00_2		
			CTS4_2		
12	12	E4	P09	E	G
			TRACECLK		
			TIOB00_2		
			RTS4_2		
			DTTI2X_0		
13	13	E5	P50	E	H
			INT00_0		
			AIN0_2		
			SIN3_1		
			RTO10_0		
			IC20_0		
			MOEX_0		
14	14	F1	P51	E	H
			INT01_0		
			BIN0_2		
			SOT3_1		
			RTO11_0		
			IC21_0		
			MWEX_0		
15	15	F2	P52	E	H
			INT02_0		
			ZIN0_2		
			SCK3_1		
			RTO12_0		
			IC22_0		
			MDQM0_0		
16	16	F3	P53	E	H
			SIN6_0		
			TIOA01_2		
			INT07_2		
			RTO13_0		
			IC23_0		
			MDQM1_0		

Pin No			Pin Name	I/O circuit type	Pin State type
LQFP-176	LQFP-144	BGA-192			
17	17	F4	P54 SOT6_0 TIOB01_2 RTO14_0 MALE_0	E	I
18	18	F5	P55 SCK6_0 ADTG_1 RTO15_0 MRDY_0	E	I
19	19	F6	P56 SIN1_0 INT08_2 TIOA09_2 DTTI1X_0 MNALE_0	E	H
20	20	G2	P57 SOT1_0 TIOB09_2 INT16_1 MNCLE_0	E	H
21	21	G3	P58 SCK1_0 TIOA11_2 INT17_1 MNWEX_0	E	H
22	22	G4	P59 SIN7_0 RX1_1 TIOB11_2 INT09_2 MNREX_0	E	H
23	23	G5	P5A SOT7_0 TX1_1 TIOA13_1 INT18_1 MCSX0_0	E	H
24	24	G6	P5B SCK7_0 TIOB13_1 INT19_1 MCSX1_0	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
25	-	H1	P5C TIOA06_2 INT28_0 IC20_1	E	H
26	-	H2	P5D TIOB06_2 INT29_0 DTTI2X_1	E	H
27	25	J1	VSS	-	
28	-	H3	P30 AIN0_0 TIOB00_1 INT03_2	E	H
29	-	H4	P31 BIN0_0 TIOB01_1 SCK6_1 INT04_2	E	H
30	-	H5	P32 ZIN0_0 TIOB02_1 SOT6_1 INT05_2	E	H
31	-	H6	P33 INT04_0 TIOB03_1 SIN6_1 ADTG_6	E	H
32	-	J5	P34 FRCK0_0 TX0_1 TIOB04_1	E	I
33	-	J4	P35 IC03_0 RX0_1 TIOB05_1 INT08_1	E	H
34	26	J3	P36 IC02_0 SIN5_2 INT09_1 TIOA12_2 MCSX2_0	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
35	27	J2	P37 IC01_0 SOT5_2 INT10_1 TIOB12_2 MCSX3_0	E	H
36	28	K1	P38 IC00_0 SCK5_2 INT11_1 MCLKOUT_0	E	H
37	29	K2	P39 DTTI0X_0 ADTG_2	E	I
38	30	K3	P3A RTO00_0 TIOA00_1	G	I
39	31	K4	P3B RTO01_0 TIOA01_1	G	I
40	32	L1	P3C RTO02_0 TIOA02_1	G	I
41	33	L2	P3D RTO03_0 TIOA03_1	G	I
42	34	L3	P3E RTO04_0 TIOA04_1	G	I
43	35	M2	P3F RTO05_0 TIOA05_1	G	I
44	36	M1	VSS	-	
45	37	N1	VCC	-	
46	38	N2	P40 TIOA00_0 RTO10_1 INT12_1	G	H
47	39	N3	P41 TIOA01_0 RTO11_1 INT13_1	G	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
48	40	M3	P42	G	I
			TIOA02_0		
			RTO12_1		
49	41	L4	P43	G	I
			TIOA03_0		
			RTO13_1		
			ADTG_7		
50	42	M4	P44	G	I
			TIOA04_0		
			RTO14_1		
51	43	N4	P45	G	I
			TIOA05_0		
			RTO15_1		
52	44	P2	C	-	
53	45	P3	VSS	-	
54	46	P4	VCC	-	
55	47	P5	P46	D	M
			X0A		
56	48	P6	P47	D	N
			X1A		
57	49	N5	INITX	B	C
58	50	M5	P48	E	H
			DTTI1X_1		
			INT14_1		
			SIN3_2		
59	51	L5	P49	E	I
			TIOB00_0		
			IC10_1		
			AIN0_1		
			SOT3_2		
60	52	K5	P4A	E	I
			TIOB01_0		
			IC11_1		
			BIN0_1		
			SCK3_2		
			MADATA00_0		
61	53	N6	P4B	E	I
			TIOB02_0		
			IC12_1		
			ZIN0_1		
			MADATA01_0		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
62	54	M6	P4C	E	I
			TIOB03_0		
			IC13_1		
			SCK7_1		
			AIN1_2		
			MADATA02_0		
63	55	L6	P4D	E	I
			TIOB04_0		
			FRCK1_1		
			SOT7_1		
			BIN1_2		
			MADATA03_0		
64	56	K6	P4E	E	H
			TIOB05_0		
			INT06_2		
			SIN7_1		
			ZIN1_2		
			MADATA04_0		
65	57	J6	P70	E	I
			TIOA04_2		
			TX0_0		
			MADATA05_0		
66	58	N8	P71	E	H
			INT13_2		
			TIOB04_2		
			RX0_0		
			MADATA06_0		
67	59	M8	P72	E	H
			SIN2_0		
			INT14_2		
			AIN2_0		
			MADATA07_0		
68	60	L8	P73	E	H
			SOT2_0		
			INT15_2		
			BIN2_0		
			MADATA08_0		
69	61	K8	P74	E	I
			SCK2_0		
			ZIN2_0		
			MADATA09_0		
70	62	P8	P75	E	H
			SIN3_0		
			ADTG_8		
			INT07_1		
			MADATA10_0		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
71	63	J8	P76 SOT3_0 TIOA07_2 INT11_2 MADATA11_0	E	H
72	64	P9	P77 SCK3_0 TIOB07_2 INT12_2 MADATA12_0	E	H
73	65	N9	P78 AIN1_0 TIOA15_0 MADATA13_0	E	I
74	66	M9	P79 BIN1_0 TIOB15_0 INT23_1 MADATA14_0	E	H
-	-	E1	VSS	-	
-	-	G1	VSS	-	
75	67	L9	P7A ZIN1_0 INT24_1 MADATA15_0	E	H
76	-	K9	P7B TIOB07_0 INT10_0	E	H
77	-	P10	P7C TIOA07_0 INT11_0	E	H
78	-	N10	P7D TIOA14_1 FRCK2_1 INT12_0	E	H
79	-	L10	P7E TIOB14_1 IC21_1 INT24_0	E	H
80	-	K10	P7F TIOA15_1 IC22_1 INT25_0	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
81	-	M10	PF0	I[1]	H
			TIOB15_1		
			SIN1_2		
			INT13_0		
			IC23_1		
82	-	N11	PF1	I[1]	H
			TIOA08_1		
			SOT1_2		
			INT14_0		
83	-	M11	PF2	I[1]	H
			TIOB08_1		
			SCK1_2		
			INT15_0		
84	68	N13	PE0	C	P
			MD1		
85	69	N12	MD0	J	D
86	70	P12	PE2	A	A
			X0		
87	71	P13	PE3	A	B
			X1		
88	72	N14	VSS	-	
89	73	M14	VCC	-	
-	-	L7	VSS	-	
-	-	K7	VSS	-	
90	74	M13	P10	F	K
			AN00		
			MCSX7_0		
91	75	M12	P11	F	L
			AN01		
			SIN1_1		
			RX1_2		
			INT02_1		
			FRCK0_2		
			MCSX6_0		
92	76	L13	P12	F	K
			AN02		
			SOT1_1		
			TX1_2		
			IC00_2		
			MCSX5_0		
93	77	L12	P13	F	K
			AN03		
			SCK1_1		
			IC01_2		
			MCSX4_0		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
94	78	L11	P14 AN04 SIN0_1 INT03_1 IC02_2 MAD00_0	F	L
95	79	K13	P15 AN05 SOT0_1 IC03_2 MAD01_0	F	K
96	80	K12	P16 AN06 SCK0_1 INT20_1 MAD02_0	F	L
97	81	K14	P17 AN07 SIN2_2 INT04_1 MAD03_0	F	L
-	-	P7	VSS	-	
-	-	P11	VSS	-	
-	-	L14	VSS	-	
98	82	K11	P18 AN08 SOT2_2 INT21_1 MAD04_0	F	L
99	83	J13	P19 AN09 SCK2_2 INT22_1 MAD05_0	F	L
100	84	J12	P1A AN10 SIN4_1 INT05_1 TIOA13_2 IC00_1 MAD06_0	F	L

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
101	85	J11	P1B AN11 SOT4_1 INT25_1 TIOB13_2 IC01_1 MAD07_0	F	L
102	86	J10	P1C AN12 SCK4_1 INT26_1 TIOA14_2 IC02_1 MAD08_0	F	L
103	87	J9	P1D AN13 CTS4_1 INT27_1 TIOB14_2 IC03_1 MAD09_0	F	L
104	88	H10	P1E AN14 RTS4_1 INT28_1 TIOA15_2 DTTI0X_1 MAD10_0	F	L
105	89	H9	P1F AN15 ADTG_5 INT29_1 TIOB15_2 FRCK0_1 MAD11_0	F	L
106	90	J14	AVCC	-	
107	91	H14	AVRH	-	
108	92	G14	AVSS	-	
109	93	F14	VSS	-	
110	-	H13	PB0 AN16 TIOA09_1 SIN7_2 INT16_0	F	L

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
111	-	H12	PB1	F	L
			AN17		
			TIOB09_1		
			SOT7_2		
			INT17_0		
112	-	H11	PB2	F	L
			AN18		
			TIOA10_1		
			SCK7_2		
			INT18_0		
113	-	G13	PB3	F	L
			AN19		
			TIOB10_1		
			INT19_0		
114	-	G12	PB4	F	L
			AN20		
			TIOA11_1		
			SIN0_2		
			INT20_0		
115	-	G11	PB5	F	L
			AN21		
			TIOB11_1		
			SOT0_2		
			INT21_0		
			AIN2_2		
-	-	G7	VSS	-	
-	-	J7	VSS	-	
116	-	G10	PB6	F	L
			AN22		
			TIOA12_1		
			SCK0_2		
			INT22_0		
			BIN2_2		
117	-	G9	PB7	F	L
			AN23		
			TIOB12_1		
			INT23_0		
			ZIN2_2		
118	94	F10	P29	F	K
			AN24		
			MAD12_0		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
119	95	F11	P28 AN25 ADTG_4 INT09_0 RTO05_1 MAD13_0	F	L
120	96	F12	P27 AN26 INT02_2 RTO04_1 MAD14_0	F	L
121	97	F13	P26 AN27 SCK2_1 RTO03_1 MAD15_0	F	K
122	98	E10	P25 AN28 SOT2_1 TX1_0 RTO02_1 MAD16_0	F	K
123	99	E11	P24 AN29 SIN2_1 RX1_0 INT01_2 RTO01_1 MAD17_0	F	L
124	100	E12	P23 AN30 SCK0_0 TIOA07_1 RTO00_1	F	K
125	101	E13	P22 AN31 SOT0_0 TIOB07_1 ZIN1_1	F	K
126	102	D12	P21 SIN0_0 INT06_1 BIN1_1	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
124	100	E12	P23	F	K
			AN30		
			SCK0_0		
			TIOA07_1		
			RTO00_1		
125	101	E13	P22	F	K
			AN31		
			SOT0_0		
			TIOB07_1		
			ZIN1_1		
126	102	D12	P21	E	H
			SIN0_0		
			INT06_1		
			BIN1_1		
127	103	D13	P20	E	H
			INT05_0		
			CROUT_0		
			UHCONX1		
			AIN1_1		
			MAD18_0		
128	104	C13	PF6	I[1]	J
			FRCK2_0		
			NMIX		
129	105	E14	USBVCC1	-	
130	106	D14	P82	H	O
			UDM1		
131	107	C14	P83	H	O
			UDP1		
132	108	B14	VSS	-	
133	109	A13	VCC	-	
134	110	B13	P00	E	E
			TRSTX		
135	111	A12	P01	E	E
			TCK		
			SWCLK		
136	112	C12	P02	E	E
			TDI		
137	113	B12	P03	E	E
			TMS		
			SWDIO		
138	114	B11	P04	E	E
			TDO		
			SWO		
139	-	C11	P90	E	H
			TIOB08_0		
			RTO20_1		
			INT30_0		
			MAD19_0		
-	-	A8	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
140	-	D11	P91 TIOB09_0 RTO21_1 INT31_0 MAD20_0	E	H
141	-	B10	P92 TIOB10_0 RTO22_1 SIN5_1 MAD21_0	E	I
142	-	C10	P93 TIOB11_0 RTO23_1 SOT5_1 MAD22_0	E	I
143	-	D10	P94 TIOB12_0 RTO24_1 SCK5_1 INT26_0 MAD23_0	E	H
144	-	B9	P95 TIOB13_0 RTO25_1 INT27_0 MAD24_0	E	H
145	115	C9	PC0 E_RXER0_RXDV1	K	Q
146	116	B8	PC1 E_RX03_RX11	K	Q
147	117	D9	PC2 E_RX02_RX10	K	Q
148	118	E9	PC3 E_RX01 TIOA06_1	K	Q
149	119	F9	PC4 E_RX00 TIOA08_2	K	Q
150	120	C8	PC5 E_RXDV0 TIOA10_2	K	Q
-	-	A5	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
151	121	D8	PC6	K	Q
			E_MDIO0		
			TIOA14_0		
152	122	E8	PC7	L	Q
			E_MDC0		
			CROUT_1		
153	123	A10	PC8	K	Q
			E_RXCK0_REFCK		
154	124	F8	PC9	K	Q
			E_COL0		
155	125	B7	PCA	K	Q
			E_CRS0		
156	126	A9	ETHVCC	-	
157	127	A11	VSS	-	
158	128	A7	PCB	L	Q
			E_COUT		
159	129	C7	PCC	K	Q
			E_MDIO1		
160	130	A6	PCD	K	Q
			E_TCK0_MDC1		
161	131	D7	PCE	L	Q
			E_TXER0_TXEN1		
			RTS4_0		
			TIOB06_1		
162	132	E7	PCF	L	Q
			E_TX03_TX11		
			CTS4_0		
			TIOB08_2		
163	133	F7	PD0	L	R
			E_TX02_TX10		
			SCK4_0		
			TIOB10_2		
			INT30_1		
164	134	B6	PD1	L	R
			E_TX01		
			SOT4_0		
			TIOB14_0		
			INT31_1		
-	-	N7	VSS	-	
-	-	G8	VSS	-	
-	-	H7	VSS	-	
-	-	H8	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
165	135	C6	PD2 E_TX00 SIN4_0 TIOA03_2 INT00_2	L	R
166	136	D6	PD3 E_TXEN0 TIOB03_2	L	Q
167	137	E6	P62 E_PPS0_PPS1 SCK5_0 ADTG_3	E	Q
168	138	B5	P61 SOT5_0 TIOB02_2 UHCONX0	E	I
169	139	C5	P60 SIN5_0 TIOA02_2 INT15_1	E	H
170	-	B4	PF3 TIOA06_0 SIN6_2 INT06_0 AIN2_1	I[1]	H
171	-	C4	PF4 TIOB06_0 SOT6_2 INT07_0 BIN2_1	I[1]	H
172	140	B3	PF5 SCK6_2 INT08_0 ZIN2_1	I[1]	H
173	141	A4	USBVCC0	-	
174	142	A3	P80 UDM0	H	O
175	143	A2	P81 UDP0	H	O
176	144	B1	VSS	-	
-	-	M7	VSS	-	

*1: 5 V tolerant I/O

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
ADC	ADTG_0	A/D converter external trigger input pin	10	10	E2
	ADTG_1		18	18	F5
	ADTG_2		37	29	K2
	ADTG_3		167	137	E6
	ADTG_4		119	95	F11
	ADTG_5		105	89	H9
	ADTG_6		31	-	H6
	ADTG_7		49	41	L4
	ADTG_8		70	62	P8
	AN00	A/D converter analog input pin (ANxx describes ADC ch.xx)	90	74	M13
	AN01		91	75	M12
	AN02		92	76	L13
	AN03		93	77	L12
	AN04		94	78	L11
	AN05		95	79	K13
	AN06		96	80	K12
	AN07		97	81	K14
	AN08		98	82	K11
	AN09		99	83	J13
	AN10		100	84	J12
	AN11		101	85	J11
	AN12		102	86	J10
	AN13		103	87	J9
	AN14		104	88	H10
	AN15		105	89	H9
	AN16		110	-	H13
	AN17		111	-	H12
	AN18		112	-	H11
	AN19		113	-	G13
	AN20		114	-	G12
	AN21		115	-	G11
	AN22		116	-	G10
	AN23		117	-	G9
	AN24		118	94	F10
	AN25		119	95	F11
	AN26		120	96	F12
	AN27		121	97	F13
	AN28		122	98	E10
	AN29		123	99	E11
	AN30		124	100	E12
	AN31		125	101	E13

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	46	38	N2
	TIOA0_1		38	30	K3
	TIOA0_2		11	11	E3
	TIOB0_0	Base timer ch.0 TIOB pin	59	51	L5
	TIOB0_1		28	-	H3
	TIOB0_2		12	12	E4
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	47	39	N3
	TIOA1_1		39	31	K4
	TIOA1_2		16	16	F3
	TIOB1_0	Base timer ch.1 TIOB pin	60	52	K5
	TIOB1_1		29	-	H4
	TIOB1_2		17	17	F4
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	48	40	M3
	TIOA2_1		40	32	L1
	TIOA2_2		169	139	C5
	TIOB2_0	Base timer ch.2 TIOB pin	61	53	N6
	TIOB2_1		30	-	H5
	TIOB2_2		168	138	B5
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	49	41	L4
	TIOA3_1		41	33	L2
	TIOA3_2		165	135	C6
	TIOB3_0	Base timer ch.3 TIOB pin	62	54	M6
	TIOB3_1		31	-	H6
	TIOB3_2		166	136	D6
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	50	42	M4
	TIOA4_1		42	34	L3
	TIOA4_2		65	57	J6
	TIOB4_0	Base timer ch.4 TIOB pin	63	55	L6
	TIOB4_1		32	-	J5
	TIOB4_2		66	58	N8
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	51	43	N4
	TIOA5_1		43	35	M2
	TIOA5_2		8	8	D3
	TIOB5_0	Base timer ch.5 TIOB pin	64	56	K6
	TIOB5_1		33	-	J4
	TIOB5_2		9	9	D4
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	170	-	B4
	TIOA6_1		148	118	E9
	TIOA6_2		25	-	H1
	TIOB6_0	Base timer ch.6 TIOB pin	171	-	C4
	TIOB6_1		161	131	D7
	TIOB6_2		26	-	H2

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 7	TIOA07_0	Base timer ch.7 TIOA pin	77	-	P10
	TIOA07_1		124	100	E12
	TIOA07_2		71	63	J8
	TIOB07_0	Base timer ch.7 TIOB pin	76	-	K9
	TIOB07_1		125	101	E13
	TIOB07_2		72	64	P9
Base Timer 8	TIOA08_0	Base timer ch.8 TIOA pin	2	2	B2
	TIOA08_1		82	-	N11
	TIOA08_2		149	119	F9
	TIOB08_0	Base timer ch.8 TIOB pin	139	-	C11
	TIOB08_1		83	-	M11
	TIOB08_2		162	132	E7
Base Timer 9	TIOA09_0	Base timer ch.9 TIOA pin	3	3	C2
	TIOA09_1		110	-	H13
	TIOA09_2		19	19	F6
	TIOB09_0	Base timer ch.9 TIOB pin	140	-	D11
	TIOB09_1		111	-	H12
	TIOB09_2		20	20	G2
Base Timer 10	TIOA10_0	Base timer ch.10 TIOA pin	4	4	C3
	TIOA10_1		112	-	H11
	TIOA10_2		150	120	C8
	TIOB10_0	Base timer ch.10 TIOB pin	141	-	B10
	TIOB10_1		113	-	G13
	TIOB10_2		163	133	F7
Base Timer 11	TIOA11_0	Base timer ch.11 TIOA pin	5	5	D5
	TIOA11_1		114	-	G12
	TIOA11_2		21	21	G3
	TIOB11_0	Base timer ch.11 TIOB pin	142	-	C10
	TIOB11_1		115	-	G11
	TIOB11_2		22	22	G4
Base Timer 12	TIOA12_0	Base timer ch.12 TIOA pin	6	6	D2
	TIOA12_1		116	-	G10
	TIOA12_2		34	26	J3
	TIOB12_0	Base timer ch.12 TIOB pin	143	-	D10
	TIOB12_1		117	-	G9
	TIOB12_2		35	27	J2
Base Timer 13	TIOA13_0	Base timer ch.13 TIOA pin	7	7	D1
	TIOA13_1		23	23	G5
	TIOA13_2		100	84	J12
	TIOB13_0	Base timer ch.13 TIOB pin	144	-	B9
	TIOB13_1		24	24	G6
	TIOB13_2		101	85	J11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 14	TIOA14_0	Base timer ch.14 TIOA pin	151	121	D8
	TIOA14_1		78	-	N10
	TIOA14_2		102	86	J10
	TIOB14_0	Base timer ch.14 TIOB pin	164	134	B6
	TIOB14_1		79	-	L10
	TIOB14_2		103	87	J9
Base Timer 15	TIOA15_0	Base timer ch.15 TIOA pin	73	65	N9
	TIOA15_1		80	-	K10
	TIOA15_2		104	88	H10
	TIOB15_0	Base timer ch.15 TIOB pin	74	66	M9
	TIOB15_1		81	-	M10
	TIOB15_2		105	89	H9
CAN 0	TX0_0	CAN interface ch.0 TX output pin	65	57	J6
	TX0_1		32	-	J5
	TX0_2		7	7	D1
	RX0_0	CAN interface ch.0 RX output pin	66	58	N8
	RX0_1		33	-	J4
	RX0_2		6	6	D2
CAN 1	TX1_0	CAN interface ch.1 TX output pin	122	98	E10
	TX1_1		23	23	G5
	TX1_2		92	76	L13
	RX1_0	CAN interface ch.1 RX output pin	123	99	E11
	RX1_1		22	22	G4
	RX1_2		91	75	M12
Debugger	SWCLK	Serial wire debug interface clock input pin	135	111	A12
	SWDIO	Serial wire debug interface data input / output pin	137	113	B12
	SWO	Serial wire viewer output pin	138	114	B11
	TCK	JTAG test clock input pin	135	111	A12
	TDI	JTAG test data input pin	136	112	C12
	TDO	JTAG debug data output pin	138	114	B11
	TMS	JTAG test mode state input/output pin	137	113	B12
	TRACECLK	Trace CLK output pin of ETM	12	12	E4
	TRACED0	Trace data output pin of ETM	8	8	D3
	TRACED1		9	9	D4
	TRACED2		10	10	E2
	TRACED3		11	11	E3
	TRSTX	JTAG test reset input pin	134	110	B13

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Bus	MAD00_0	External bus interface address bus	94	78	L11
	MAD01_0		95	79	K13
	MAD02_0		96	80	K12
	MAD03_0		97	81	K14
	MAD04_0		98	82	K11
	MAD05_0		99	83	J13
	MAD06_0		100	84	J12
	MAD07_0		101	85	J11
	MAD08_0		102	86	J10
	MAD09_0		103	87	J9
	MAD10_0		104	88	H10
	MAD11_0		105	89	H9
	MAD12_0		118	94	F10
	MAD13_0		119	95	F11
	MAD14_0		120	96	F12
	MAD15_0		121	97	F13
	MAD16_0		122	98	E10
	MAD17_0		123	99	E11
	MAD18_0		127	103	D13
	MAD19_0		139	-	C11
	MAD20_0		140	-	D11
	MAD21_0		141	-	B10
	MAD22_0		142	-	C10
	MAD23_0		143	-	D10
	MAD24_0		144	-	B9
	MCSX0_0	External bus interface chip select output pin	23	23	G5
	MCSX1_0		24	24	G6
	MCSX2_0		34	26	J3
	MCSX3_0		35	27	J2
	MCSX4_0		93	77	L12
	MCSX5_0		92	76	L13
	MCSX6_0		91	75	M12
	MCSX7_0		90	74	M13
	MDQM0_0	External bus interface byte mask signal output pin	15	15	F2
	MDQM1_0		16	16	F3
	MOEX_0	External bus interface read enable signal for SRAM	13	13	E5
	MWEX_0	External bus interface write enable signal for SRAM	14	14	F1

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Bus	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	19	19	F6
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	20	20	G2
	MNREX_0	External bus interface read enable signal to control NAND Flash	22	22	G4
	MNWEX_0	External bus interface write enable signal to control NAND Flash	21	21	G3
	MADATA00_0	External bus interface data bus (Address / data multiplex bus)	60	52	K5
	MADATA01_0		61	53	N6
	MADATA02_0		62	54	M6
	MADATA03_0		63	55	L6
	MADATA04_0		64	56	K6
	MADATA05_0		65	57	J6
	MADATA06_0		66	58	N8
	MADATA07_0		67	59	M8
	MADATA08_0		68	60	L8
	MADATA09_0		69	61	K8
	MADATA10_0		70	62	P8
	MADATA11_0		71	63	J8
	MADATA12_0		72	64	P9
	MADATA13_0		73	65	N9
	MADATA14_0		74	66	M9
	MADATA15_0		75	67	L9
	MALE_0	External bus interface Address Latch enable output signal for multiplex	17	17	F4
	MRDY_0	External bus interface external RDY input signal	18	18	F5
	MCLKOUT_0	External bus interface external clock output pin	36	28	K1

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT00_0	External interrupt request 00 input pin	13	13	E5
	INT00_1		8	8	D3
	INT00_2		165	135	C6
	INT01_0	External interrupt request 01 input pin	14	14	F1
	INT01_1		9	9	D4
	INT01_2		123	99	E11
	INT02_0	External interrupt request 02 input pin	15	15	F2
	INT02_1		91	75	M12
	INT02_2		120	96	F12
	INT03_0	External interrupt request 03 input pin	6	6	D2
	INT03_1		94	78	L11
	INT03_2		28	-	H3
	INT04_0	External interrupt request 04 input pin	31	-	H6
	INT04_1		97	81	K14
	INT04_2		29	-	H4
	INT05_0	External interrupt request 05 input pin	127	103	D13
	INT05_1		100	84	J12
	INT05_2		30	-	H5
	INT06_0	External interrupt request 06 input pin	170	-	B4
	INT06_1		126	102	D12
	INT06_2		64	56	K6
	INT07_0	External interrupt request 07 input pin	171	-	C4
	INT07_1		70	62	P8
	INT07_2		16	16	F3
	INT08_0	External interrupt request 08 input pin	172	140	B3
	INT08_1		33	-	J4
	INT08_2		19	19	F6
	INT09_0	External interrupt request 09 input pin	119	95	F11
	INT09_1		34	26	J3
	INT09_2		22	22	G4
	INT10_0	External interrupt request 10 input pin	76	-	K9
	INT10_1		35	27	J2
	INT10_2		7	7	D1
	INT11_0	External interrupt request 11 input pin	77	-	P10
	INT11_1		36	28	K1
	INT11_2		71	63	J8
	INT12_0	External interrupt request 12 input pin	78	-	N10
	INT12_1		46	38	N2
	INT12_2		72	64	P9
	INT13_0	External interrupt request 13 input pin	81	-	M10
	INT13_1		47	39	N3
	INT13_2		66	58	N8
	INT14_0	External interrupt request 14 input pin	82	-	N11
	INT14_1		58	50	M5
	INT14_2		67	59	M8

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT15_0	External interrupt request 15 input pin	83	-	M11
	INT15_1		169	139	C5
	INT15_2		68	60	L8
	INT16_0	External interrupt request 16 input pin	110	-	H13
	INT16_1		20	20	G2
	INT17_0	External interrupt request 17 input pin	111	-	H12
	INT17_1		21	21	G3
	INT18_0	External interrupt request 18 input pin	112	-	H11
	INT18_1		23	23	G5
	INT19_0	External interrupt request 19 input pin	113	-	G13
	INT19_1		24	24	G6
	INT20_0	External interrupt request 20 input pin	114	-	G12
	INT20_1		96	80	K12
	INT21_0	External interrupt request 21 input pin	115	-	G11
	INT21_1		98	82	K11
	INT22_0	External interrupt request 22 input pin	116	-	G10
	INT22_1		99	83	J13
	INT23_0	External interrupt request 23 input pin	117	-	G9
	INT23_1		74	66	M9
	INT24_0	External interrupt request 24 input pin	79	-	L10
	INT24_1		75	67	L9
	INT25_0	External interrupt request 25 input pin	80	-	K10
	INT25_1		101	85	J11
	INT26_0	External interrupt request 26 input pin	143	-	D10
	INT26_1		102	86	J10
	INT27_0	External interrupt request 27 input pin	144	-	B9
	INT27_1		103	87	J9
	INT28_0	External interrupt request 28 input pin	25	-	H1
	INT28_1		104	88	H10
	INT29_0	External interrupt request 29 input pin	26	-	H2
	INT29_1		105	89	H9
	INT30_0	External interrupt request 30 input pin	139	-	C11
	INT30_1		163	133	F7
	INT31_0	External interrupt request 31 input pin	140	-	D11
	INT31_1		164	134	B6
	NMIX	Non-Maskable Interrupt input pin	128	104	C13

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P00	General-purpose I/O port 0	134	110	B13
	P01		135	111	A12
	P02		136	112	C12
	P03		137	113	B12
	P04		138	114	B11
	P05		8	8	D3
	P06		9	9	D4
	P07		10	10	E2
	P08		11	11	E3
	P09		12	12	E4
	P10	General-purpose I/O port 1	90	74	M13
	P11		91	75	M12
	P12		92	76	L13
	P13		93	77	L12
	P14		94	78	L11
	P15		95	79	K13
	P16		96	80	K12
	P17		97	81	K14
	P18		98	82	K11
	P19		99	83	J13
	P1A		100	84	J12
	P1B		101	85	J11
	P1C		102	86	J10
	P1D		103	87	J9
	P1E		104	88	H10
	P1F		105	89	H9
	P20	General-purpose I/O port 2	127	103	D13
	P21		126	102	D12
	P22		125	101	E13
	P23		124	100	E12
	P24		123	99	E11
	P25		122	98	E10
	P26		121	97	F13
	P27		120	96	F12
	P28		119	95	F11
	P29		118	94	F10

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P30	General-purpose I/O port 3	28	-	H3
	P31		29	-	H4
	P32		30	-	H5
	P33		31	-	H6
	P34		32	-	J5
	P35		33	-	J4
	P36		34	26	J3
	P37		35	27	J2
	P38		36	28	K1
	P39		37	29	K2
	P3A		38	30	K3
	P3B		39	31	K4
	P3C		40	32	L1
	P3D		41	33	L2
	P3E		42	34	L3
	P3F		43	35	M2
	P40	General-purpose I/O port 4	46	38	N2
	P41		47	39	N3
	P42		48	40	M3
	P43		49	41	L4
	P44		50	42	M4
	P45		51	43	N4
	P46		55	47	P5
	P47		56	48	P6
	P48		58	50	M5
	P49		59	51	L5
	P4A		60	52	K5
	P4B		61	53	N6
	P4C		62	54	M6
	P4D		63	55	L6
	P4E		64	56	K6
	P50	General-purpose I/O port 5	13	13	E5
	P51		14	14	F1
	P52		15	15	F2
	P53		16	16	F3
	P54		17	17	F4
	P55		18	18	F5
	P56		19	19	F6
	P57		20	20	G2
	P58		21	21	G3
	P59		22	22	G4
	P5A		23	23	G5
	P5B		24	24	G6
	P5C		25	-	H1
	P5D		26	-	H2

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P60	General-purpose I/O port 6	169	139	C5
	P61		168	138	B5
	P62		167	137	E6
	P70	General-purpose I/O port 7	65	57	J6
	P71		66	58	N8
	P72		67	59	M8
	P73		68	60	L8
	P74		69	61	K8
	P75		70	62	P8
	P76		71	63	J8
	P77		72	64	P9
	P78		73	65	N9
	P79		74	66	M9
	P7A		75	67	L9
	P7B		76	-	K9
	P7C		77	-	P10
	P7D		78	-	N10
	P7E		79	-	L10
	P7F		80	-	K10
	P80	General-purpose I/O port 8	174	142	A3
	P81		175	143	A2
	P82		130	106	D14
	P83		131	107	C14
	P90	General-purpose I/O port 9	139	-	C11
	P91		140	-	D11
	P92		141	-	B10
	P93		142	-	C10
	P94		143	-	D10
	P95		144	-	B9
	PA0	General-purpose I/O port A	2	2	B2
	PA1		3	3	C2
	PA2		4	4	C3
	PA3		5	5	D5
	PA4		6	6	D2
	PA5		7	7	D1
	PB0	General-purpose I/O port B	110	-	H13
	PB1		111	-	H12
	PB2		112	-	H11
	PB3		113	-	G13
	PB4		114	-	G12
	PB5		115	-	G11
	PB6		116	-	G10
	PB7		117	-	G9

Module	Pin name	Function	Pin no		
			LQFP-176	LQFP-144	BGA-192
GPIO	PC0	General-purpose I/O port C	145	115	C9
	PC1		146	116	B8
	PC2		147	117	D9
	PC3		148	118	E9
	PC4		149	119	F9
	PC5		150	120	C8
	PC6		151	121	D8
	PC7		152	122	E8
	PC8		153	123	A10
	PC9		154	124	F8
	PCA		155	125	B7
	PCB		158	128	A7
	PCC		159	129	C7
	PCD		160	130	A6
	PCE		161	131	D7
	PCF		162	132	E7
	PD0	General-purpose I/O port D	163	133	F7
	PD1		164	134	B6
	PD2		165	135	C6
	PD3		166	136	D6
	PE0	General-purpose I/O port E	84	68	N13
	PE2		86	70	P12
	PE3		87	71	P13
	PF0	General-purpose I/O port F [*1]	81	-	M10
	PF1		82	-	N11
	PF2		83	-	M11
	PF3		170	-	B4
	PF4		171	-	C4
	PF5		172	140	B3
	PF6		128	104	C13

Module	Pin name	Function	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	126	102	D12
	SIN0_1		94	78	L11
	SIN0_2		114	-	G12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	125	101	E13
	SOT0_1 (SDA0_1)		95	79	K13
	SOT0_2 (SDA0_2)		115	-	G11
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4).	124	100	E12
	SCK0_1 (SCL0_1)		96	80	K12
	SCK0_2 (SCL0_2)		116	-	G10
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	19	19	F6
	SIN1_1		91	75	M12
	SIN1_2		81	-	M10
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	20	20	G2
	SOT1_1 (SDA1_1)		92	76	L13
	SOT1_2 (SDA1_2)		82	-	N11
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4).	21	21	G3
	SCK1_1 (SCL1_1)		93	77	L12
	SCK1_2 (SCL1_2)		83	-	M11

Module	Pin name	Function	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	67	59	M8
	SIN2_1		123	99	E11
	SIN2_2		97	81	K14
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	68	60	L8
	SOT2_1 (SDA2_1)		122	98	E10
	SOT2_2 (SDA2_2)		98	82	K11
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I^2C (operation mode 4).	69	61	K8
	SCK2_1 (SCL2_1)		121	97	F13
	SCK2_2 (SCL2_2)		99	83	J13
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	70	62	P8
	SIN3_1		13	13	E5
	SIN3_2		58	50	M5
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	71	63	J8
	SOT3_1 (SDA3_1)		14	14	F1
	SOT3_2 (SDA3_2)		59	51	L5
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I^2C (operation mode 4).	72	64	P9
	SCK3_1 (SCL3_1)		15	15	F2
	SCK3_2 (SCL3_2)		60	52	K5

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	165	135	C6
	SIN4_1		100	84	J12
	SIN4_2		8	8	D3
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	164	134	B6
	SOT4_1 (SDA4_1)		101	85	J11
	SOT4_2 (SDA4_2)		9	9	D4
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	163	133	F7
	SCK4_1 (SCL4_1)		102	86	J10
	SCK4_2 (SCL4_2)		10	10	E2
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	161	131	D7
	RTS4_1		104	88	H10
	RTS4_2		12	12	E4
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	162	132	E7
	CTS4_1		103	87	J9
	CTS4_2		11	11	E3
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	169	139	C5
	SIN5_1		141	-	B10
	SIN5_2		34	26	J3
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	168	138	B5
	SOT5_1 (SDA5_1)		142	-	C10
	SOT5_2 (SDA5_2)		35	27	J2
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	167	137	E6
	SCK5_1 (SCL5_1)		143	-	D10
	SCK5_2 (SCL5_2)		36	28	K1

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	16	16	F3
	SIN6_1		31	-	H6
	SIN6_2		170	-	B4
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	17	17	F4
	SOT6_1 (SDA6_1)		30	-	H5
	SOT6_2 (SDA6_2)		171	-	C4
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	18	18	F5
	SCK6_1 (SCL6_1)		29	-	H4
	SCK6_2 (SCL6_2)		172	140	B3
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	22	22	G4
	SIN7_1		64	56	K6
	SIN7_2		110	-	H13
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	23	23	G5
	SOT7_1 (SDA7_1)		63	55	L6
	SOT7_2 (SDA7_2)		111	-	H12
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	24	24	G6
	SCK7_1 (SCL7_1)		62	54	M6
	SCK7_2 (SCL7_2)		112	-	H11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	37	29	K2
	DTTI0X_1		104	88	H10
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	32	-	J5
	FRCK0_1		105	89	H9
	FRCK0_2		91	75	M12
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. (ICxx describes channel number)	36	28	K1
	IC00_1		100	84	J12
	IC00_2		92	76	L13
	IC01_0		35	27	J2
	IC01_1		101	85	J11
	IC01_2		93	77	L12
	IC02_0		34	26	J3
	IC02_1		102	86	J10
	IC02_2		94	78	L11
	IC03_0		33	-	J4
	IC03_1		103	87	J9
	IC03_2		95	79	K13
	RTO00_0 (PPG00_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	38	30	K3
	RTO00_1 (PPG00_1)		124	100	E12
	RTO01_0 (PPG00_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	39	31	K4
	RTO01_1 (PPG00_1)		123	99	E11
	RTO02_0 (PPG02_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	40	32	L1
	RTO02_1 (PPG02_1)		122	98	E10
	RTO03_0 (PPG02_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	41	33	L2
	RTO03_1 (PPG02_1)		121	97	F13
	RTO04_0 (PPG04_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	42	34	L3
	RTO04_1 (PPG04_1)		120	96	F12
	RTO05_0 (PPG04_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	43	35	M2
	RTO05_1 (PPG04_1)		119	95	F11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	19	19	F6
	DTTI1X_1		58	50	M5
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	2	2	B2
	FRCK1_1		63	55	L6
	IC10_0	16-bit input capture ch.1 input pin of multi-function timer 1. (ICxx describes channel number)	3	3	C2
	IC10_1		59	51	L5
	IC11_0		4	4	C3
	IC11_1		60	52	K5
	IC12_0		5	5	D5
	IC12_1		61	53	N6
	IC13_0		6	6	D2
	IC13_1		62	54	M6
	RTO10_0 (PPG10_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	13	13	E5
	RTO10_1 (PPG10_1)		46	38	N2
	RTO11_0 (PPG10_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	14	14	F1
	RTO11_1 (PPG10_1)		47	39	N3
	RTO12_0 (PPG12_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	15	15	F2
	RTO12_1 (PPG12_1)		48	40	M3
	RTO13_0 (PPG12_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	16	16	F3
	RTO13_1 (PPG12_1)		49	41	L4
	RTO14_0 (PPG14_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	17	17	F4
	RTO14_1 (PPG14_1)		50	42	M4
	RTO15_0 (PPG14_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	18	18	F5
	RTO15_1 (PPG14_1)		51	43	N4

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Timer 2	DTTI2X_0	Input signal controlling wave form generator outputs RTO20 to RTO25 of multi-function timer 2.	12	12	E4
	DTTI2X_1		26	-	H2
	FRCK2_0	16-bit free-run timer ch.2 external clock input pin	128	104	C13
	FRCK2_1		78	-	N10
	IC20_0	16-bit input capture ch.2 input pin of multi-function timer 2. (ICxx describes channel number)	13	13	E5
	IC20_1		25	-	H1
	IC21_0		14	14	F1
	IC21_1		79	-	L10
	IC22_0		15	15	F2
	IC22_1		80	-	K10
	IC23_0		16	16	F3
	IC23_1		81	-	M10
	RTO20_0 (PPG20_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	B2
	RTO20_1 (PPG20_1)		139	-	C11
	RTO21_0 (PPG20_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	C2
	RTO21_1 (PPG20_1)		140	-	D11
	RTO22_0 (PPG22_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	C3
	RTO22_1 (PPG22_1)		141	-	B10
	RTO23_0 (PPG22_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	D5
	RTO23_1 (PPG22_1)		142	-	C10
	RTO24_0 (PPG24_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	D2
	RTO24_1 (PPG24_1)		143	-	D10
	RTO25_0 (PPG24_0)	Wave form generator output pin of multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	D1
	RTO25_1 (PPG24_1)		144	-	B9

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	28	-	H3
	AIN0_1		59	51	L5
	AIN0_2		13	13	E5
	BIN0_0	QPRC ch.0 BIN input pin	29	-	H4
	BIN0_1		60	52	K5
	BIN0_2		14	14	F1
	ZIN0_0	QPRC ch.0 ZIN input pin	30	-	H5
	ZIN0_1		61	53	N6
	ZIN0_2		15	15	F2
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	73	65	N9
	AIN1_1		127	103	D13
	AIN1_2		62	54	M6
	BIN1_0	QPRC ch.1 BIN input pin	74	66	M9
	BIN1_1		126	102	D12
	BIN1_2		63	55	L6
	ZIN1_0	QPRC ch.1 ZIN input pin	75	67	L9
	ZIN1_1		125	101	E13
	ZIN1_2		64	56	K6
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	67	59	M8
	AIN2_1		170	-	B4
	AIN2_2		115	-	G11
	BIN2_0	QPRC ch.2 BIN input pin	68	60	L8
	BIN2_1		171	-	C4
	BIN2_2		116	-	G10
	ZIN2_0	QPRC ch.2 ZIN input pin	69	61	K8
	ZIN2_1		172	140	B3
	ZIN2_2		117	-	G9
USB0	UDM0	USB ch.0 device/host D – pin	174	142	A3
	UDP0	USB ch.0 device/host D + pin	175	143	A2
	UHCONX0	USB ch.0. USB external pull-up control pin	168	138	B5
USB1	UDM1	USB ch.1 device/host D – pin	130	106	D14
	UDP1	USB ch.1 device/host D + pin	131	107	C14
	UHCONX1	USB ch.1. USB external pull-up control pin	127	103	D13

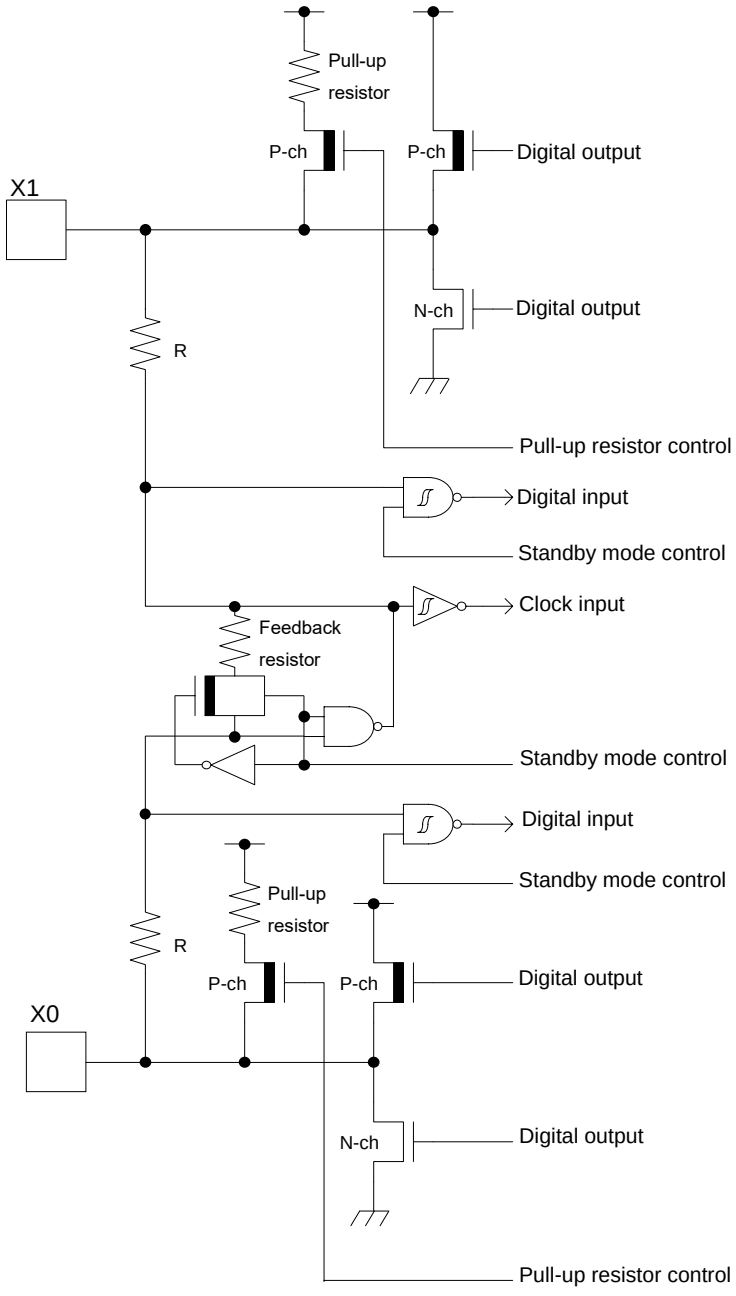
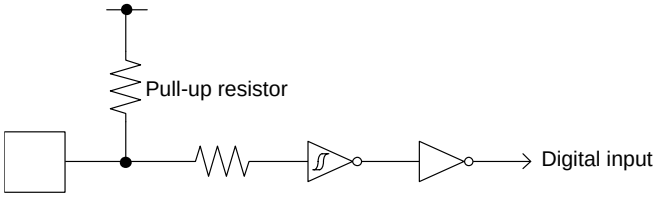
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Ethernet	E_COL0	Ch.0 collision detection	154	124	F8
	E_COUT	Clock output pin for EtherPHY	158	128	A7
	E_CRS0	Ch.0 carrier detection	155	125	B7
	E_MDC0	Ch.0 management clock	152	122	E8
	E_MDIO0	Ch.0 management data input/output	151	121	D8
	E_MDIO1	Ch.1 management data input/output	159	129	C7
	E_PPS0_PPS1	Ch.0 PTP counter monitor/ Ch.1 PTP counter monitor	167	137	E6
	E_RX00	Ch.0 received data0	149	119	F9
	E_RX01	Ch.0 received data1	148	118	E9
	E_RX02_RX10	Ch.0 received data2/ Ch.1 received data0	147	117	D9
	E_RX03_RX11	Ch.0 received data3/ Ch.1 received data1	146	116	B8
	E_RXCK0_REFCK	Ch.0 received clock input/ reference clock	153	123	A10
	E_RXDV0	Ch.0 received data enable	150	120	C8
	E_RXER0_RXDV1	Ch.0 received data error detection/ Ch.1 received data enable	145	115	C9
	E_TCK0_MDC1	Ch.0 transition clock input/ Ch.1 management clock	160	130	A6
	E_TX00	Ch.0 transition data0	165	135	C6
	E_TX01	Ch.0 transition data1	164	134	B6
	E_TX02_TX10	Ch.0 transition data2/ Ch.1 transition data0	163	133	F7
	E_TX03_TX11	Ch.0 transition data3/ Ch.1 transition data1	162	132	E7
	E_TXEN0	Ch.0 transition data enable	166	136	D6
	E_TXER0_TXEN1	Ch.0 transition data error detection/ Ch.1 transition data enable	161	131	D7
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	57	49	N5
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	85	69	N12
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	84	68	N13

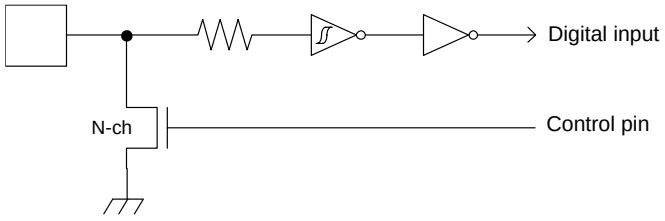
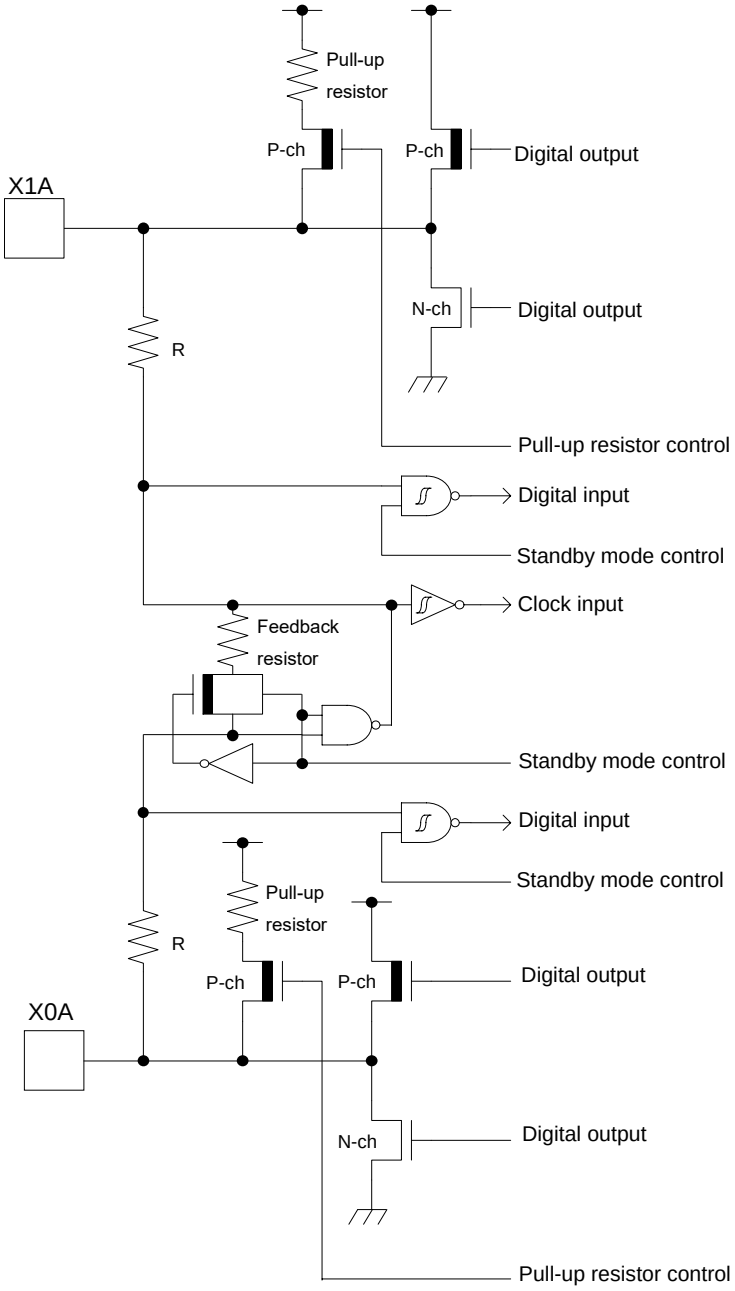
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Power	VCC	Power supply Pin	1	1	C1
	VCC	Power supply Pin	45	37	N1
	VCC	Power supply Pin	54	46	P4
	VCC	Power supply Pin	89	73	M14
	VCC	Power supply Pin	133	109	A13
	USBVCC0	3.3V Power supply port for USB I/O	173	141	A4
	USBVCC1		129	105	E14
	ETHVCC	Power supply pin for Ethernet I/O	156	126	A9
GND	VSS	GND Pin	27	25	J1
	VSS	GND Pin	44	36	M1
	VSS	GND Pin	53	45	P3
	VSS	GND Pin	88	72	N14
	VSS	GND Pin	109	93	F14
	VSS	GND Pin	132	108	B14
	VSS	GND Pin	157	127	A11
	VSS	GND Pin	176	144	B1
	VSS	GND Pin	-	-	E1
	VSS	GND Pin	-	-	G1
	VSS	GND Pin	-	-	P7
	VSS	GND Pin	-	-	P11
	VSS	GND Pin	-	-	L14
	VSS	GND Pin	-	-	A8
	VSS	GND Pin	-	-	A5
	VSS	GND Pin	-	-	N7
	VSS	GND Pin	-	-	M7
	VSS	GND Pin	-	-	L7
	VSS	GND Pin	-	-	K7
	VSS	GND Pin	-	-	J7
	VSS	GND Pin	-	-	G7
	VSS	GND Pin	-	-	H7
	VSS	GND Pin	-	-	H8
	VSS	GND Pin	-	-	G8
Clock	X0	Main clock (oscillation) input pin	86	70	P12
	X0A	Sub clock (oscillation) input pin	55	47	P5
	X1	Main clock (oscillation) I/O pin	87	71	P13
	X1A	Sub clock (oscillation) I/O pin	56	48	P6
	CROUT_0	Bulit-in high-speed CR-osc clock output port	127	103	D13
	CROUT_1		152	122	E8
Analog Power	AVCC	A/D converter analog power supply pin	106	90	J14
	AVRH	A/D converter analog reference voltage input pin	107	91	H14
Analog GND	AVSS	A/D converter GND pin	108	92	G14
C pin	C	Power stabilization capacity pin	52	44	P2

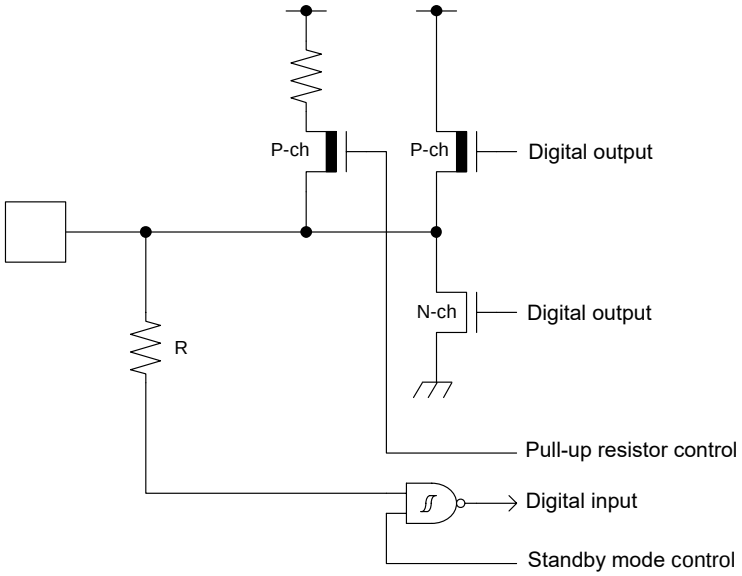
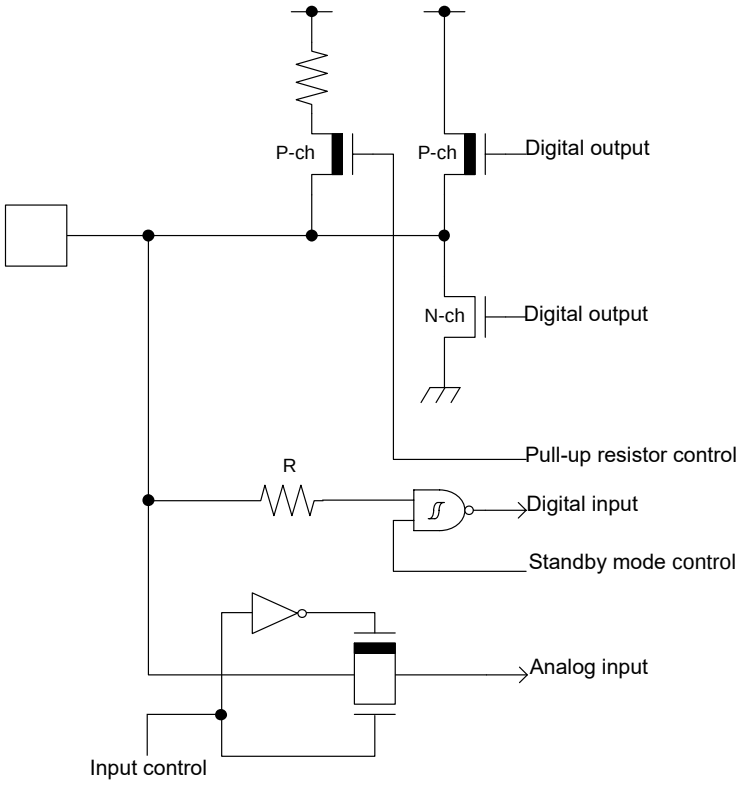
Note:

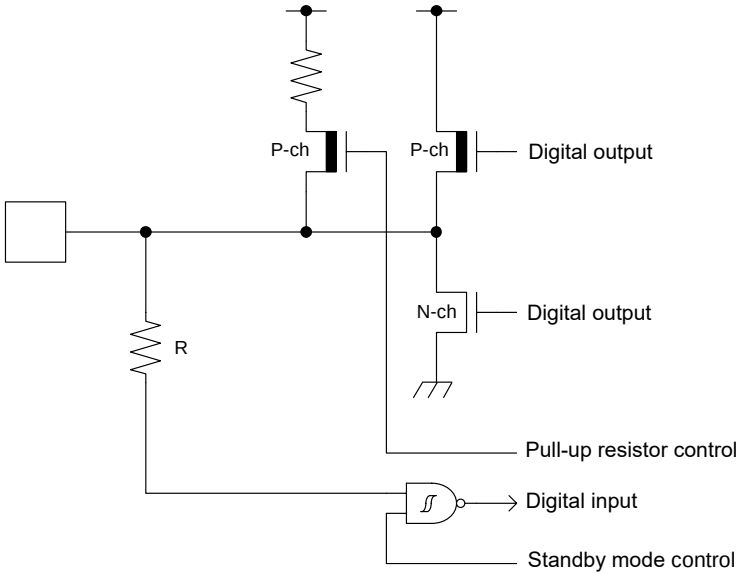
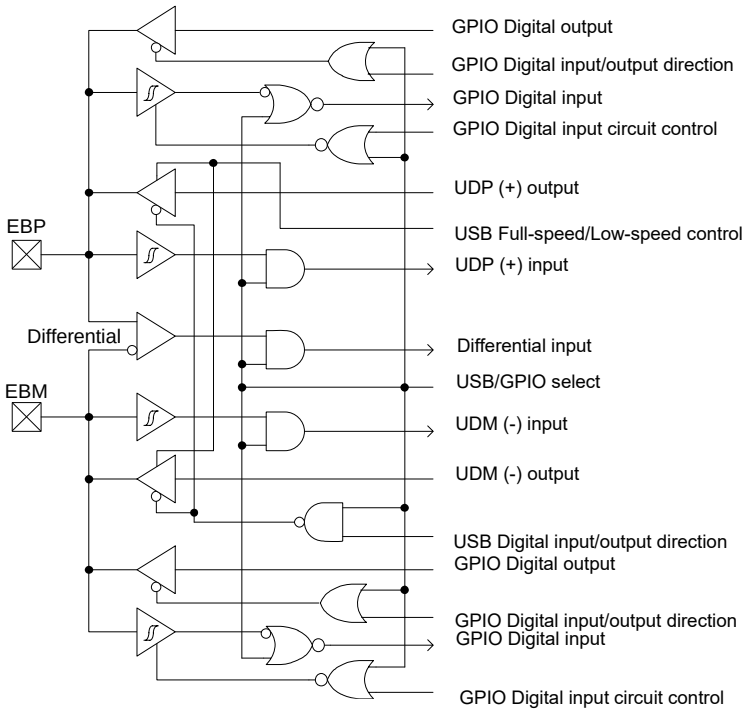
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

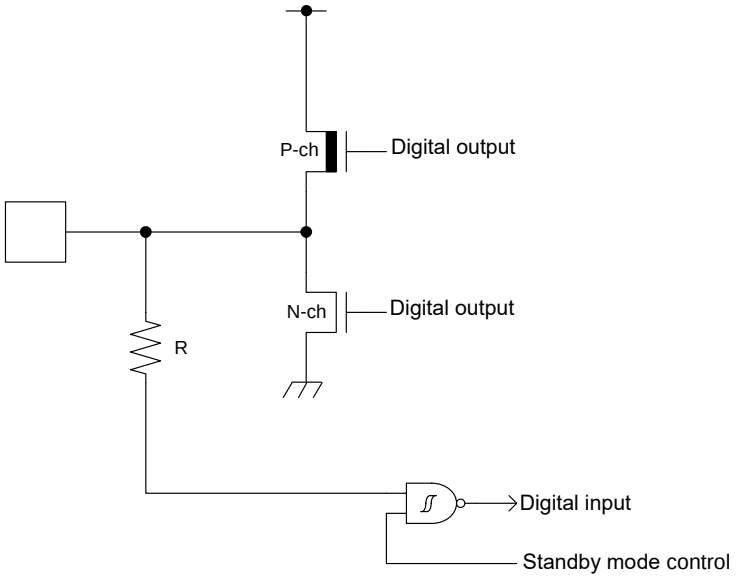
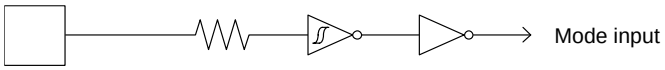
5. I/O Circuit Type

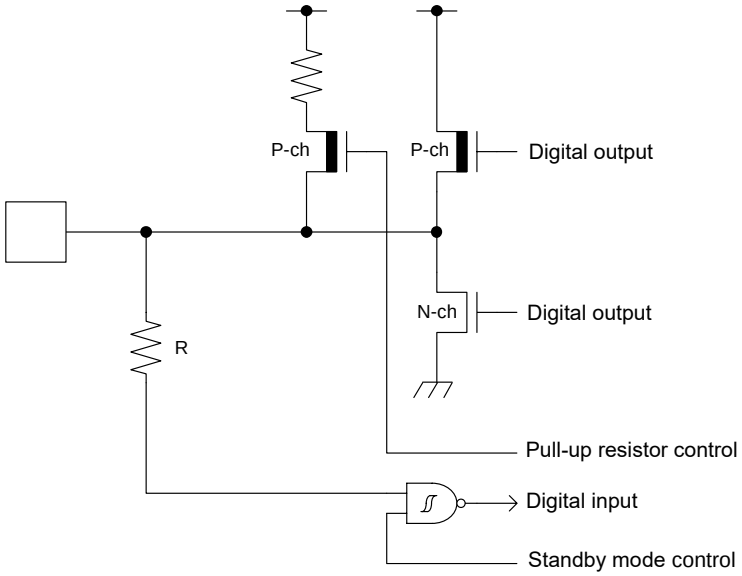
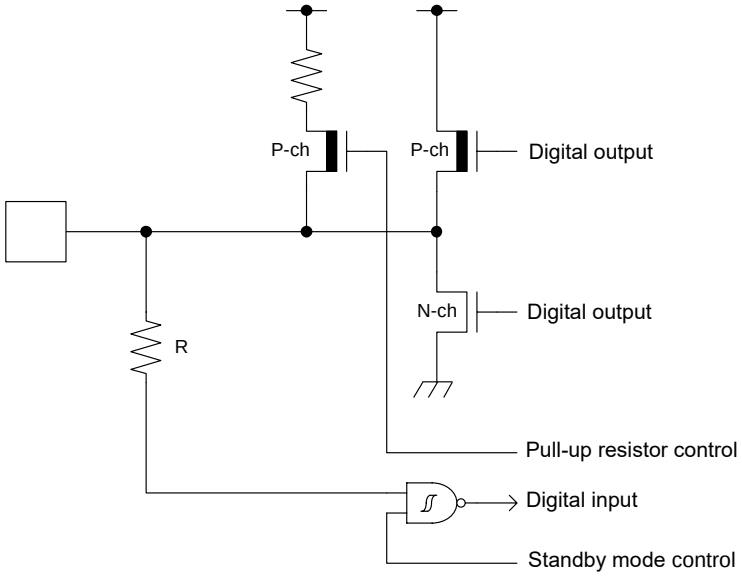
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor : Approximately 5 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
E		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – +B input is available
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. – Full-speed, Low-speed control When the GPIO is selected. – CMOS level output – CMOS level hysteresis input – With standby mode control – I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Type	Circuit	Remarks
I		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With standby mode control – I_{OH} = -4 mA, I_{OL} = 4 mA – Available to control of PZR registers. – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		– CMOS level hysteresis input

Type	Circuit	Remarks
K		– CMOS level output – TTL level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
L		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -8 mA, I_{OL} = 8 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress Inc. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pins and GND pins, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

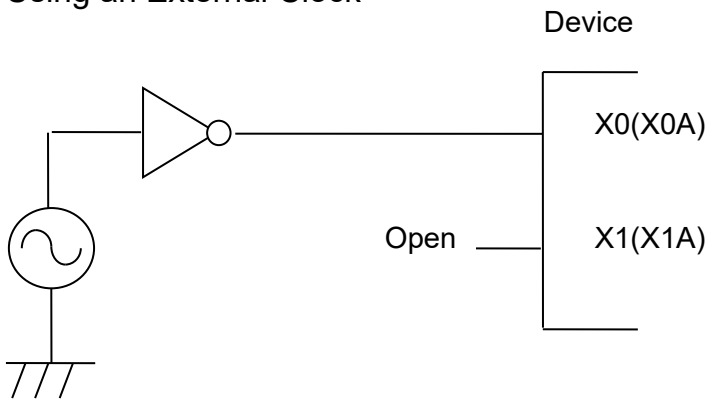
It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

When using an external clock, the clock signal should be input to the X0,X0A pin only and the X1,X1A pin should be kept open.

- Example of Using an External Clock

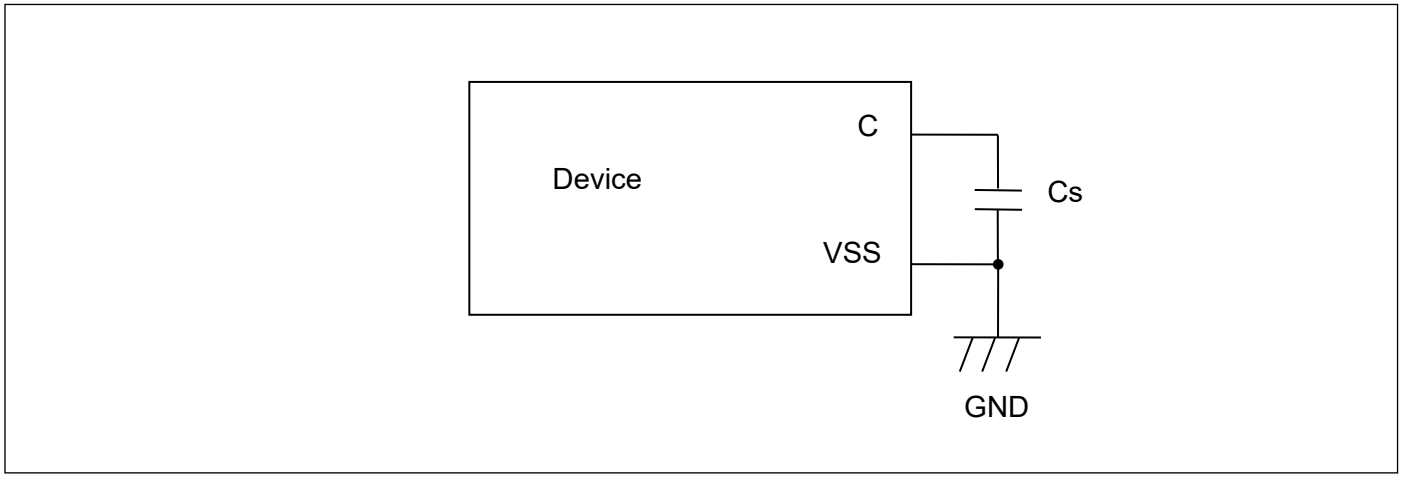


Handling when using Multi-function serial pin as I²C pin

If it is using multi-function serial pin as I²C pins, P-ch transistor of digital output is always disable. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC =VCC and AVSS = VSS.

Turning on: VCC → USBVCC0
VCC → USBVCC1
VCC → ETHVCC
VCC → AVCC → AVRH

Turning off: AVRH → AVCC → VCC
ETHVCC → VCC
USBVCC1 → VCC
USBVCC0 → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash products and MASK products

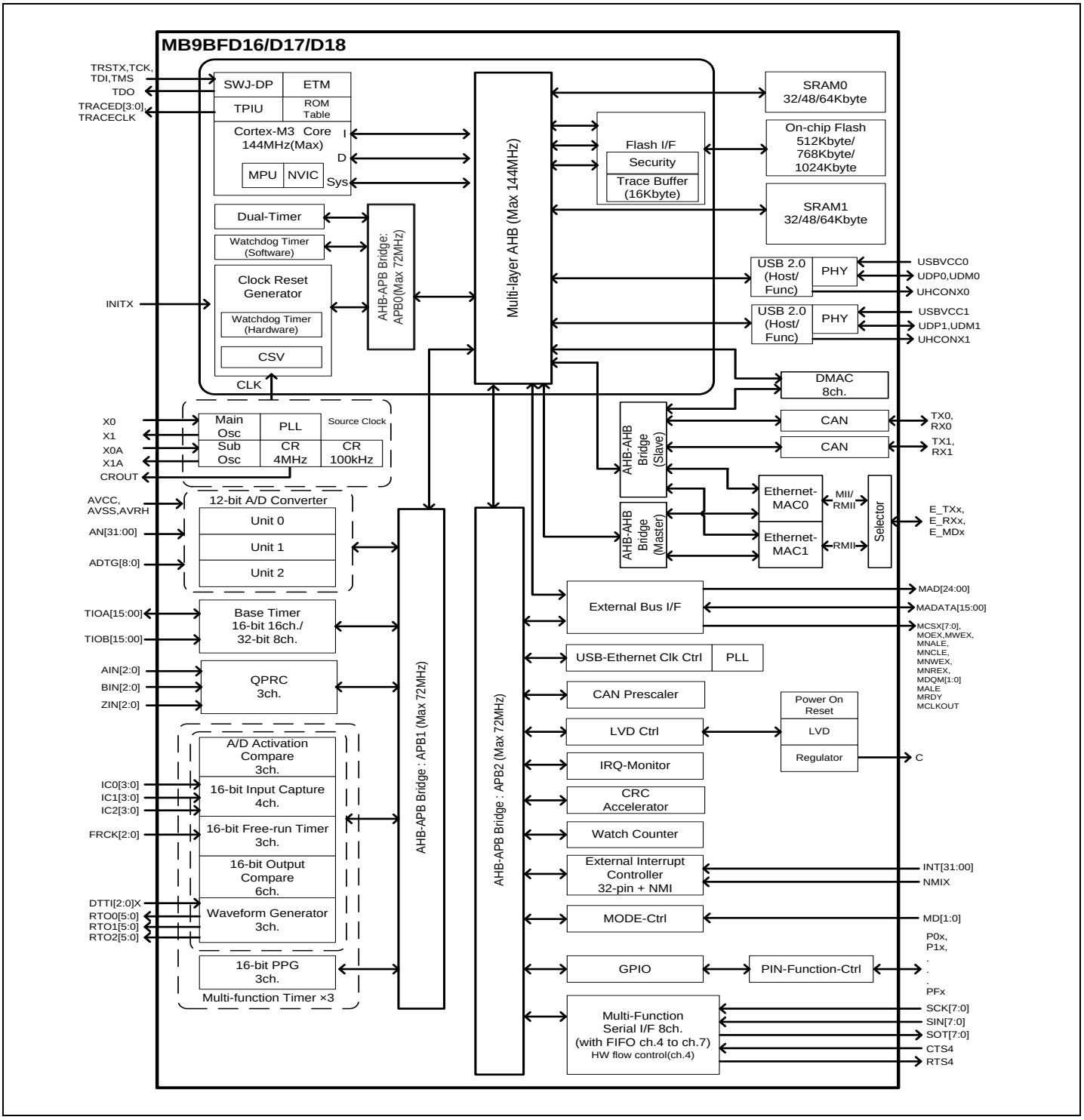
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Base Timer

In the case of using ch.8 and ch.9 at I/O mode 1 (timer full mode), the TIOA09 pin cannot be used for external startup trigger input (TGIN).
Be sure to use the pin with making ESG1 and ESG2 bits of the Timer Control Register (Ch.9-TMCR) in the Base Timer to be "0b00" in order to disable trigger input.

8. Block Diagram



Note:

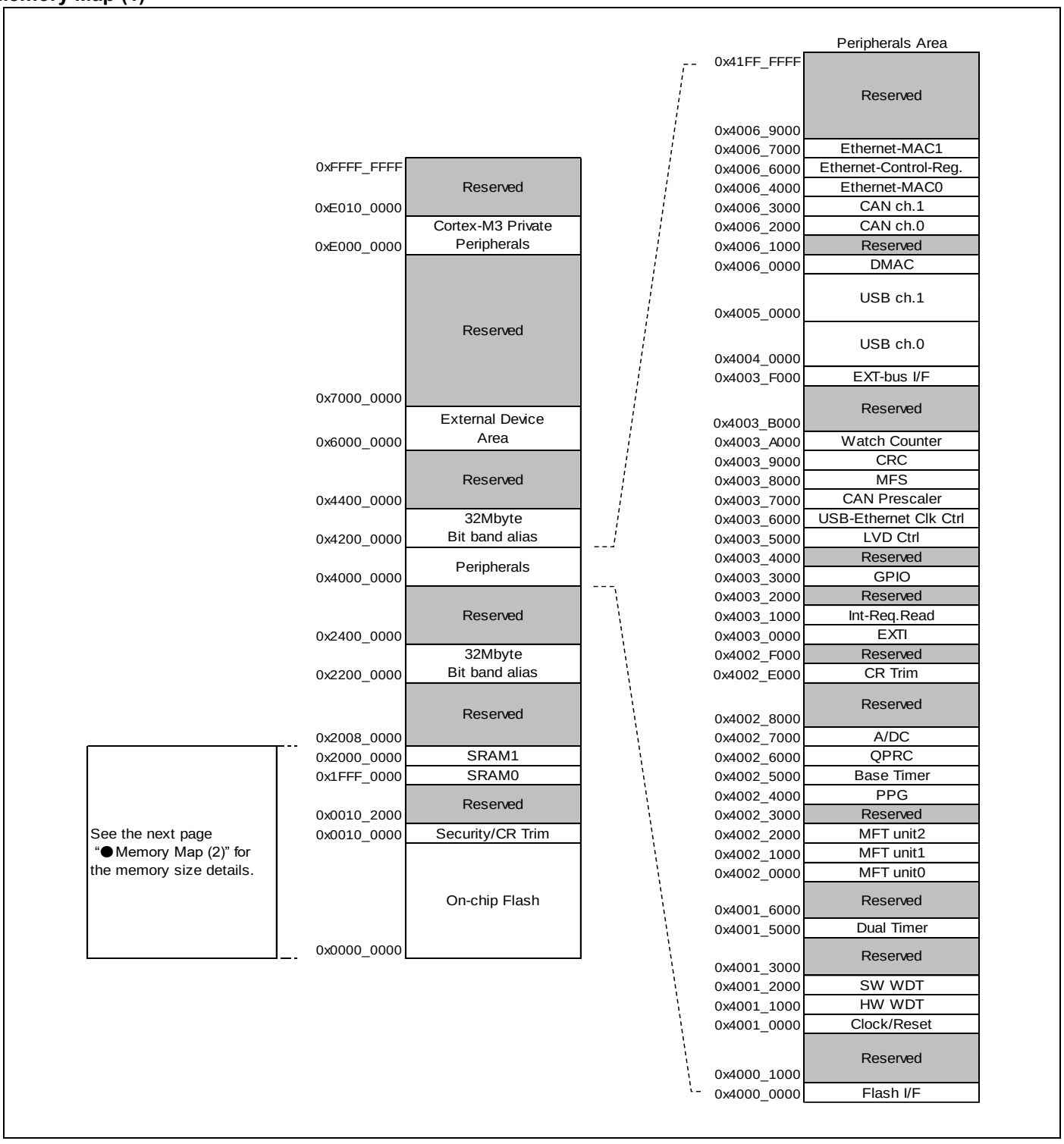
- *The following items vary depending on the package.*
  - Number of external bus interface pin
  - Number of 12-bit A/D converter channel

9. Memory Size

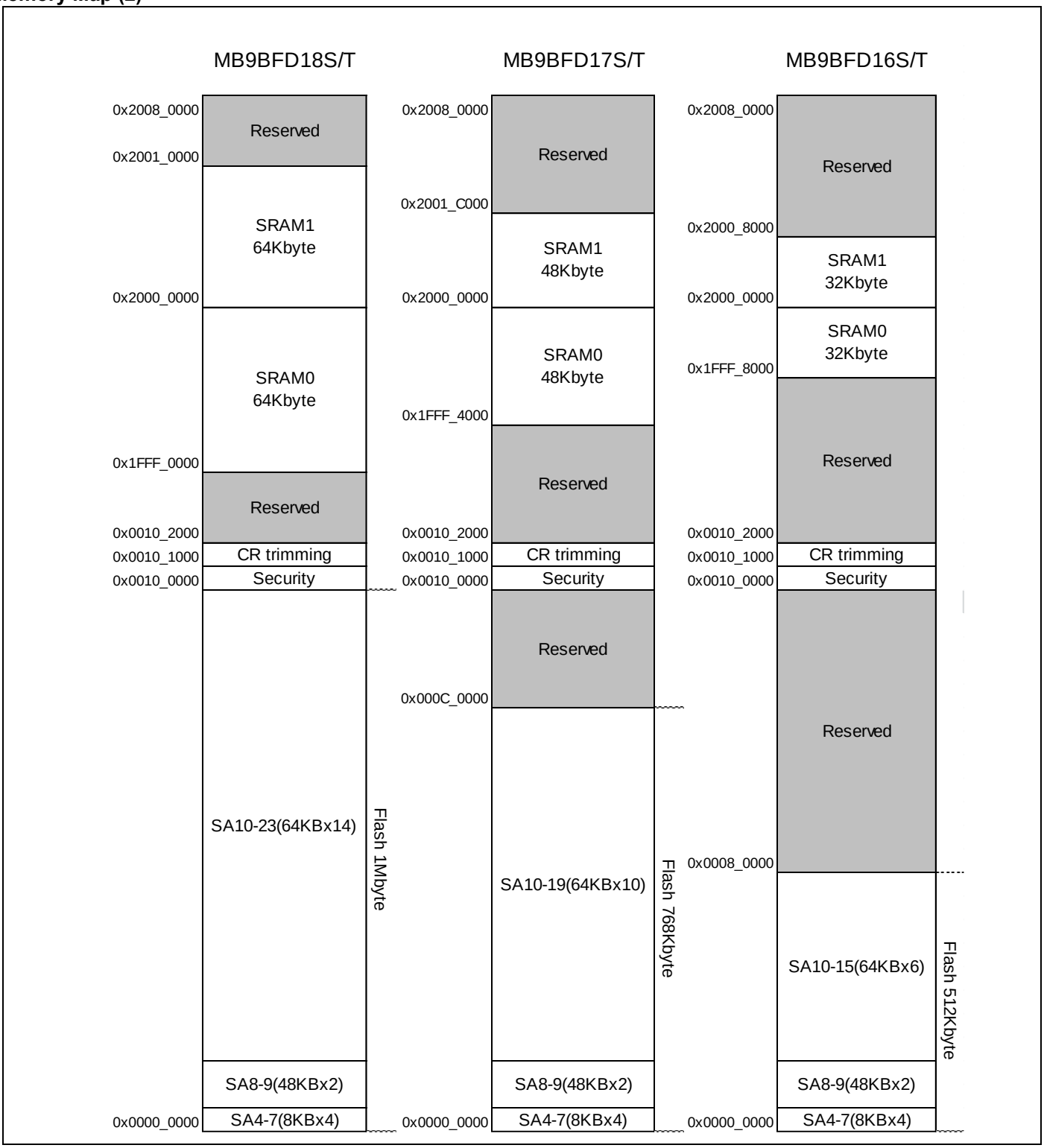
See “Memory size” in “1. Product Lineup” to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



See "CY9BD10T/610T/510T/410T/310T/210T/110T Series Flash Programming Manual" for sector structure of Flash.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Multi-function timer unit2
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter (QPRC)
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low-Voltage Detector
0x4003_6000	0x4003_6FFF		USB-Ethernet clock generator
0x4003_7000	0x4003_7FFF		CAN Prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External bus I/F
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4005_FFFF		USB ch.1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		CAN ch.0
0x4006_3000	0x4006_3FFF		CAN ch.1
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch.0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting Register
0x4006_7000	0x4006_8FFF		Ethernet-MAC ch.1
0x4006_9000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0

This is the period when the INITX pin is the "L" level.

■INITX=1

This is the period when the INITX pin is the "H" level.

■SPL=0

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".

■SPL=1

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".

■Input enabled

Indicates that the input function can be used.

■Internal input fixed at "0"

This is the status that the input function cannot be used. Internal input is fixed at "L".

■Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled

Indicates that the setting is disabled.

■Maintain previous state

Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled

Indicates that the analog input is enabled.

■Trace output

Indicates that the trace function can be used.

List of Pin Status

Pin Status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop[*1]/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop[*1]/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin Status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Hi-Z at transmission/ Input enabled/ Internal input fixed at "0" at reception	Hi-Z at transmission/ Input enabled/ Internal input fixed at "0" at reception
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Input enabled
Q	Ethernet input or output selected*3	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
R	Ethernet input or output pin selected*3	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	External interrupt enabled selected						
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

*1: Oscillation is stopped at Sub timer mode, Low-speed CR timer mode, and STOP mode.

*2: Oscillation is stopped at STOP mode.

*3: When selected by EPFR14.E_SPLC register.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[*1, *2]	Vcc	Vss - 0.5	Vss + 6.5	V	
Power supply voltage (for USB ch.0)[*1, *3]	USBVcc0	Vss - 0.5	Vss + 6.5	V	
Power supply voltage (for USB ch.1)[*1, *3]	USBVcc1	Vss - 0.5	Vss + 6.5	V	
Power supply voltage (for Ethernet)[*1, *4]	ETHVcc	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage[*1, *5]	AVcc	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage[*1, *5]	AVRH	Vss - 0.5	Vss + 6.5	V	
Input voltage[*1]	V_I	Vss - 0.5	Vcc + 0.5 (≤ 6.5 V)	V	Except for USB pin and Ethernet-MAC pin
		Vss - 0.5	USBVcc0 + 0.5 (≤ 6.5 V)	V	USB ch.0 pin
		Vss - 0.5	USBVcc1 + 0.5 (≤ 6.5 V)	V	USB ch.1 pin
		Vss - 0.5	ETHVcc + 0.5 (≤ 6.5 V)	V	Ethernet-MAC pin
		Vss - 0.5	Vss + 6.5	V	5 V tolerant
Analog pin input voltage[*1]	V_{IA}	Vss - 0.5	AVcc + 0.5 (≤ 6.5 V)	V	
Output voltage[*1]	V_O	Vss - 0.5	Vcc + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*9
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*9
"L" level maximum output current [*6]	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			39	mA	P80,P81,P82,P83
"L" level average output current [*7]	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			18.5	mA	P80,P81,P82,P83
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current [*8]	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current [*6]	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	8 mA type
			- 20	mA	12 mA type
			- 39	mA	P80,P81,P82,P83
"H" level average output current [*7]	I_{OHAV}	-	- 4	mA	4 mA type
			- 8	mA	8 mA type
			- 12	mA	12 mA type
			- 20.5	mA	P80,P81,P82,P83
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current [*8]	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	1000	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that Vss = AVss = 0.0 V.

*2: Vcc must not drop below Vss - 0.5 V.

*3: USBVcc0 and USBVcc1 must not drop below Vss - 0.5 V.

*4: ETHVcc must not drop below Vss - 0.5 V.

*5: Ensure that the voltage does not to exceed Vcc + 0.5 V, for example, when the power is turned on.

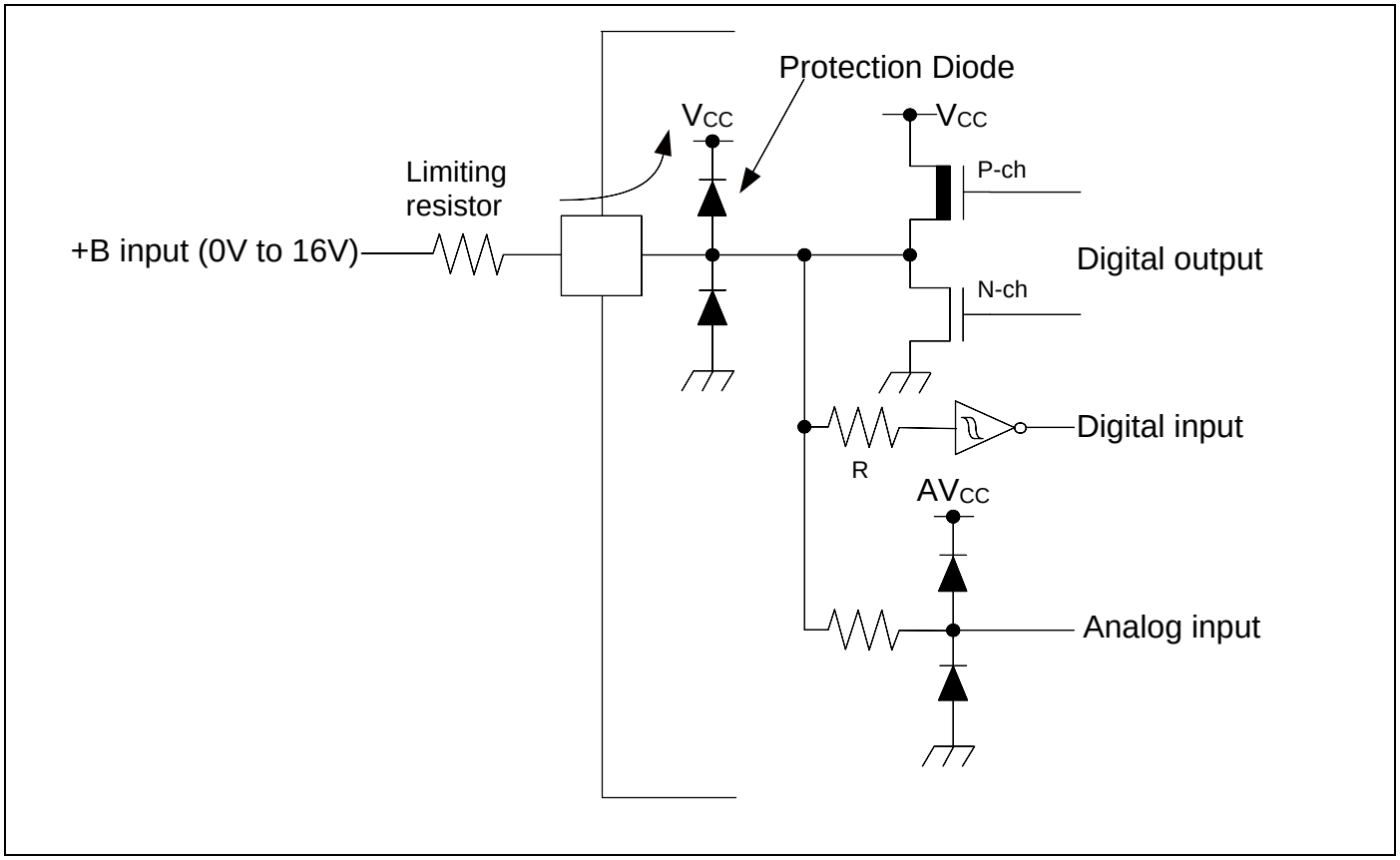
*6: The maximum output current is the peak value for a single pin.

*7: The average output is the average current for a single pin over a period of 100 ms.

*8: The total average output current is the average current for all pins over a period of 100 ms.

*9:

- See "4. List of Pin Functions" and "5. I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

– *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

12.2 Recommended Operating Conditions

(Vss = AVss = 0.0 V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		Vcc	-	2.7[8]	5.5	V	
Power supply voltage (3V power supply) for USB ch.0		USBVcc0	-	3.0	3.6 (≤ Vcc)	V	*1
				2.7	5.5 (≤ Vcc)		*2
Power supply voltage (3V power supply) for USB ch.1		USBVcc1	-	3.0	3.6 (≤ Vcc)	V	*3
				2.7	5.5 (≤ Vcc)		*4
Power supply voltage for Ethernet		ETHVcc	-	3.0	3.6 (≤ Vcc)	V	*5
				4.5	5.5 (≤ Vcc)		*5
				2.7	5.5 (≤ Vcc)		*6
Analog power supply voltage		AVcc	-	2.7	5.5	V	AVcc = Vcc
Analog reference voltage		AVRH	-	2.7	AVcc	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *7
Operating temperature	LQS144, LQP176, LBE192	T_A	When mounted on four-layer PCB	- 40	+ 85	°C	

*1: When P81/UDP0 and P80/UDM0 pin are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pin are used as GPIO (P81, P80).

*3: When P83/UDP1 and P82/UDM1 pin are used as USB (UDP1, UDM1).

*4: When P83/UDP1 and P82/UDM1 pin are used as GPIO (P83, P82).

*5: When the pins in "Ethernet-MAC pins" except P62/E_PPS0_PPS1/SCK5_0/ADTG_3 pin are used as Ethernet-MAC pin.

*6: When the pins in "Ethernet-MAC pins" except P62/E_PPS0_PPS1/SCK5_0/ADTG_3 pin are used as function pins other than Ethernet-MAC pin.

*7: See "C pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*8: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

– *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Ethernet-MAC pins

Pin Name	Ethernet-MAC function	Except for Ethernet-MAC function	Power Supply type
P62/E_PPS0_PPS1/SCK5_0/ADTG_3	E_PPS0_PPS1*1	P62 /SCK5_0/ADTG_3	Vcc
PC0/E_RXER0_RXDV1	E_RXER0_RXDV1	PC0	ETHVcc
PC1/E_RX03_RX11	E_RX03_RX11	PC1	
PC2/E_RX02_RX10	E_RX02_RX10	PC2	
PC3/E_RX01/TIOA06_1	E_RX01	PC3/TIOA06_1	
PC4/E_RX00/TIOA08_2	E_RX00	PC4/TIOA08_2	
PC5/E_RXDV0/TIOA10_2	E_RXDV0	PC5/TIOA10_2	
PC6/E_MDIO0/TIOA14_0	E_MDIO0	PC6/TIOA14_0	
PC7/E_MDC0/CROUT_1	E_MDC0	PC7/CROUT_1	
PC8/E_RXCK0_REFCK	E_RXCK0_REFCK	PC8	
PC9/E_COL0	E_COL0	PC9	
PCA/E_CRS0	E_CRS0	PCA	
PCB/E_COUT	E_COUT	PCB	
PCC/E_MDIO1	E_MDIO1	PCC	
PCD/E_TCK0_MDC1	E_TCK0_MDC1	PCD	
PCE/E_TXER0_TXEN1/RTS4_0/ TIOB06_1	E_TXER0_TXEN	PCE/RTS4_0/TIOB06_1	
PCF/E_TX03_TX11/CTS4_0/TIOB08_2	E_TX03_TX11	PCF/CTS4_0/TIOB08_2	
PD0/E_TX02_TX10/SCK4_0/TIOB10_2/ INT30_1	E_TX02_TX10	PD0/SCK4_0/TIOB10_2/ INT30_1	
PD1/E_TX01/SOT4_0/TIOB14_0/INT31_1	E_TX01	PD1/SOT4_0/TIOB14_0/ INT31_1	
PD2/E_TX00/SIN4_0/TIOA03_2/INT00_2	E_TX00	PD2/TIOA03_2/INT00_2	
PD3/E_TXEN0/TIOB03_2	E_TXEN0	PD3/TIOB03_2	

*1: It is used to confirm the PTP counter cycle in Ethernet-MAC by wave forms.

12.3 DC Characteristics

12.3.1 Current Rating

(Vcc = AVcc = USBVcc0 = USBVcc1 = ETHVcc = 2.7 V to 5.5 V, Vss = AVss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ[3]	Max[4]		
RUN mode current	Icc	VCC	PLL RUN mode	CPU: 144 MHz, Peripheral: 72 MHz, Flash 2 Wait, TraceBuffer: ON, FRWTR.RWT = 10, FSYNDN.SD = 000, FBFCR.BE = 1	100	180	mA	*1, *5
				CPU: 72 MHz, Peripheral: 72 MHz, Flash 0 Wait, TraceBuffer: OFF, FRWTR.RWT = 00, FSYNDN.SD = 000, FBFCR.BE = 0	65	135	mA	*1, *5
			High-speed CR RUN mode	CPU/ Peripheral: 4 MHz[2], Flash 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	6	57.8	mA	*1
			Sub RUN mode	CPU/ Peripheral: 32 kHz, Flash 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	1.3	51.7	mA	*1, *6
			Low-speed CR RUN mode	CPU/ Peripheral: 100 kHz, Flash 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	1.3	51.7	mA	*1
SLEEP mode current	Iccs		PLL SLEEP mode	Peripheral: 72 MHz	30	89	mA	*1, *5
			High-speed CR SLEEP mode	Peripheral: 4 MHz[2]	4.5	55.9	mA	*1
			Sub SLEEP mode	Peripheral: 32 kHz	1.2	51.6	mA	*1, *6
			Low-speed CR SLEEP mode	Peripheral: 100 kHz	1.2	51.6	mA	*1

*1: When all ports are fixed, Ethernet is stopped.

*2: When setting it to 4 MHz by trimming.

*3: T_A = +25°C, V_{CC} = 5.5 V

*4: T_A = +85°C, V_{CC} = 5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

(Vcc = AVcc = USBVcc0 = USBVcc1 = ETHVcc = 2.7 V to 5.5 V, Vss = AVss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	T_A = + 25°C, When LVD is off	4	10	mA	*1, *3
				T_A = + 85°C, When LVD is off	-	55	mA	*1, *3
			Sub TIMER mode	T_A = + 25°C, When LVD is off	1.1	5	mA	*1, *4
				T_A = + 85°C, When LVD is off	-	50	mA	*1, *4
STOP mode current	I_{CCH}		STOP mode	T_A = + 25°C, When LVD is off	1	5	mA	*1
				T_A = + 85°C, When LVD is off	-	50	mA	*1

*1: When all ports are fixed.

*2: V_{CC} = 5.5 V

*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	12	14	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1 unit operation	0.57	0.72	mA	
			At stop	0.06	35	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.96	mA	
			At stop	0.06	4	µA	

12.3.2 Pin Characteristics

(Vcc = USBVcc0 = USBVcc1 = ETHVcc = AVcc = 2.7 V to 5.5 V, Vss = AVss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	Vcc (ETHVcc) × 0.8	-	Vcc (ETHVcc) + 0.3	V	*1
		5V tolerant input pin	-	Vcc × 0.8	-	Vss + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	ETHVcc + 0.3	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	Vss - 0.3	-	Vcc (ETHVcc) × 0.2	V	*1
		5V tolerant input pin	-	Vss - 0.3	-	Vcc × 0.2	V	
		TTL Schmitt input pin	-	Vss - 0.3	-	0.8	V	
"H" level output voltage	V_{OH}	4 mA type	Vcc (ETHVcc) ≥ 4.5 V, I_{OH} = - 4 mA	Vcc (ETHVcc) - 0.5	-	Vcc (ETHVcc)	V	*1
			Vcc (ETHVcc) < 4.5 V, I_{OH} = - 2 mA					
		8 mA type	ETHVcc ≥ 4.5 V, I_{OH} = - 8 mA	ETHVcc - 0.5	-	ETHVcc	V	*1
			ETHVcc < 4.5 V, I_{OH} = - 4 mA					
		12 mA type	Vcc ≥ 4.5 V, I_{OH} = - 12 mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V, I_{OH} = - 8 mA					
		P80, P81, P82, P83	USBVcc ≥ 4.5 V, I_{OH} = - 20.5 mA	USBVcc - 0.4	-	USBVcc	V	*2
			USBVcc < 4.5 V, I_{OH} = - 13.0 mA					

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL}	4 mA type	Vcc (ETHVcc) ≥ 4.5 V, I_{OL} = 4 mA	Vss	-	0.4	V	*1
			Vcc (ETHVcc) < 4.5 V, I_{OL} = 2 mA					
		8 mA type	ETHVcc ≥ 4.5 V, I_{OL} = 8 mA	Vss	-	0.4	V	*1
			ETHVcc < 4.5 V, I_{OL} = 4 mA					
		12 mA type	Vcc ≥ 4.5 V, I_{OL} = 12 mA	Vss	-	0.4	V	
			Vcc < 4.5 V, I_{OL} = 8 mA					
		P80, P81, P82, P83	USBVcc ≥ 4.5 V, I_{OL} = 18.5 mA	Vss	-	0.4	V	*2
			USBVcc < 4.5 V, I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	Vcc ≥ 4.5 V	25	50	100	kΩ	
			Vcc < 4.5 V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

*1: The power supply type varies depending on the pin position.
For example, power supply A (power supply B) shows that either of power supply A or power supply B becomes a power supply voltage.

*2: USBVcc0 and USBVcc1 are described as USBVcc.

12.4 AC Characteristics

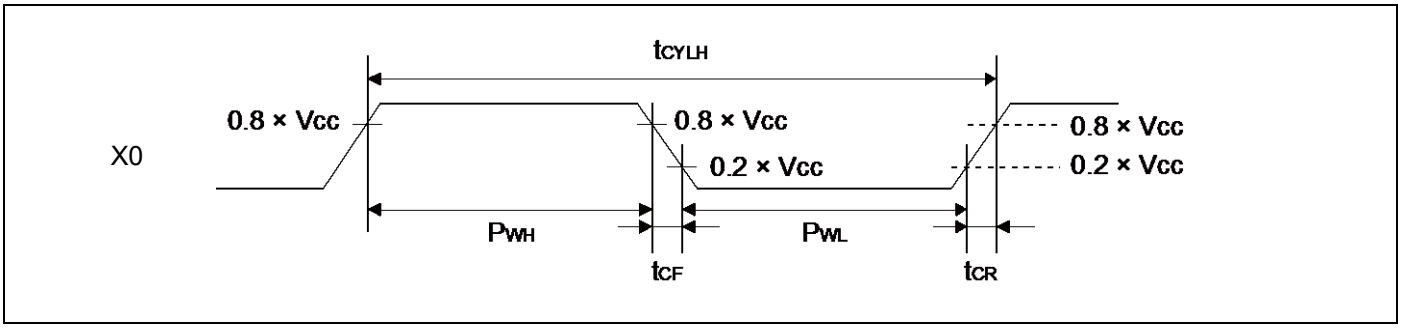
12.4.1 Main Clock Input Characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	Vcc ≥ 4.5 V	4	50	MHz	When crystal oscillator is connected
			Vcc < 4.5 V	4	20		
			Vcc ≥ 4.5 V	4	50	MHz	When using external clock
			Vcc < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		Vcc ≥ 4.5 V	20	250	ns	When using external clock
			Vcc < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating Clock[1] frequency	F_{CM}	-	-	-	144	MHz	Master clock
	F_{CC}	-	-	-	144	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	72	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	72	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	72	MHz	APB2 bus clock*2
Internal operating Clock*1 cycle time	t_{CYCC}	-	-	6.94	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	13.8	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	13.8	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	13.8	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

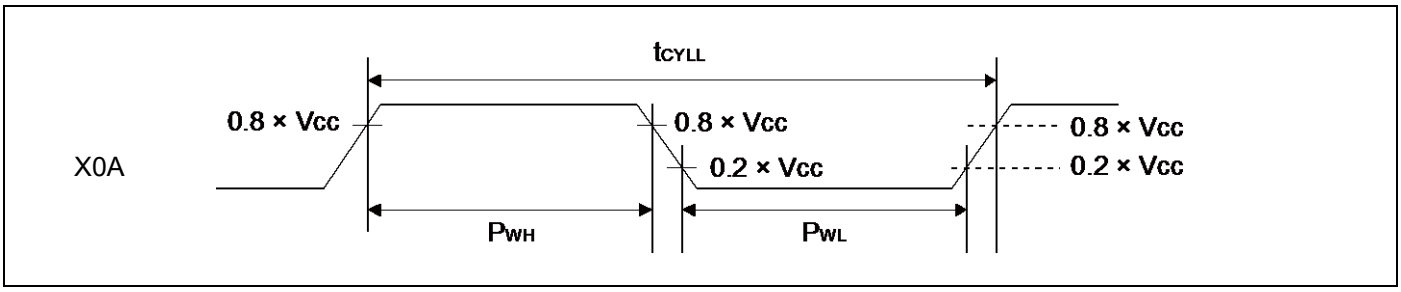
*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this datasheet.



12.4.2 Sub Clock Input Characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		PWH/tCYLL, PWL/tCYLL	45	-	55	%	When using external clock



12.4.3 Internal CR Oscillation Characteristics

High-speed internal CR

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	T_A = + 25°C	3.96	4	4.04	MHz	When trimming*1
		T_A = 0°C to + 70°C	3.84	4	4.16		
		T_A = - 40°C to + 85°C	3.8	4	4.2		
		T_A = - 40°C to + 85°C	3	4	5		When not trimming
Frequency stability time	t_{CRWT}	-	-	-	90	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Low-speed internal CR

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main and USB/Ethernet PLL (In the case of using main clock for input of PLL)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	200	-	300	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	144	MHz	
USB/Ethernet clock frequency*3	$F_{CLKSPLL}$	-	-	50	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

*3: For more information about USB/Ethernet clock, see "Chapter 2-3: USB/Ethernet Clock Generation" in "FM3 Family Peripheral Manual Communication Macro Part".

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed internal CR)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	190	-	300	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	144	MHz	

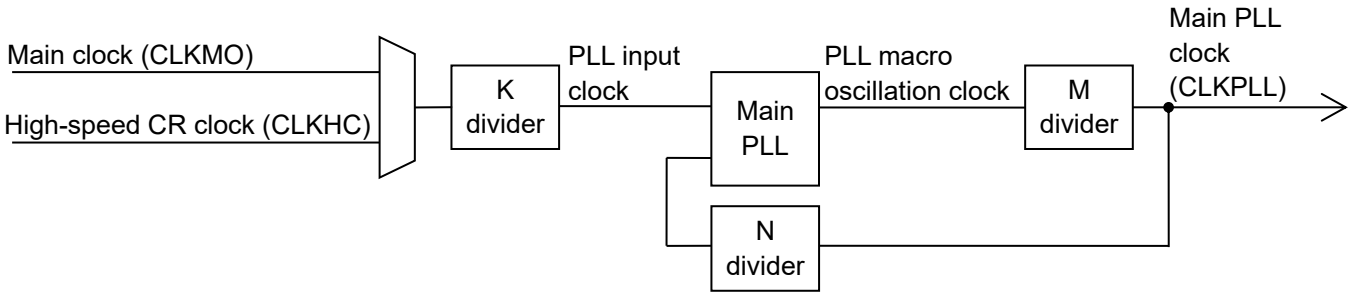
*1: Time from when the PLL starts operating until the oscillation stabilizes.

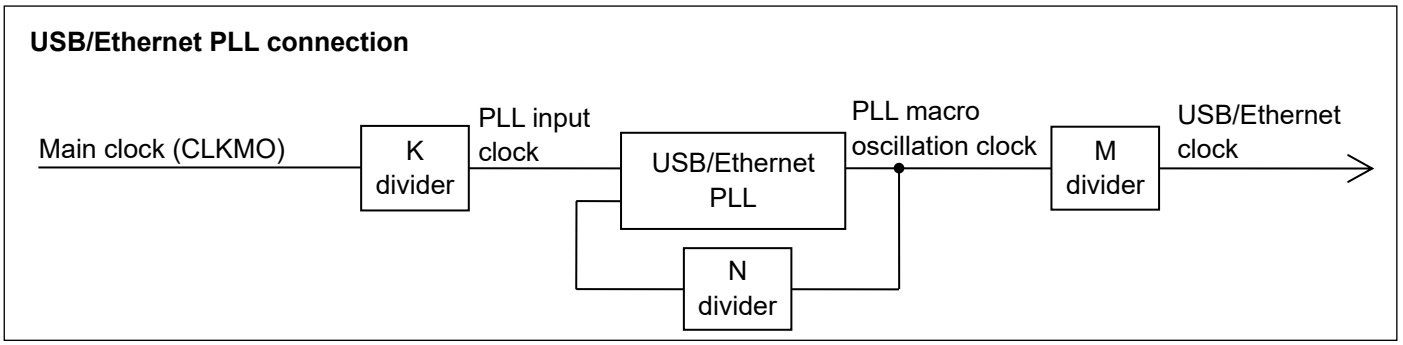
*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

Note:

− *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.*

Main PLL connection





12.4.6 Reset Input Characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(Vss = 0 V, T_A = - 40°C to + 85°C)

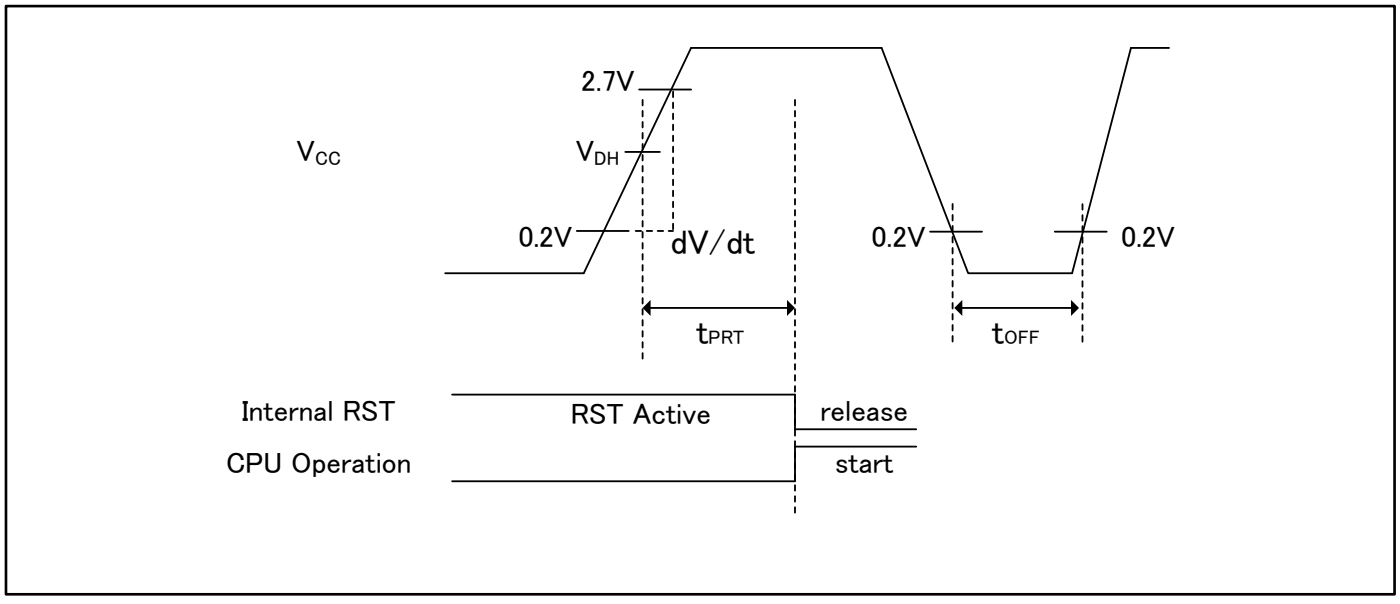
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	50	-	-	ms	*1
Power ramp rate	dV/dt		Vcc:0.2 V to 2.70 V	0.9	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.46	-	0.76	ms	

*1: VCC must be held below 0.2V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>50ms).

Note:

– *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 6.*



Glossary:

VDH: detection voltage of Low Voltage detection reset. See “12.7. Low-Voltage Detection Characteristics”

12.4.8 External Bus Timing

External bus clock output characteristics

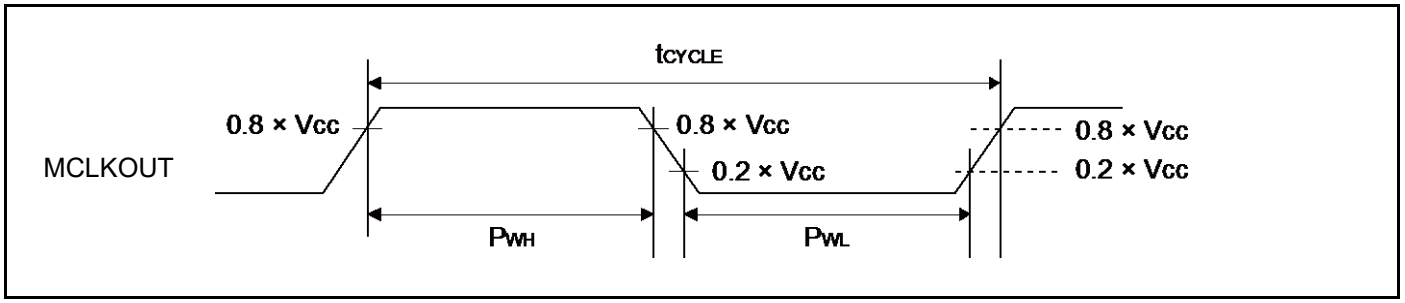
(Vcc = 2.7 V to 5.5V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	Vcc ≥ 4.5 V	-	50*2	MHz
			Vcc < 4.5 V	-	32*3	MHz

*1: External bus clock (MCLKOUT) is divided clock of HCLK.
For more information about setting of clock divider, see "Chapter 12: External Bus Interface" in "FM3 Family Peripheral Manual".
When external bus clock is not output, this characteristic does not give any effect on external bus operation.

*2: When AHB bus clock frequency is more than 100 MHz, the divider setting for MCLKOUT must be more than 4.

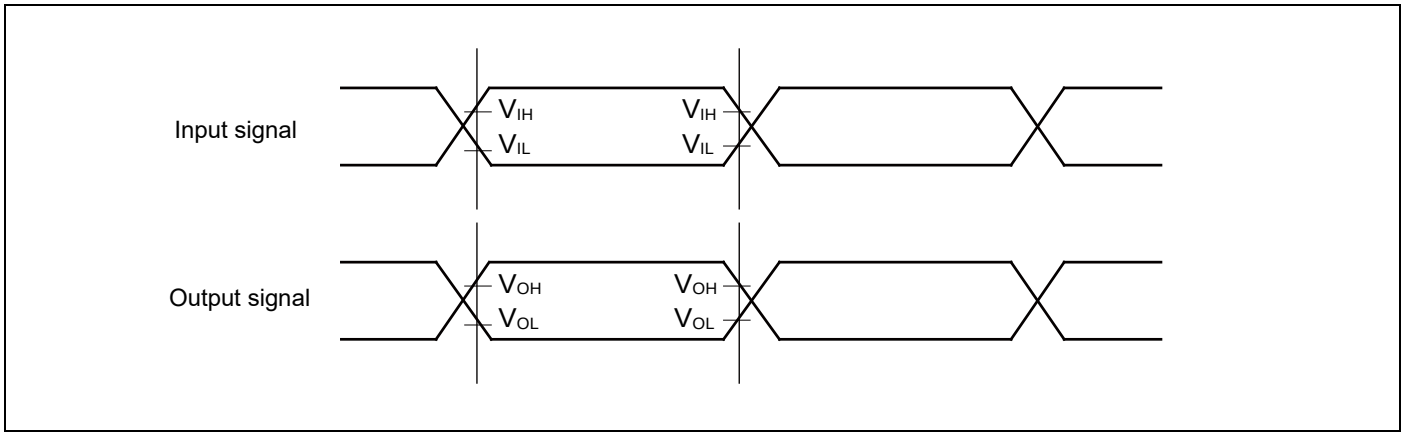
*3: When AHB bus clock frequency is more than 64 MHz, the divider setting for MCLKOUT must be more than 4.



External bus signal input/output characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



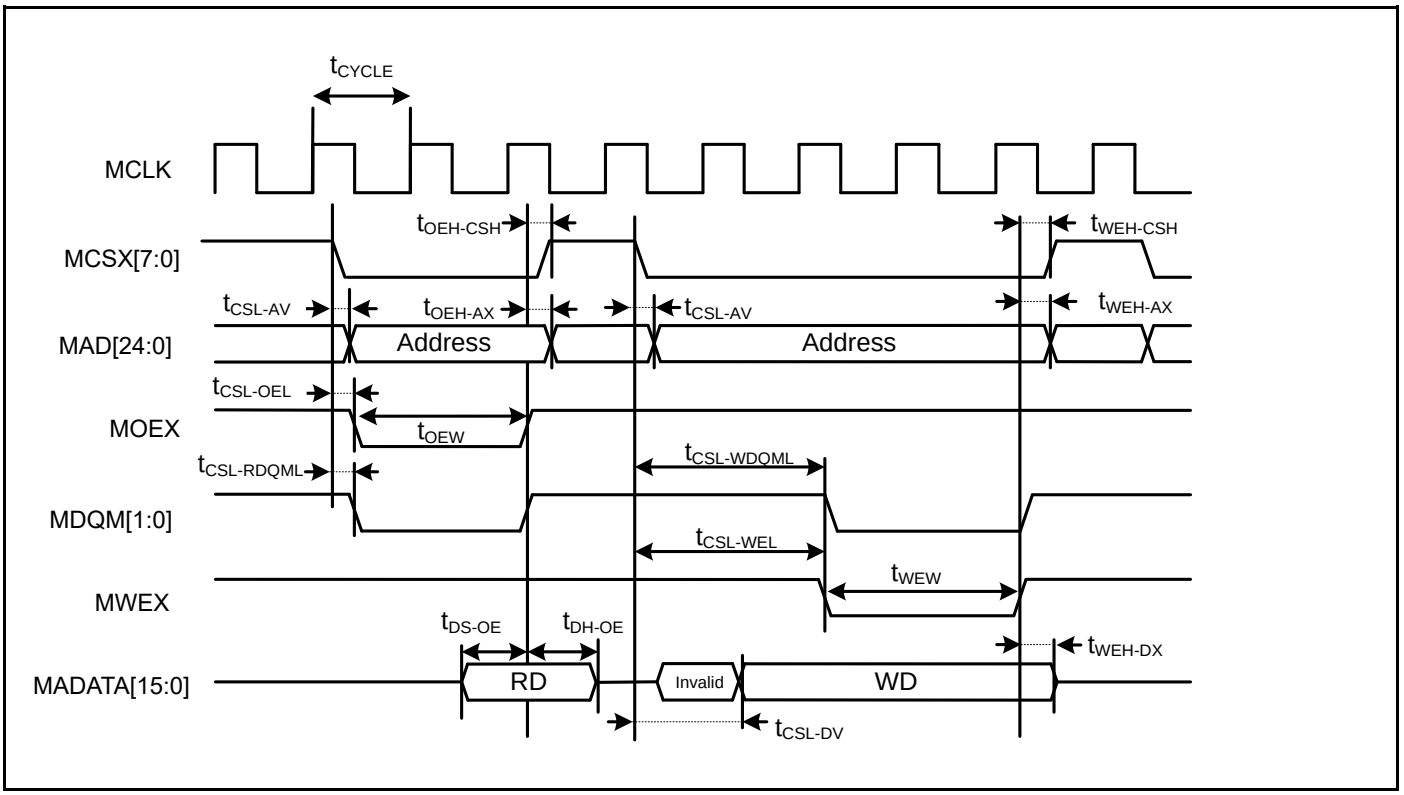
Separate bus access asynchronous SRAM mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MCSX ↓ → Address output delay time	$t_{CSL - AV}$	MCSX[7:0], MAD[24:0]	Vcc ≥ 4.5 V	-9	+9	ns
			Vcc < 4.5 V	-12	+12	
MOEX ↑ → Address hold time	$t_{OEH - AX}$	MOEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL - OEL}$	MOEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH - CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL - RDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	$t_{DS - OE}$	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	20	-	ns
			Vcc < 4.5 V	38	-	
MOEX ↑ → Data hold time	$t_{DH - OE}$	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX Min pulse width	t_{WEW}	MWEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MWEX ↑ → Address output delay time	$t_{WEH - AX}$	MWEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL - WEL}$	MWEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH - CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MCSX ↓ → Data output time	$t_{CSL - DV}$	MCSX, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK-9	MCLK+9	ns
			Vcc < 4.5 V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	$t_{WEH - DX}$	MWEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	

Note:

- *When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)*


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

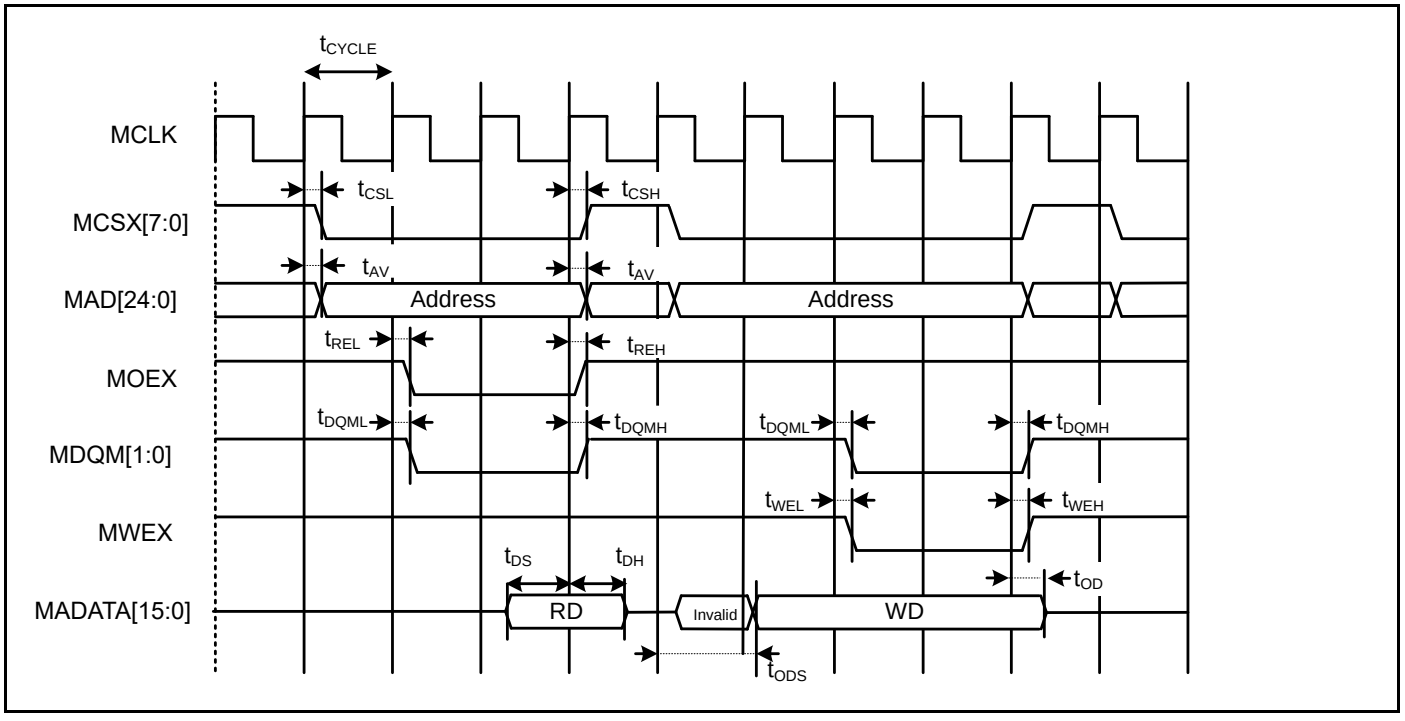
Separate bus access synchronous SRAM mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{CSH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{REH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	19	-	ns
			Vcc < 4.5 V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX delay time	t_{WEL}	MCLK, MWEX	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{WEH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{DQMH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCLK ↑ → Data output time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK+1	MCLK+18	ns
			Vcc < 4.5 V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	1	18	ns
			Vcc < 4.5 V		24	

Note:

– *When the external load capacitance = 30 pF.*



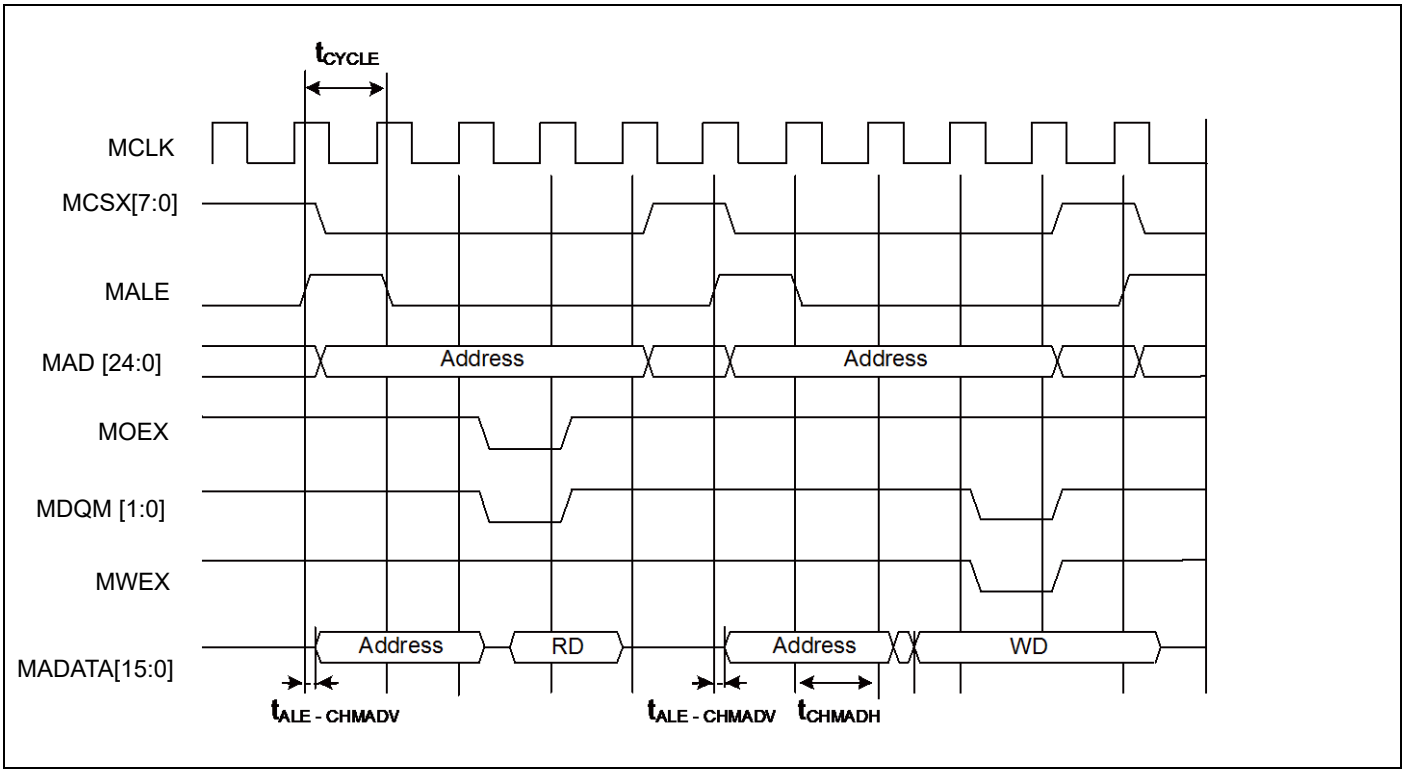
Multiplexed bus access asynchronous SRAM mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	Vcc ≥ 4.5 V	0	10	ns
			Vcc < 4.5 V		20	
Multiplexed address hold time	t_{CHMADH}		Vcc ≥ 4.5 V	MCLK×n+0	MCLK×n+10	ns
			Vcc < 4.5 V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)*



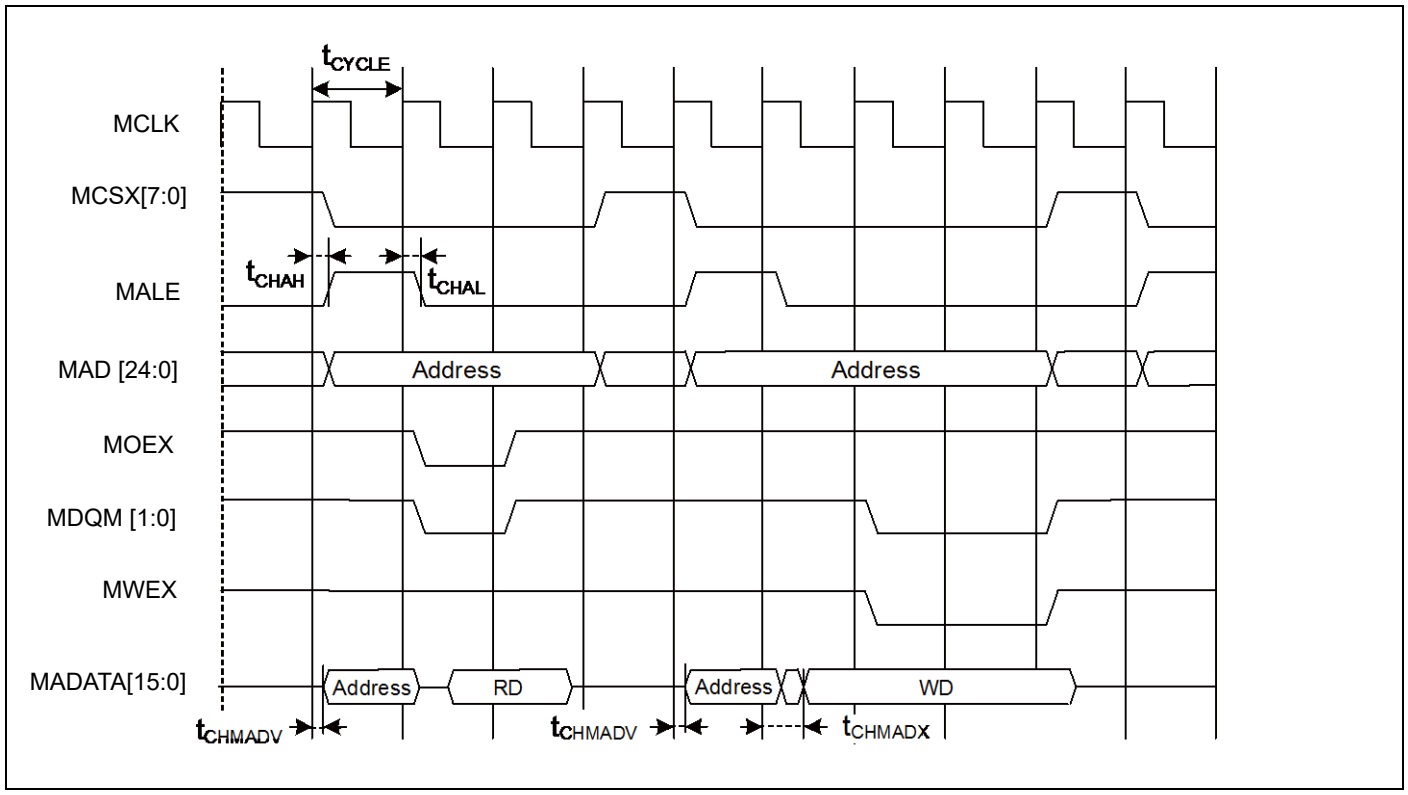
Multiplexed bus access synchronous SRAM mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	Vcc ≥ 4.5 V	1	9	ns	
			Vcc < 4.5 V		12	ns	
	t_{CHAH}		Vcc ≥ 4.5 V	1	9	ns	
			Vcc < 4.5 V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	1	t_{OD}	ns	
			Vcc < 4.5 V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		Vcc ≥ 4.5 V	1	t_{OD}	ns	
			Vcc < 4.5 V				

Note:

- *When the external load capacitance = 30 pF.*



NAND flash mode

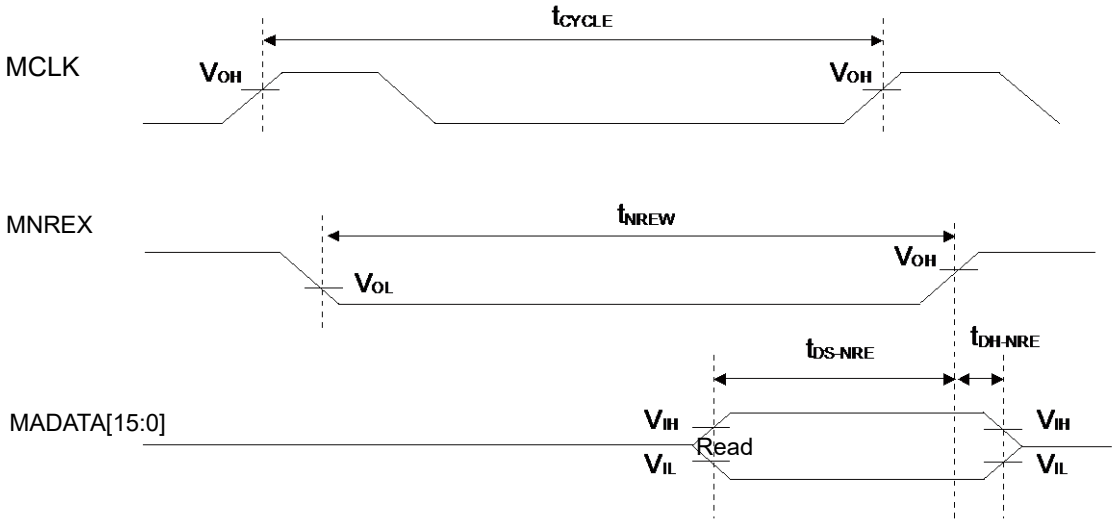
(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
Data setup → MNREX↑time	$t_{DS - NRE}$	MNREX, MADATA[15:0]	Vcc ≥ 4.5 V	20	-	ns
			Vcc < 4.5 V	38	-	
MNREX↑→ Data hold time	$t_{DH - NRE}$	MNREX, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MNALE↑→ MNWEX delay time	$t_{ALEH - NWEL}$	MNALE, MNWEX	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MNALE↓→ MNWEX delay time	$t_{ALEL - NWEL}$	MNALE, MNWEX	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MNCLE↑→ MNWEX delay time	$t_{CLEH - NWEL}$	MNCLE, MNWEX	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MNWEX↑→ MNCLE delay time	$t_{NWEH - CLEL}$	MNCLE, MNWEX	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MNWEX↓→ Data output time	$t_{NWEL - DV}$	MNWEX, MADATA[15:0]	Vcc ≥ 4.5 V	-9	+9	ns
			Vcc < 4.5 V	-12	+12	
MNWEX↑→ Data hold time	$t_{NWEH - DX}$	MNWEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	

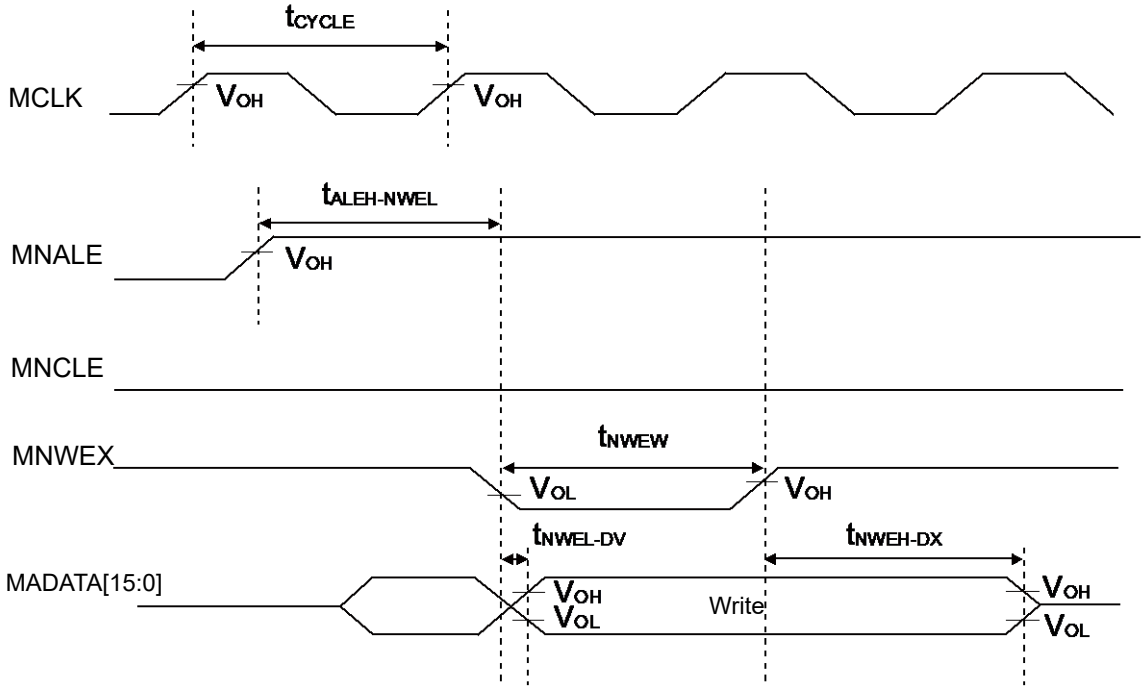
Note:

- *When the external load capacitance = 30 pF. (m=0 to 15, n=1 to 16)*

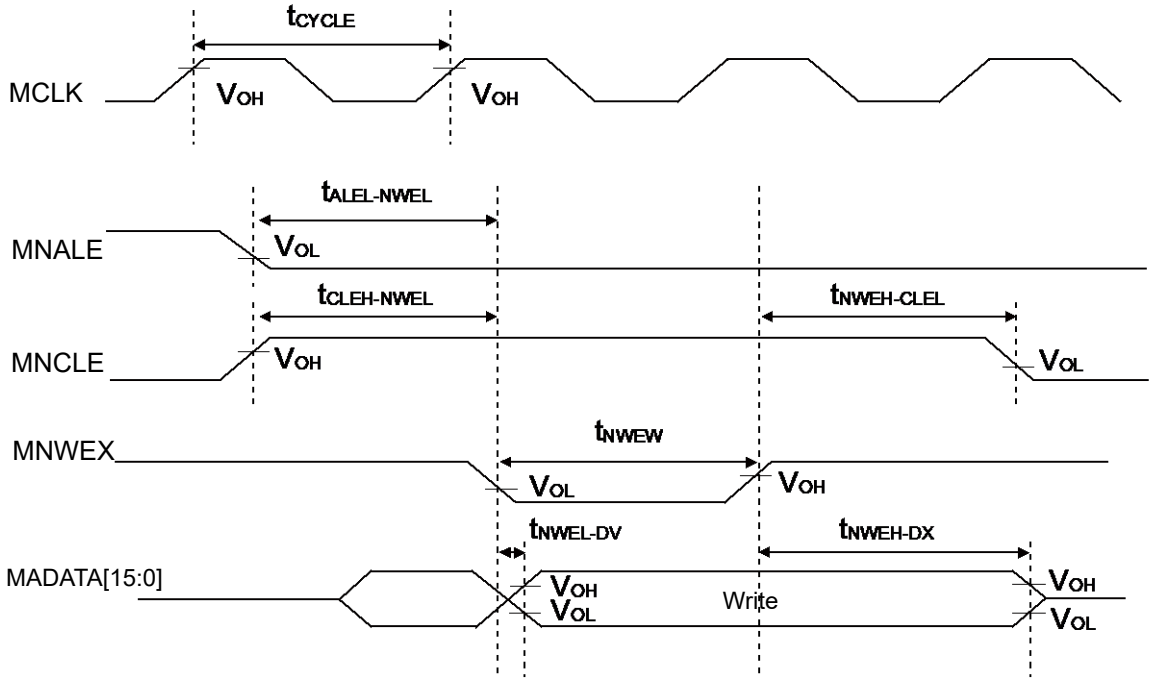
NAND Flash Read



NAND Flash Address Write



NAND Flash Command Write

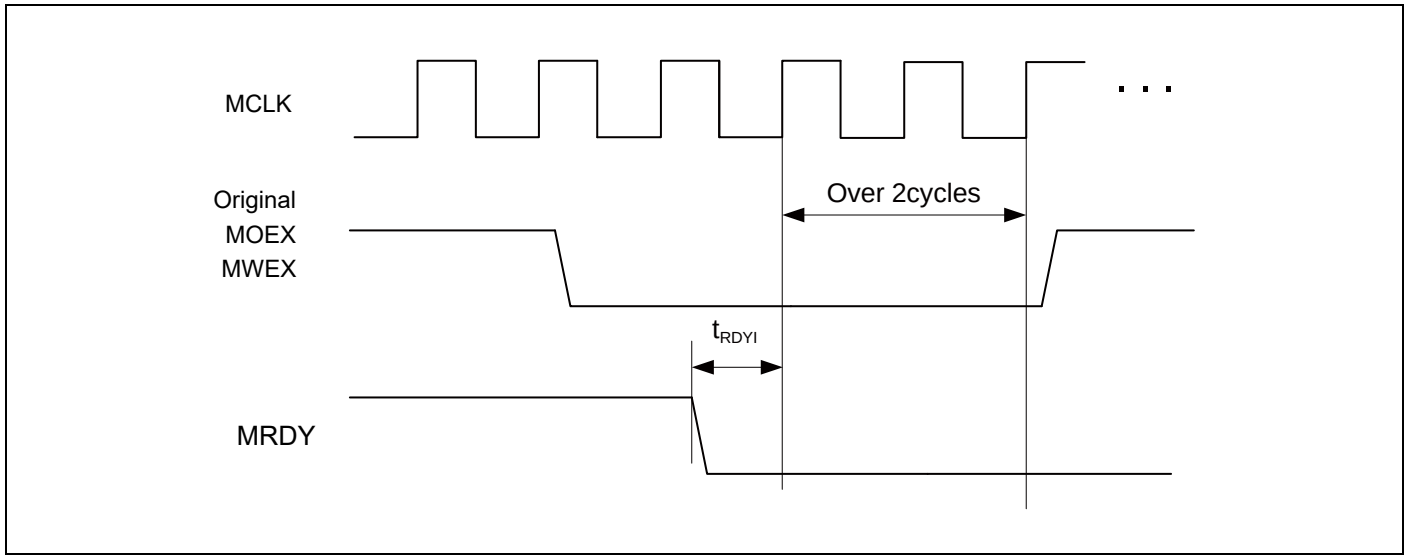


External ready input timing

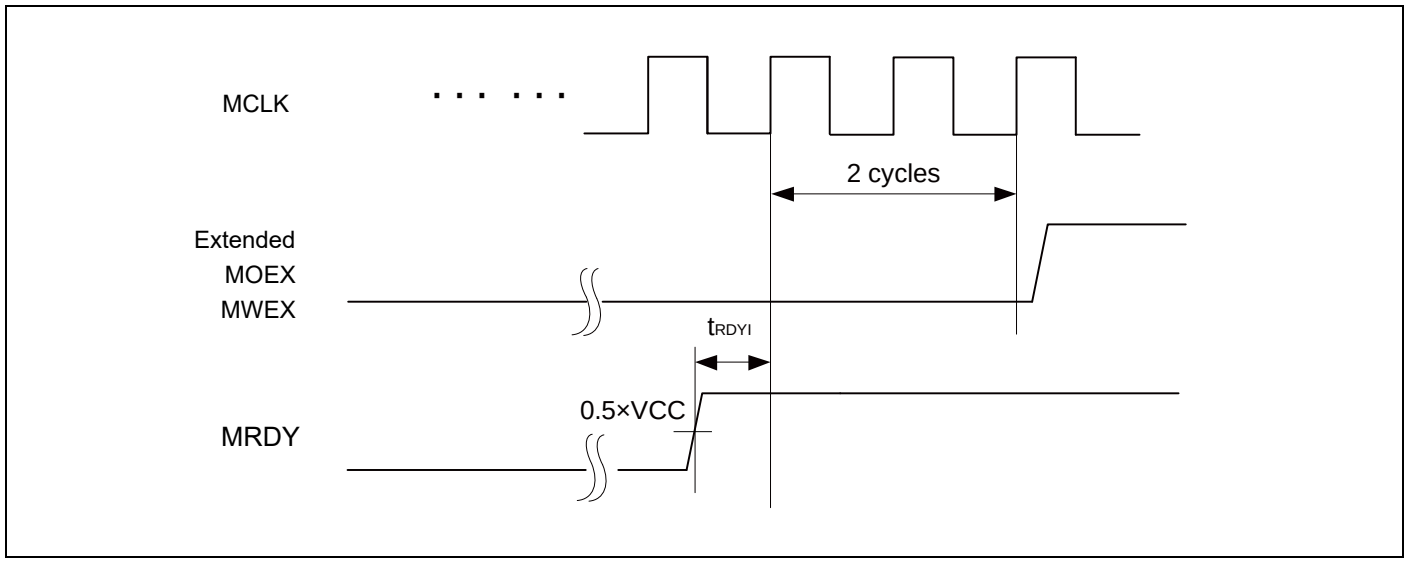
(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	Vcc ≥ 4.5 V	19	-	ns	
			Vcc < 4.5 V	37			

When RDY is input



When RDY is released

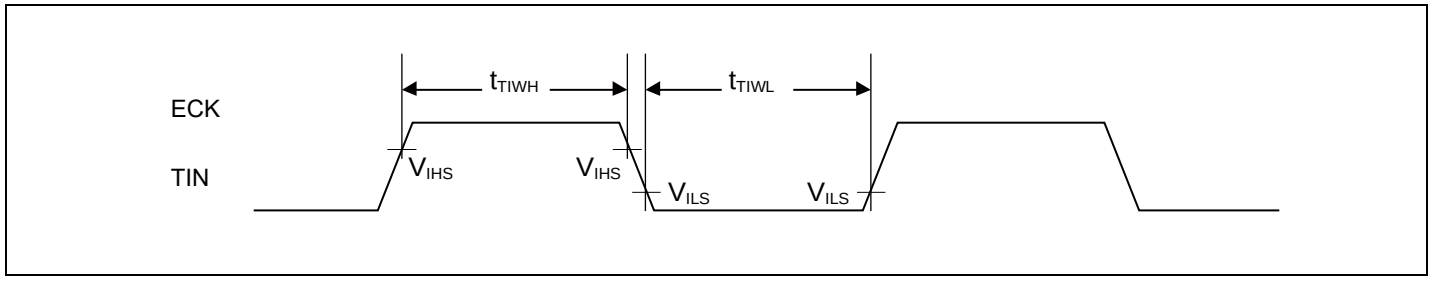


12.4.9 Base Timer Input Timing

Timer input timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

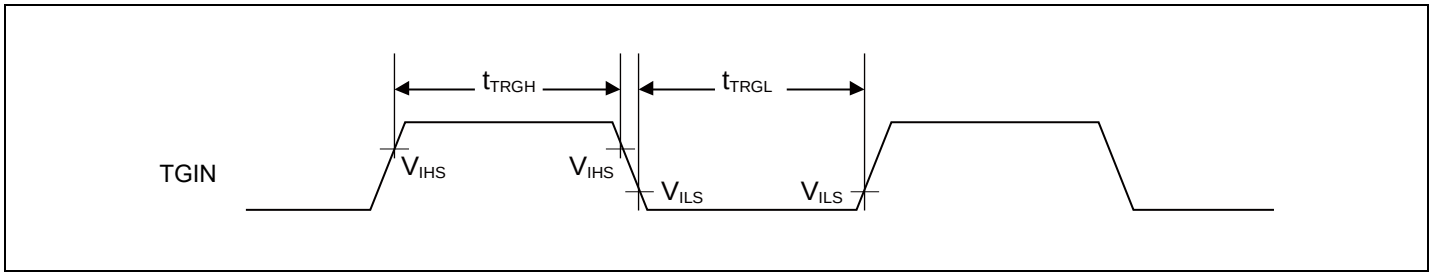
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Base Timer is connected to, see "8. Block Diagram" in this datasheet.*

12.4.10 CSIO/UART Timing

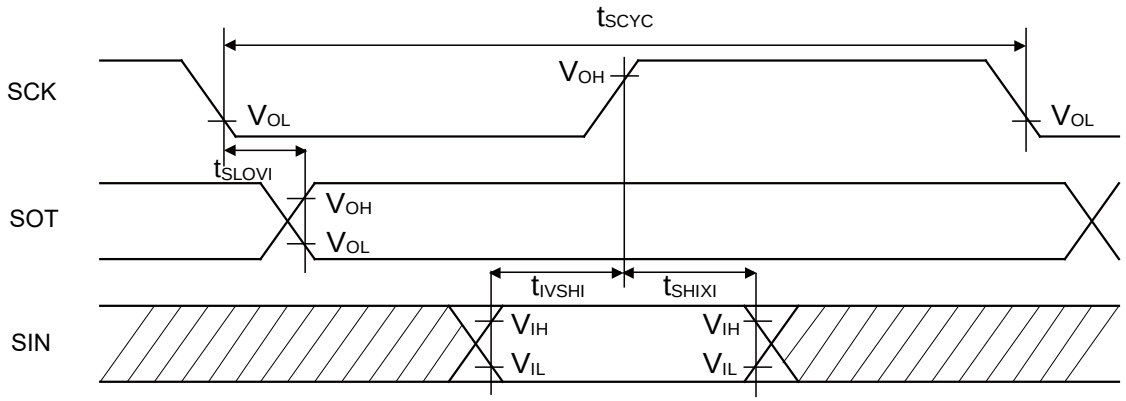
CSIO (SPI = 0, SCINV = 0)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

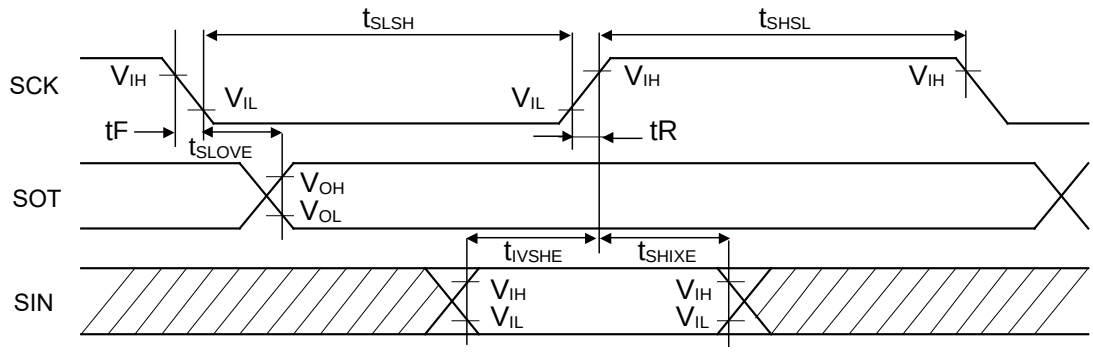
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

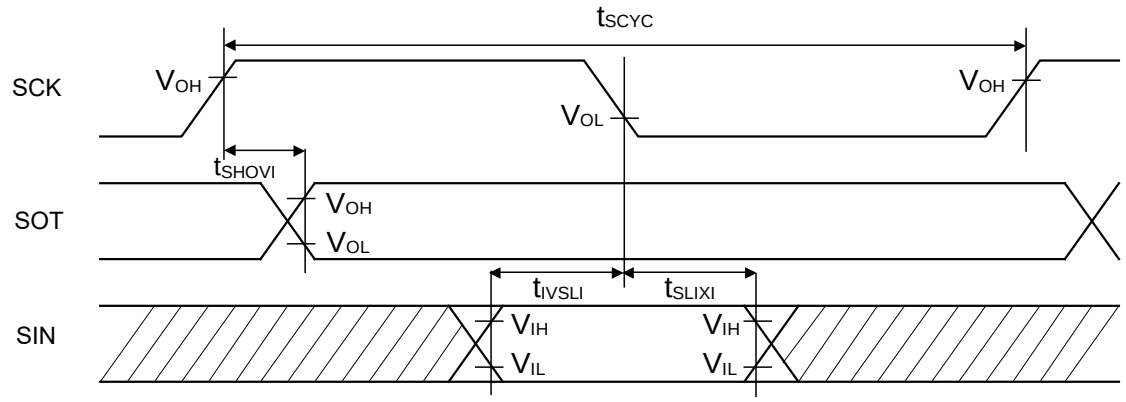
CSIO (SPI = 0, SCINV = 1)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

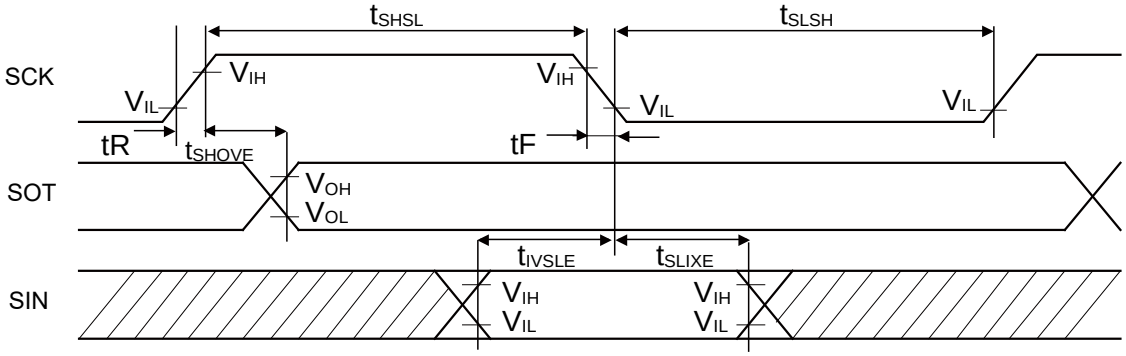
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

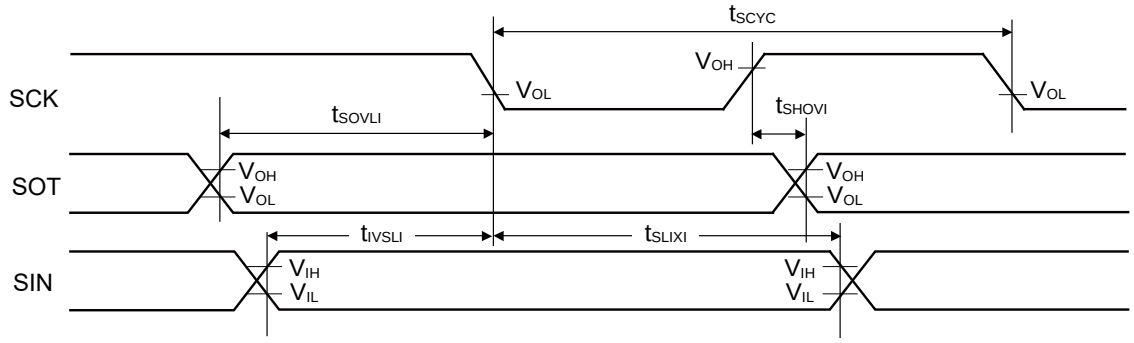
CSIO (SPI = 1, SCINV = 0)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

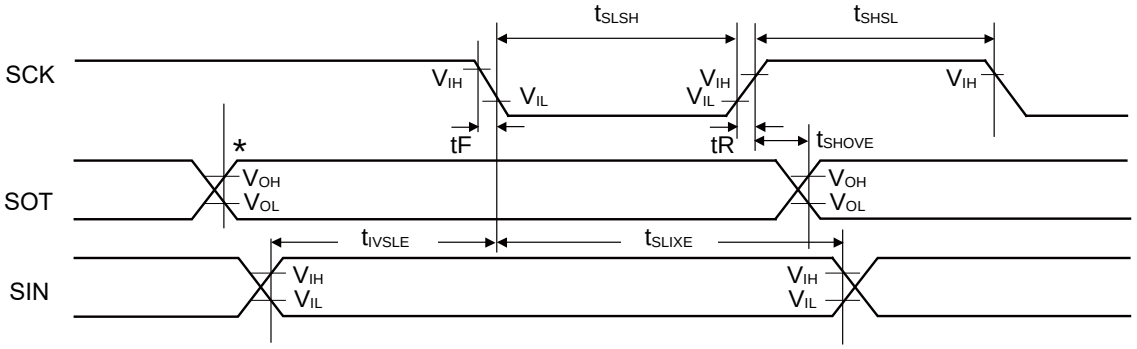
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

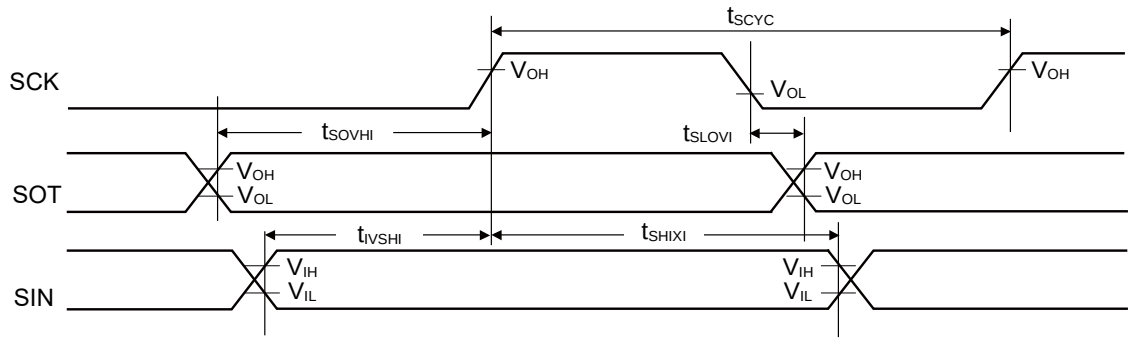
CSIO (SPI = 1, SCINV = 1)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

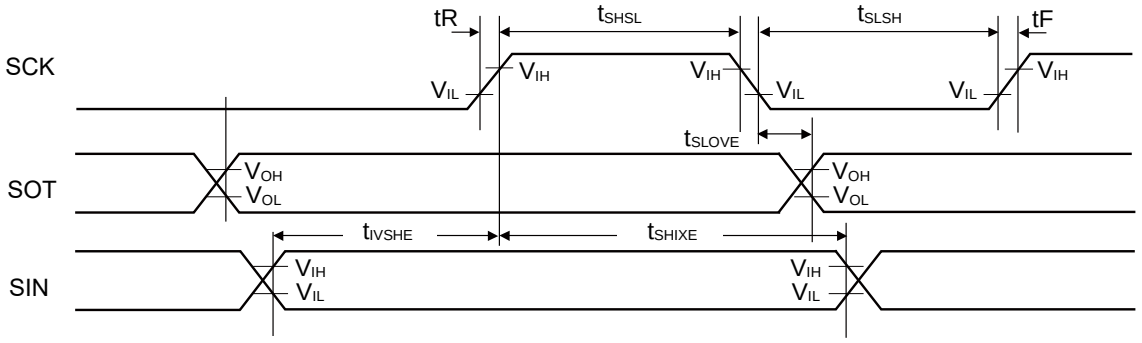
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode

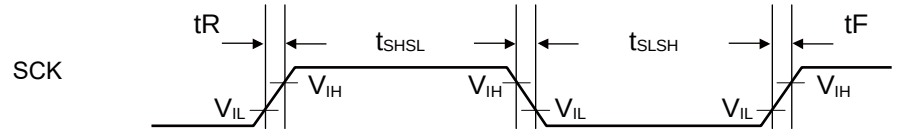


Slave mode

UART external clock input (EXT = 1)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	tF		-	5	ns	
SCK rise time	tR		-	5	ns	

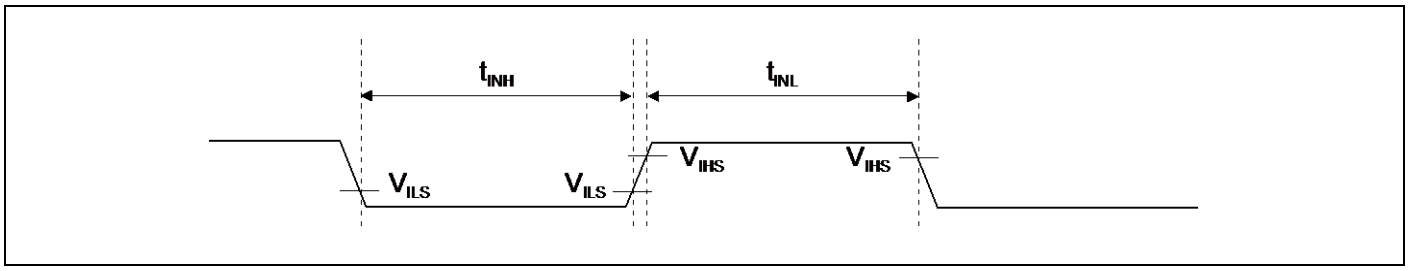


12.4.11 External Input Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$ *1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$ *1	-	ns	Wave form generator
		INTxx, NMIX	Except Timer mode, Stop mode	$2t_{CYCP}$ + 100*1	-	ns	External interrupt NMI
			Timer mode, Stop mode	500	-	ns	

*1: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "8. Block Diagram" in this datasheet.

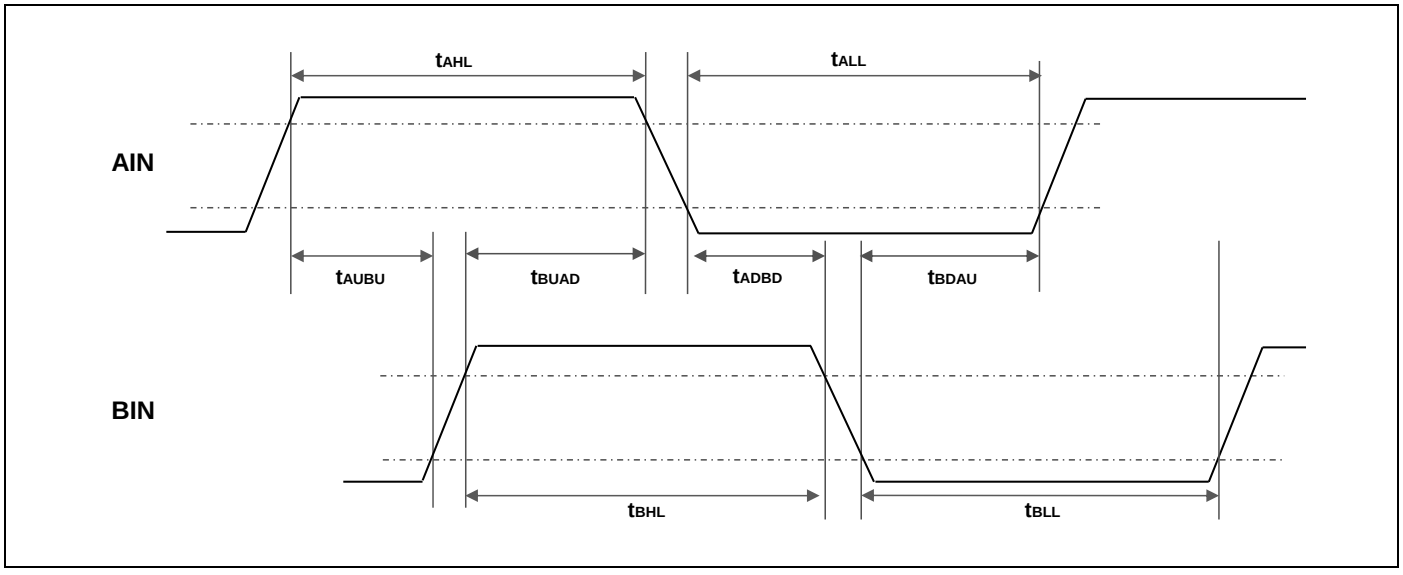


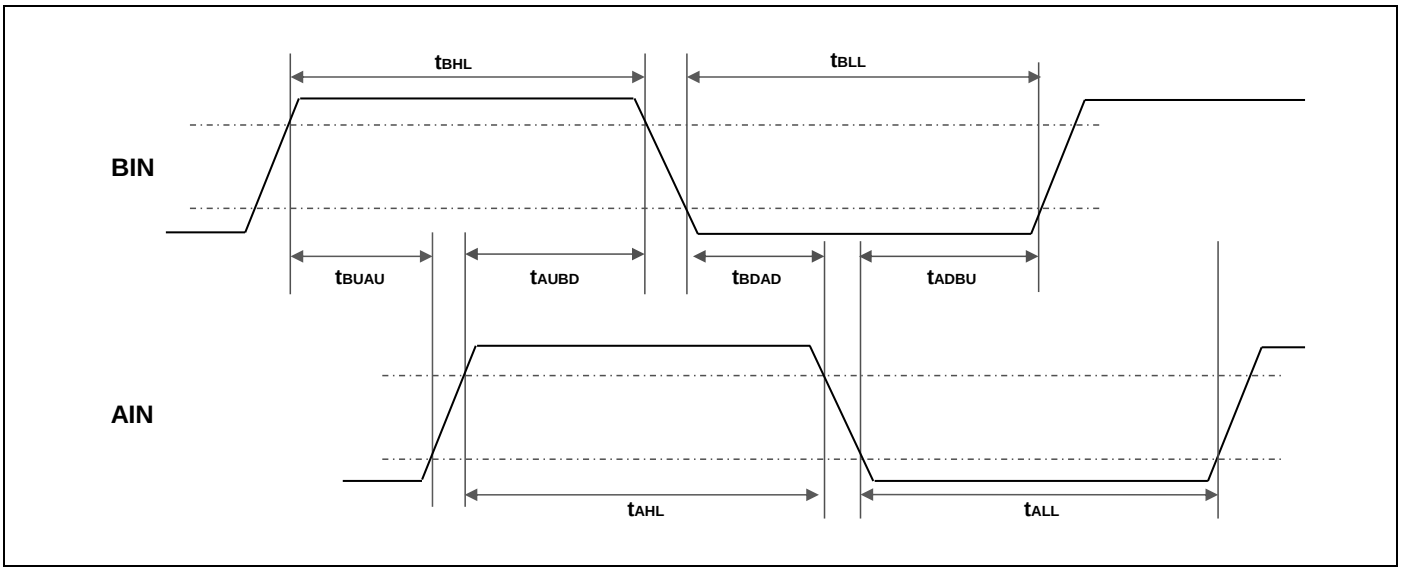
12.4.12 Quadrature Position/Revolution Counter timing

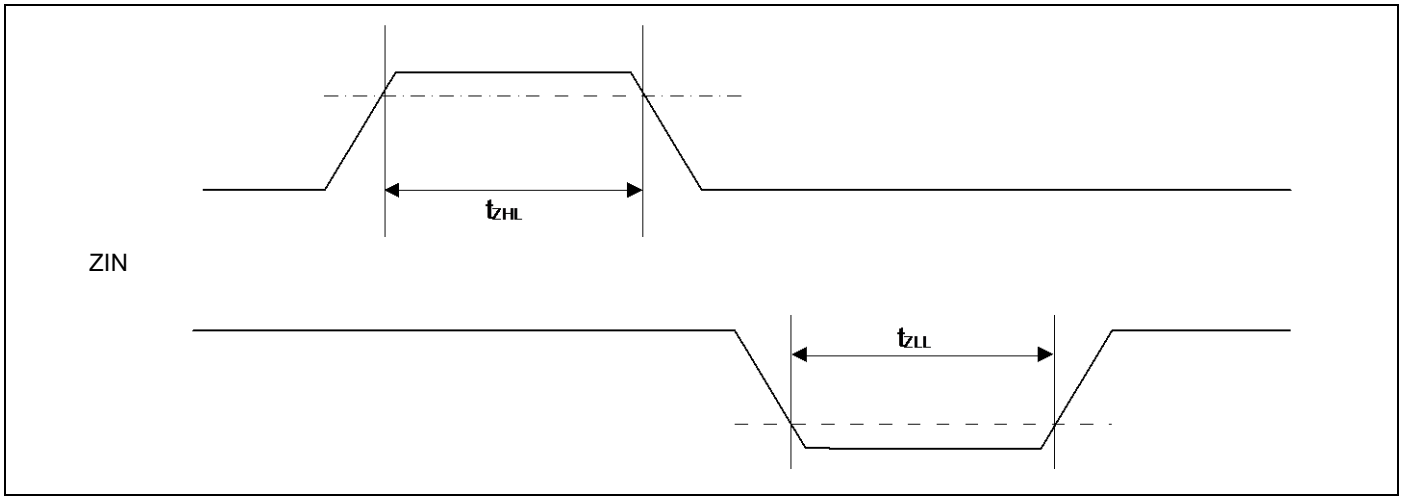
(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

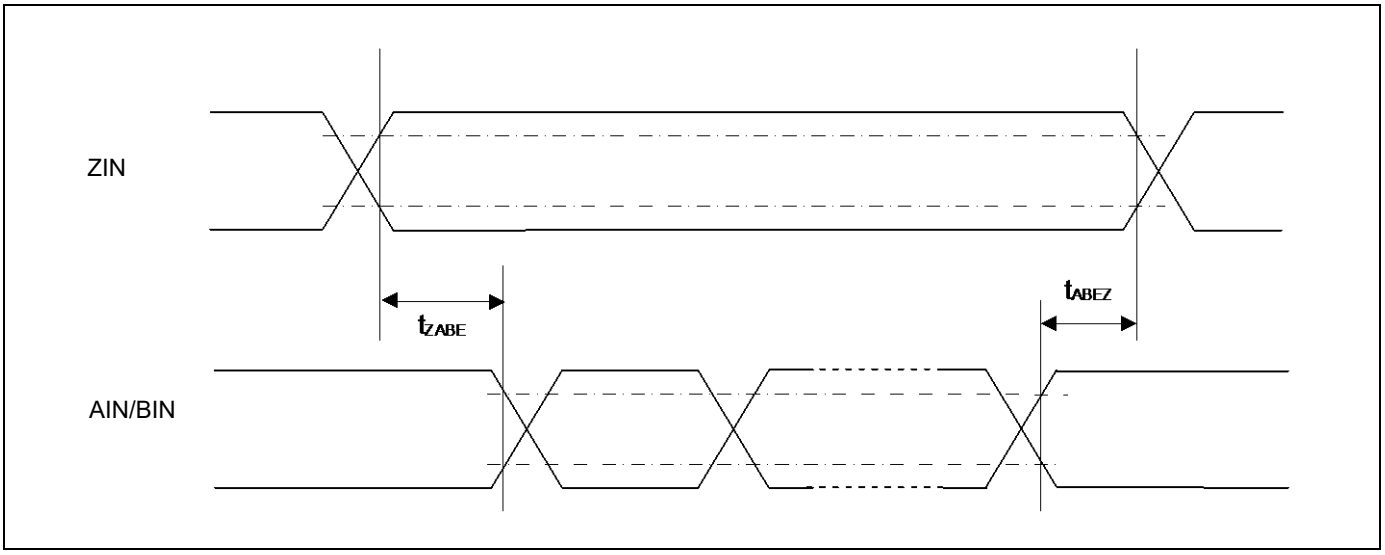
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$*1	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC="0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC="1"			

*1: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.13 I²C Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	8 MHz ≤ t_{CYCP} ≤ 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz < t_{CYCP} ≤ 60 MHz	3 t_{CYCP}*4	-	3 t_{CYCP}*4	-	ns	*5
		60 MHz < t_{CYCP} ≤ 72 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	*5

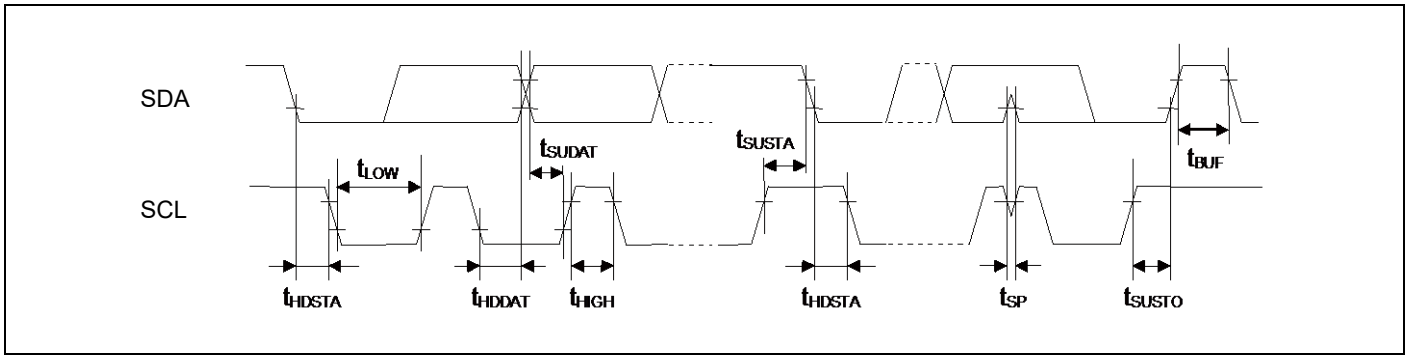
*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns"

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number which I²C is connected to, see "8. Block Diagram" in this datasheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.

*5: The number of steps of the noise filter can be changed with register settings.
Change the number of the noise filter steps according to APB2 bus clock frequency.



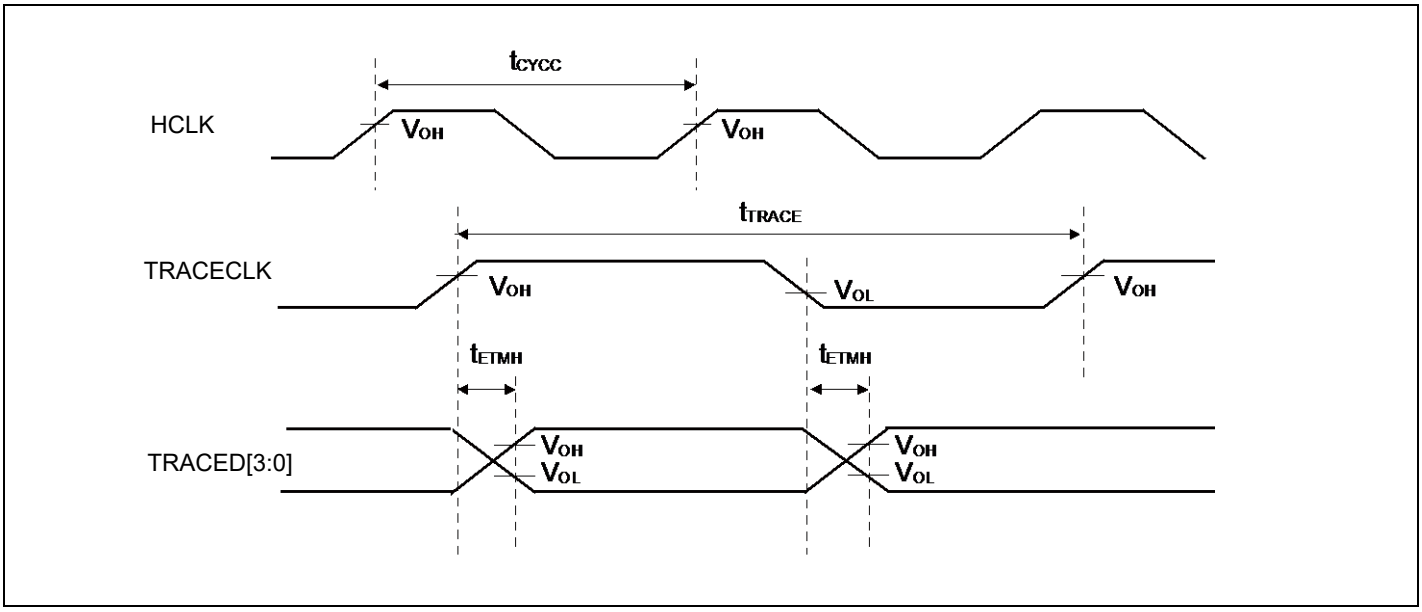
12.4.14 ETM Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	Vcc ≥ 4.5 V	2	9	ns	
			Vcc < 4.5 V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	Vcc ≥ 4.5 V	-	50	MHz	
			Vcc < 4.5 V	-	32	MHz	
TRACECLK cycle time	t_{TRACE}		Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	31.25	-	ns	

Note:

- *When the external load capacitance = 30 pF.*



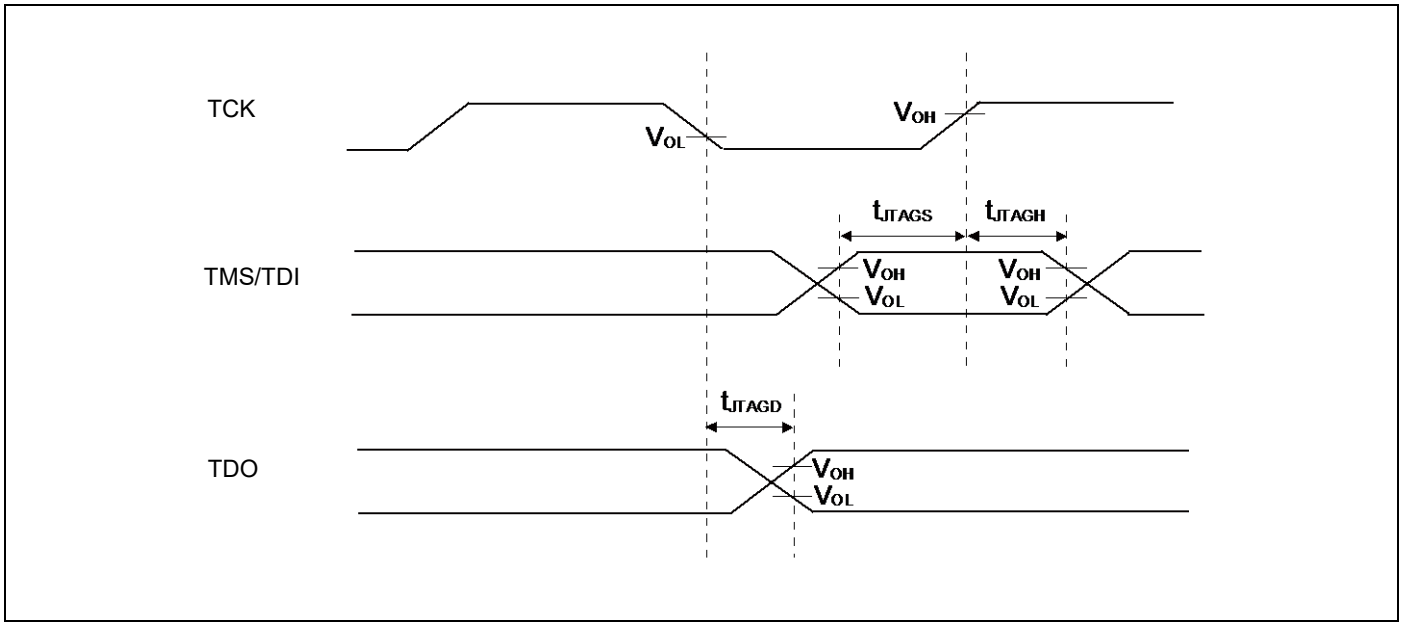
12.4.15 JTAG Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TDO delay time	t_{JTAGD}	TCK, TDO	Vcc ≥ 4.5 V	-	25	ns	
			Vcc < 4.5 V	-	45		

Note:

- *When the external load capacitance = 30 pF.*



12.4.16 Ethernet-MAC Timing

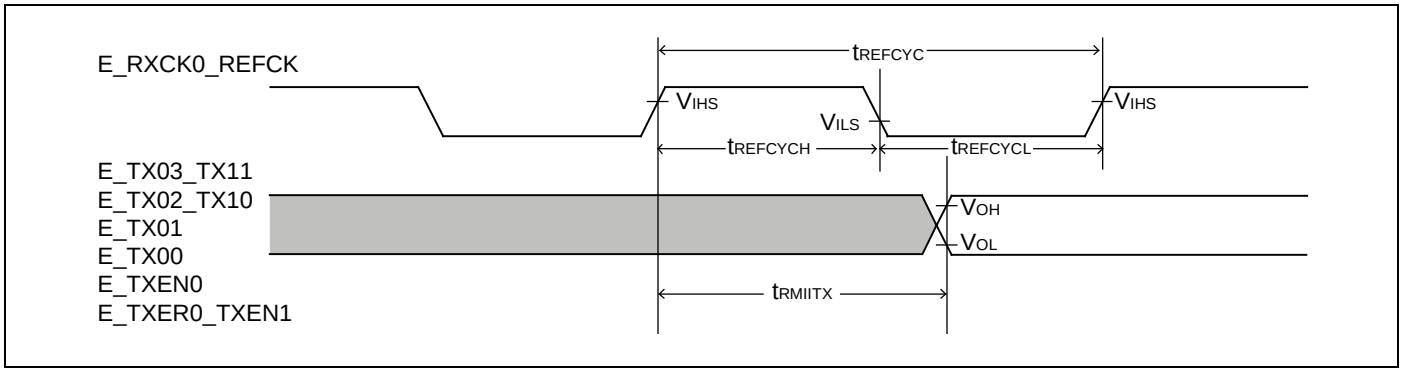
RMII transmission (100 Mbps/10 Mbps)

(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V [*1])
(Vss = 0 V, T_A = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Reference Clock Cycle time[*2]	t_{REFCYC}	E_RXCK0_REFCK	20 ns (typical)	-	-	ns
Reference Clock High pulse width duty	$t_{REFCYCH}$	E_RXCK0_REFCK	$t_{REFCYCH}$ / t_{REFCYC}	35	65	%
Reference Clock Low pulse width duty	$t_{REFCYCL}$	E_RXCK0_REFCK	$t_{REFCYCL}$ / t_{REFCYC}	35	65	%
REFCK ↑ → Transmitted data Delay time (ch.0)	t_{RMIITX}	E_TX01, E_TX00, E_TXEN0	-	-	12	ns
REFCK ↑ → Transmitted data Delay time (ch.1)		E_TX03_TX11, E_TX02_TX10, E_TXER0_TXEN1				

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.



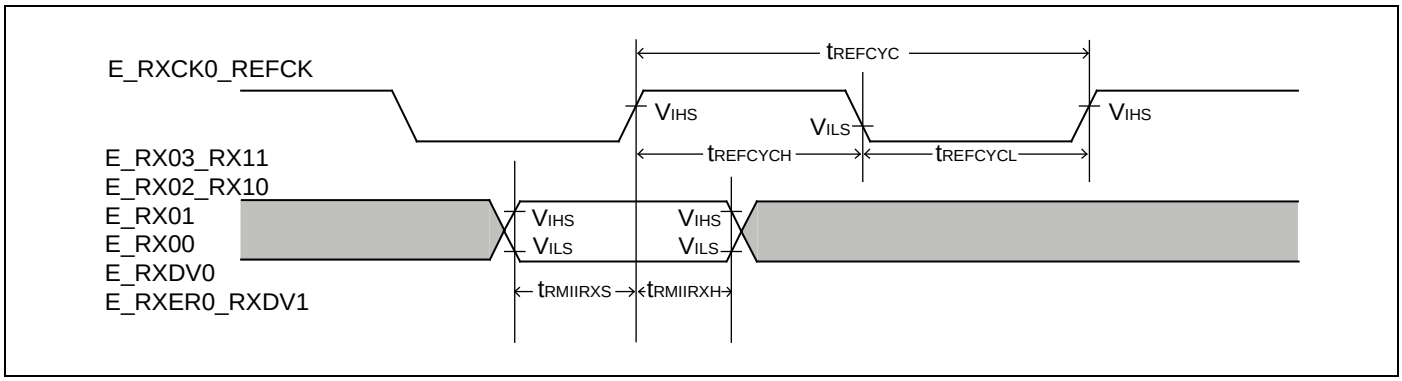
RMII receiving (100 Mbps/10 Mbps)

(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V)

(Vss = 0 V, T_A = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Reference Clock Cycle time*1	t_{REFCYC}	E_RXCK0_REFCK	20 ns (typical)	-	-	ns
Reference Clock High pulse width duty	$t_{REFCYCH}$	E_RXCK0_REFCK	$t_{REFCYCH}$ / t_{REFCYC}	35	65	%
Reference Clock Low pulse width duty	$t_{REFCYCL}$	E_RXCK0_REFCK	$t_{REFCYCL}$ / t_{REFCYC}	35	65	%
Received data → REFCK↑ Setup time(ch.0)	$t_{RMIIRXS}$	E_RX01, E_RX00, E_RXDV0	-	4	-	ns
Received data → REFCK↑ Setup time(ch.1)		E_RX03_RX11, E_RX02_RX10, E_RXER0_RXDV1				
REFCK ↑ → Received data Hold time(ch.0)	$t_{RMIIRXH}$	E_RX01, E_RX00, E_RXDV0	-	2	-	ns
REFCK ↑ → Received data Hold time (ch.1)		E_RX03_RX11, E_RX02_RX10, E_RXER0_RXDV1				

*1: The reference clock is fixed to 50 MHz in the RMII specifications.
The clock accuracy should meet the PHY-device specifications.

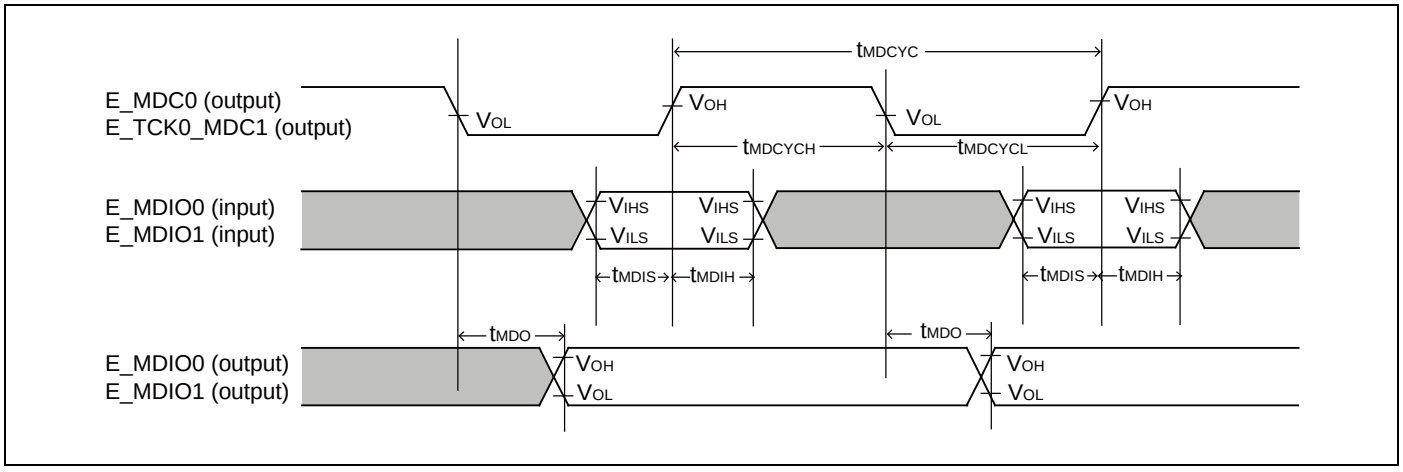


Management interface

(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V)
(Vss = 0 V, T_A = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Management Clock Cycle time*1 (ch.0)	t_{MDCYC}	E_MDC0	-	400	-	ns
Management Clock Cycle time*1 (ch.1)		E_TCK0_MDC1				
Management Clock High pulse width duty (ch.0)	t_{MDCYCH}	E_MDC0	t_{MDCYCH} / t_{MDCYC}	45	55	%
Management Clock High pulse width duty (ch.1)		E_TCK0_MDC1				
Management Clock Low pulse width duty (ch.0)	t_{MDCYCL}	E_MDC0	t_{MDCYCL} / t_{MDCYC}	45	55	%
Management Clock Low pulse width duty (ch.1)		E_TCK0_MDC1				
MDC ↓ → MDIO Delay time (ch.0)	t_{MDO}	E_MDIO0	-	-	60	ns
MDC ↓ → MDIO Delay time (ch.1)		E_MDIO1				
MDIO → MDC ↑ Setup time (ch.0)	t_{MDIS}	E_MDIO0	-	20	-	ns
MDIO → MDC ↑ Setup time (ch.1)		E_MDIO1				
MDC ↑ → MDIO Hold time (ch.0)	t_{MDIH}	E_MDIO0	-	0	-	ns
MDC ↑ → MDIO Hold time (ch.1)		E_MDIO1				

*1: The clock time should be set to a value greater than the minimum value by setting the Ether-MAC setting register.



MII transmission (100 Mbps/10 Mbps)

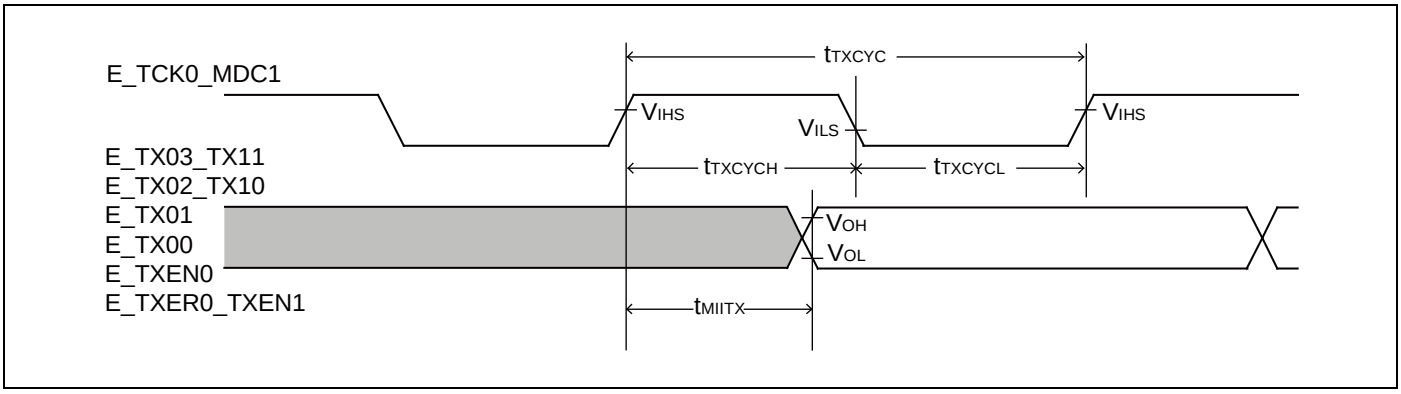
(ETHVcc = 3.0 V to 3.6 V, 4.5V to 5.5 V [*1])

(Vss = 0 V, T_A = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Transmission Clock Cycle time[*2]	t_{TXCYC}	E_TCK0_MDC1	100 Mbps, 40 ns (typical)	-	-	ns
			10 Mbps, 400 ns (typical)	-	-	ns
Transmission Clock High pulse width duty	t_{TXCYCH}	E_TCK0_MDC1	t_{TXCYCH} / t_{TXCYC}	35	65	%
Transmission Clock Low pulse width duty	t_{TXCYCL}	E_TCK0_MDC1	t_{TXCYCL} / t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data Delay time	t_{MIITX}	E_TX03_TX11, E_TX02_TX10, E_TX01, E_TX00, E_TXEN0, E_TXER0_TXEN1	-	-	24	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications.
The clock accuracy should meet the PHY-device specifications.

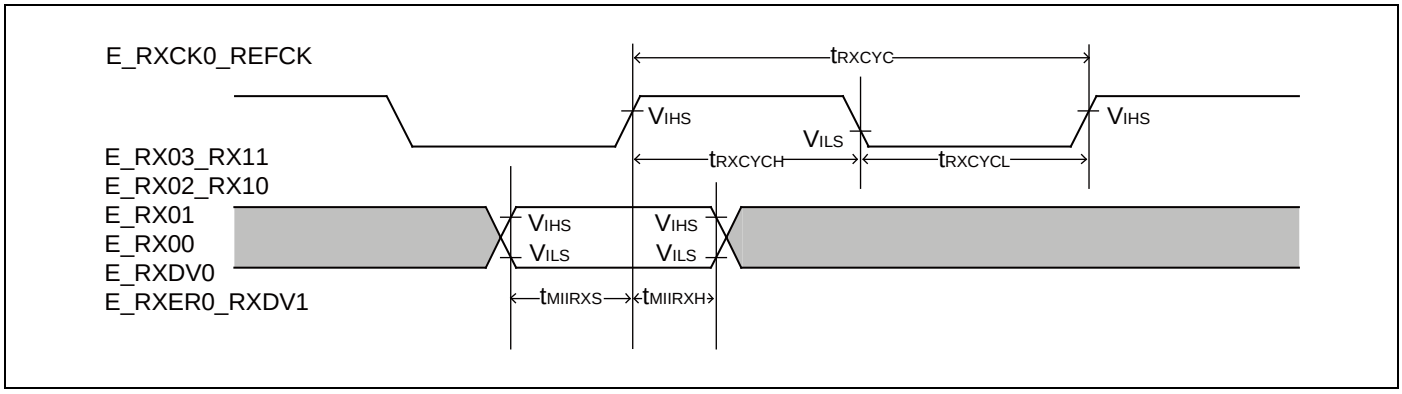


MII receiving (100 Mbps/10 Mbps)

(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V)
(Vss = 0 V, T_A = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Receiving Clock Cycle time*1	t_{RXCYC}	E_RXCK0_REFCK	100 Mbps, 40 ns (typical)	-	-	ns
			10 Mbps, 400 ns (typical)	-	-	ns
Receiving Clock High pulse width duty	t_{RXCYCH}	E_RXCK0_REFCK	t_{RXCYCH} / t_{RXCYC}	35	65	%
Receiving Clock Low pulse width duty	t_{RXCYCL}	E_RXCK0_REFCK	t_{RXCYCL} / t_{RXCYC}	35	65	%
Received data → REFCK ↑ Setup time	t_{MIIRXS}	E_RX03_RX11, E_RX02_RX10, E_RX01, E_RX00, E_RXDV0, E_RXER0_RXDV1	-	5	-	ns
REFCK ↑ → Received data Hold time	t_{MIIRXH}	E_RX03_RX11, E_RX02_RX10, E_RX01, E_RX00, E_RXDV0, E_RXER0_RXDV1	-	2	-	ns

*1: The receiving clock 100 Mbps is fixed to 25 MHz or 2.5 MHz in the MII specifications.
The clock accuracy should meet the PHY-device specifications.



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(Vcc = AVcc = 2.7 V to 5.5 V, Vss = AVss = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-		± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-		± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-		± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-		AVRH ± 15	mV	
Conversion time	-	-	1.0*1	-	-	µs	AVcc ≥ 4.5 V
			1.2*1	-	-		AVcc < 4.5 V
Sampling time	Ts	-	*2	-	-	ns	AVcc ≥ 4.5 V
			*2	-	-		AVcc < 4.5 V
Compare clock cycle*3	Tcck	-	50	-	2000	ns	
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	12.9	pF	
Analog input resistance	R_{AIN}	-	-	-	2	kΩ	AVcc ≥ 4.5 V
					3.8		AVcc < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	

*1: The Conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is the following.

AVcc ≥ 4.5 V, HCLK=120 MHz sampling time: 300 ns compare time: 700 ns
AVcc < 4.5 V, HCLK=120 MHz sampling time: 500 ns compare time: 700 ns

Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

The registers setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

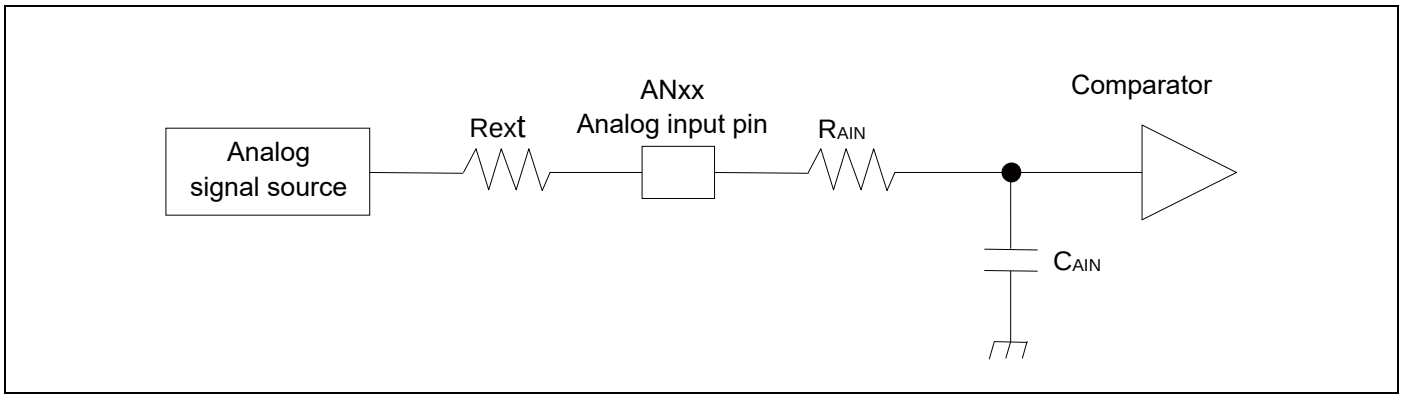
The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "8. Block Diagram" in this datasheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: Compare time (Tc) is the value of (Equation 2).



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

R_{AIN}: Input resistance of A/D = 2 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 3.8 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.9 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

Rext: Output impedance of external circuit

(Equation 2) Tc = Tcck × 14

Tc: Compare time

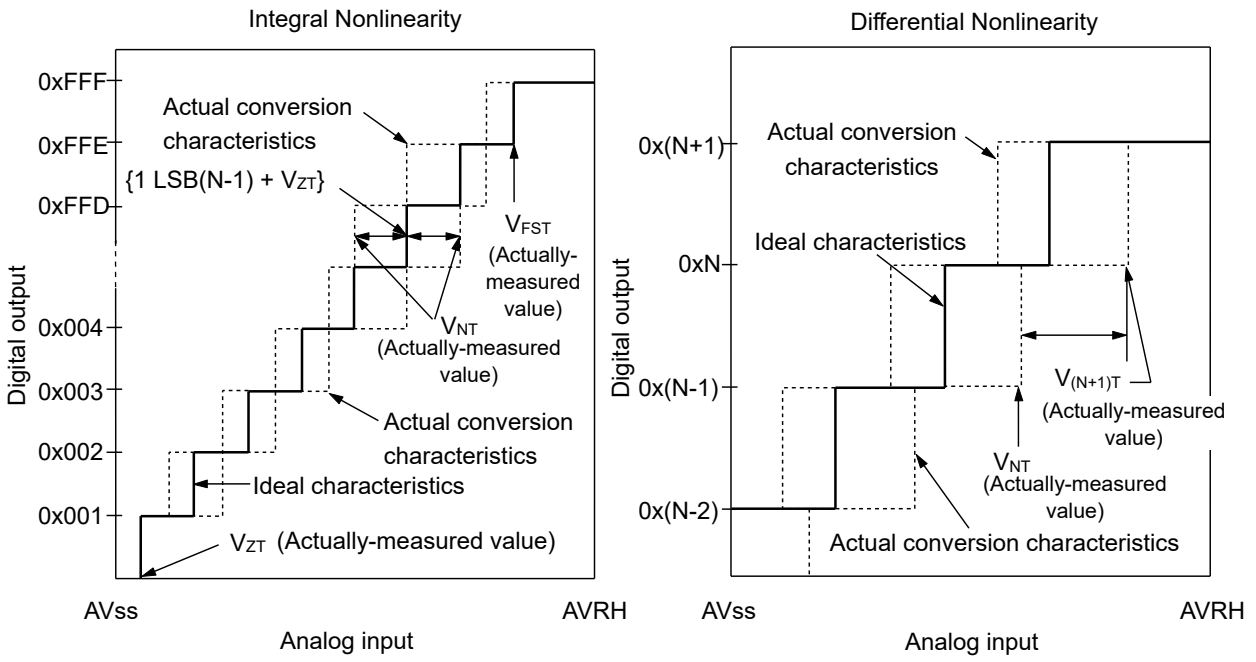
Tcck: Compare clock cycle

Definition of 12-bit A/D converter terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000⟷0b000000000001) and the full-scale transition point (0b111111111110⟷0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 USB characteristics

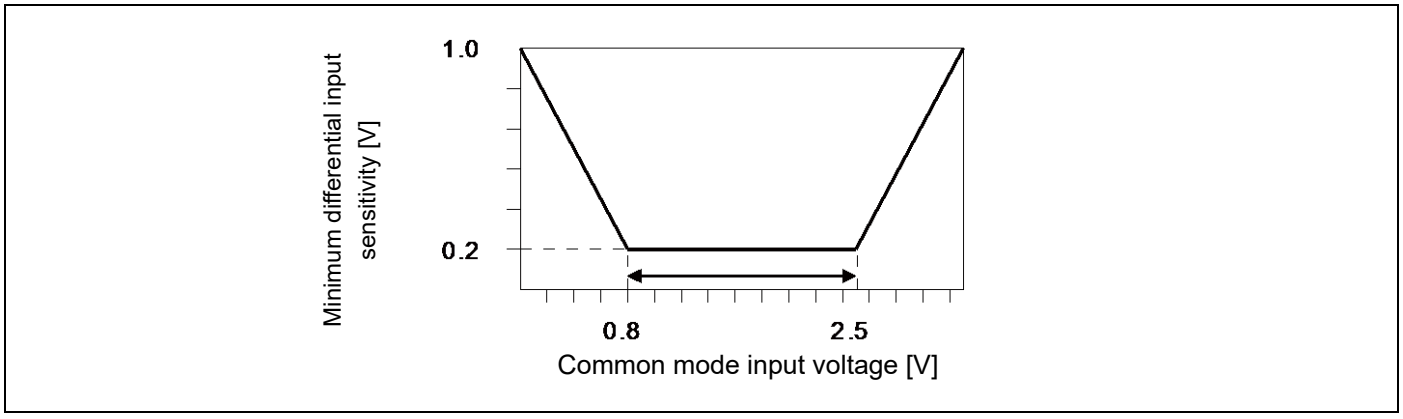
The USB characteristics of ch.0 and those of ch.1 are the same.
USBVcc0 and USBVcc1 are described as USBVcc below.

(Vcc = 2.7 V to 5.5 V, USBVcc = 3.0 V to 3.6 V, Vss = 0 V, T_A = - 40°C to + 85°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input "H" level voltage	V_{IH}	UDP0, UDM0	-	2.0	USBVcc + 0.3	V	*1
	Input "L" level voltage	V_{IL}		-	Vss - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output "H" level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output "L" level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rise time	t_{FR}		Full-Speed	4	20	ns	*5
	Fall time	t_{FF}		Full-Speed	4	20	ns	*5
	Rise/ fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rise time	t_{LR}		Low-Speed	75	300	ns	*7
	Fall time	t_{LF}		Low-Speed	75	300	ns	*7
	Rise/ fall time matching	t_{LRFM}		Low-Speed	80	125	%	*7

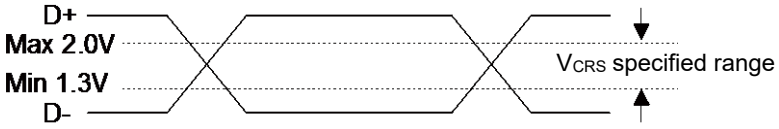
*1: The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.

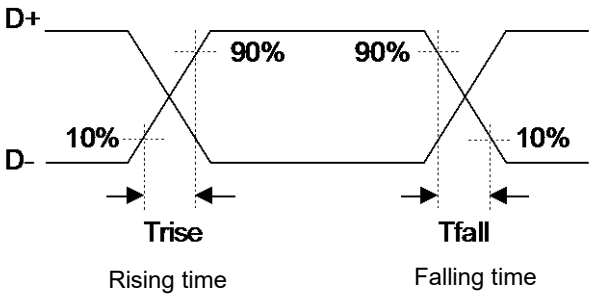


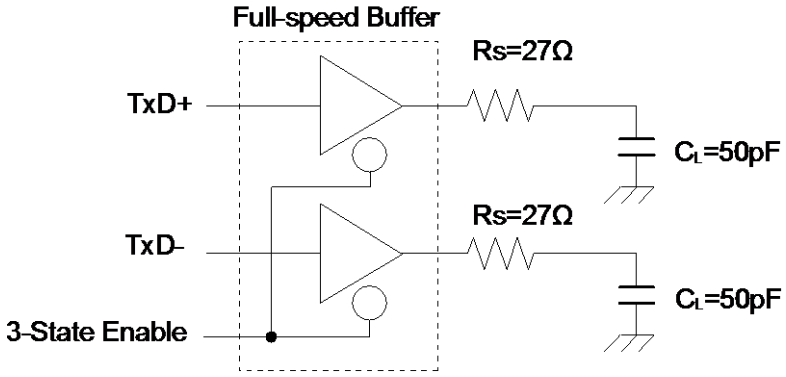
*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to ground and 1.5 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.

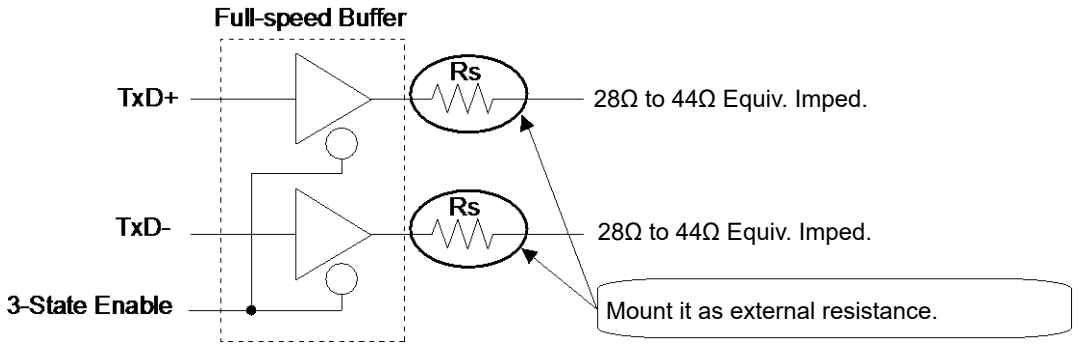


*5: They indicate rise time (Trise) and fall time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.



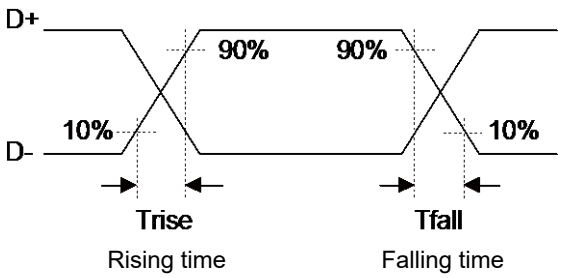


*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) series resistor Rs.



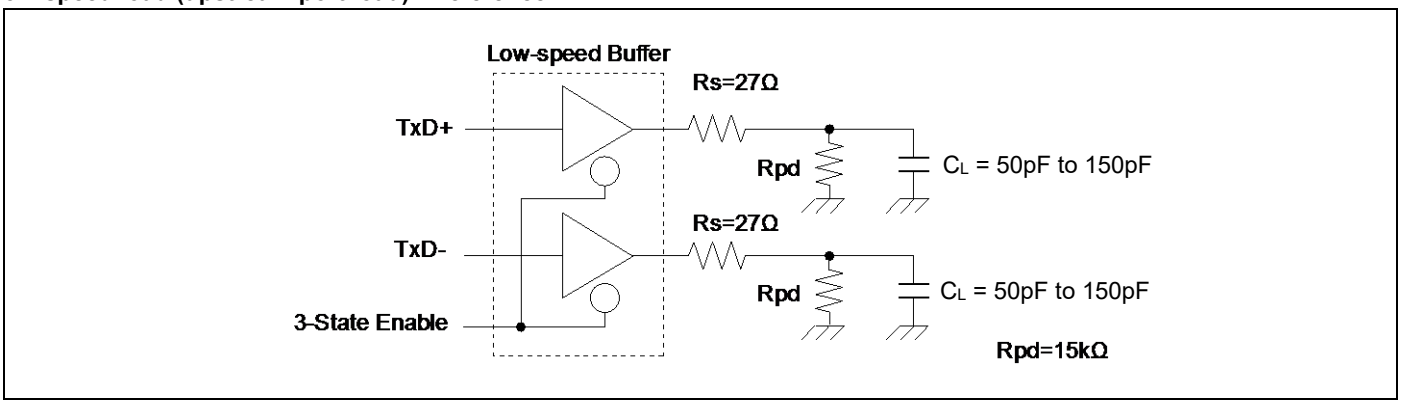
Rs series resistor 25 Ω to 30 Ω
Series resistor of 27 Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence".

*7: They indicate rise time (Trise) and fall time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.

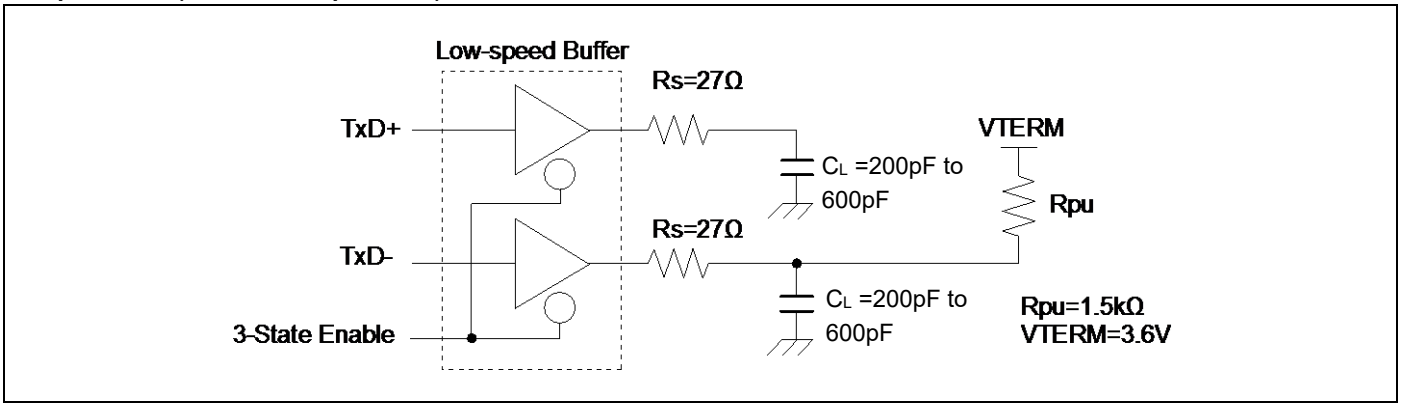


See Figure "Low-speed load (compliance load)" for conditions of external load.

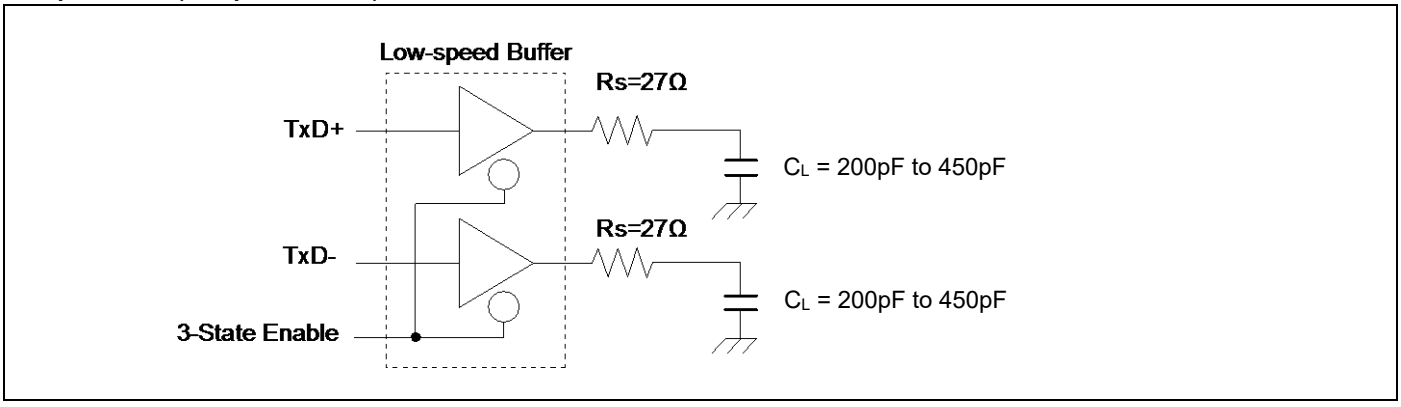
Low-speed load (upstream port load) - Reference 1



Low-speed load (downstream port load) - Reference 2



Low-speed load (compliance load)



12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	4032 × t_{CYCP}*1	µs	

*1: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8 Flash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(Vcc = 2.7 V to 5.5 V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*1	Max*1		
Sector erase time	Large Sector	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	0.3	1.1		
Half word (16-bit) write time		12	384	µs	Not including system-level overhead time.
Chip erase time		13.6	68	s	Includes write time prior to internal erase

*1: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*1	
10,000	10*1	
100,000	5*1	

*1: At average + 85°C

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

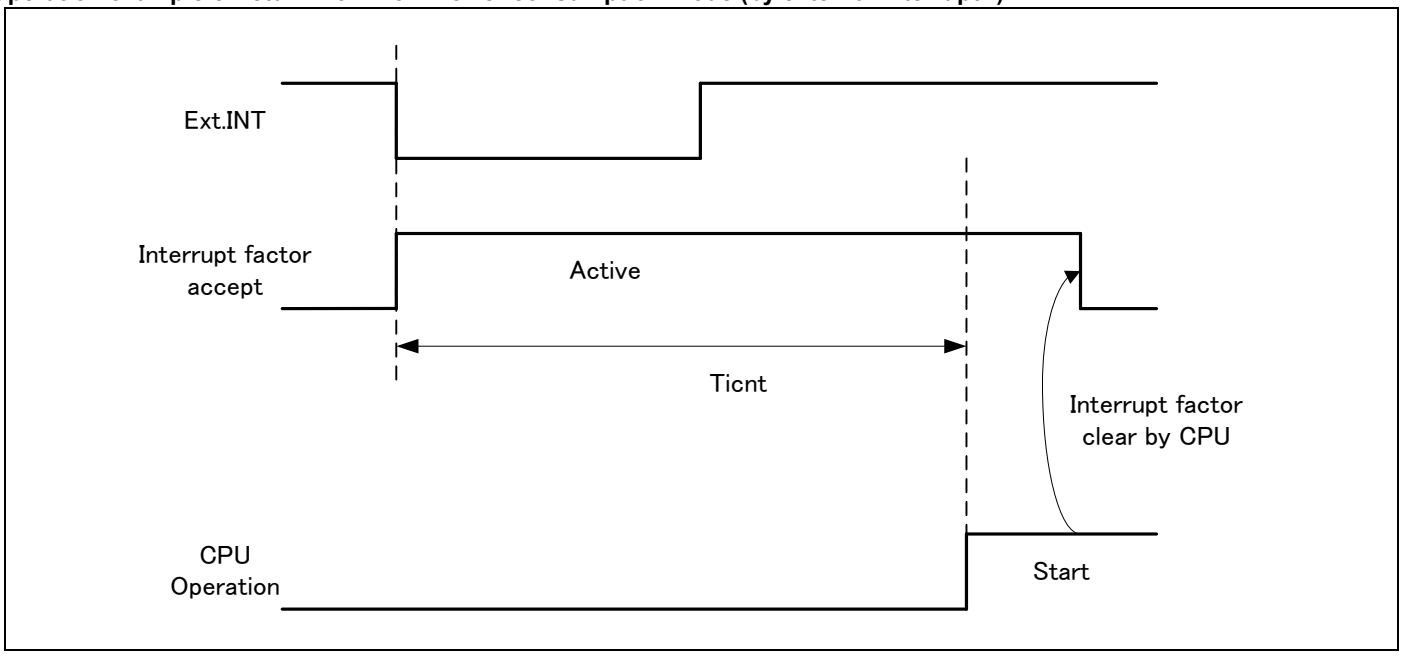
Return count time

(V_{CC} = 2.7 V to 5.5 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*1		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		40	80	µs	
Low-speed CR TIMER mode		453	737	µs	
Sub TIMER mode		453	737	µs	
STOP mode		453	737	µs	

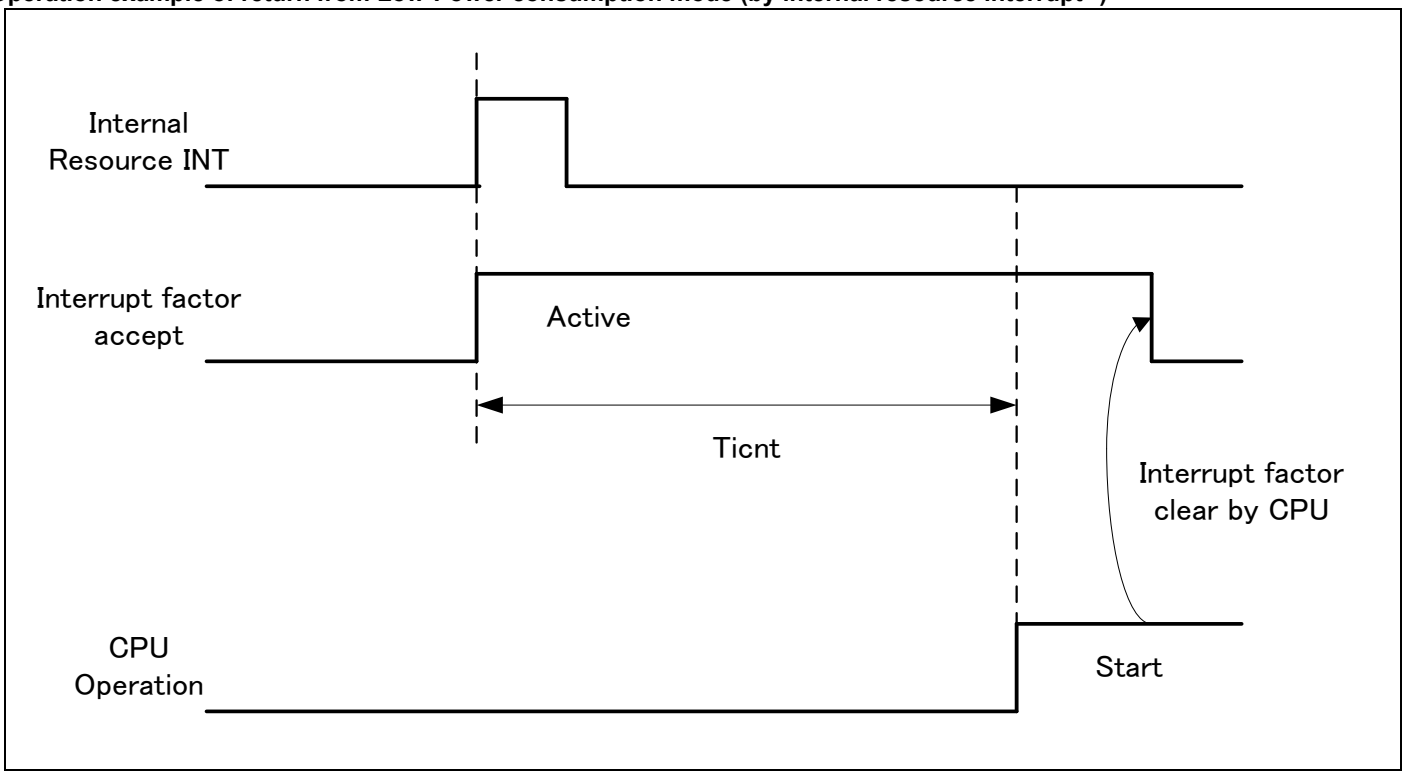
*1: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*1)



*1: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt[*1])



*1: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual about the return factor from Low-Power consumption mode.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".*

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

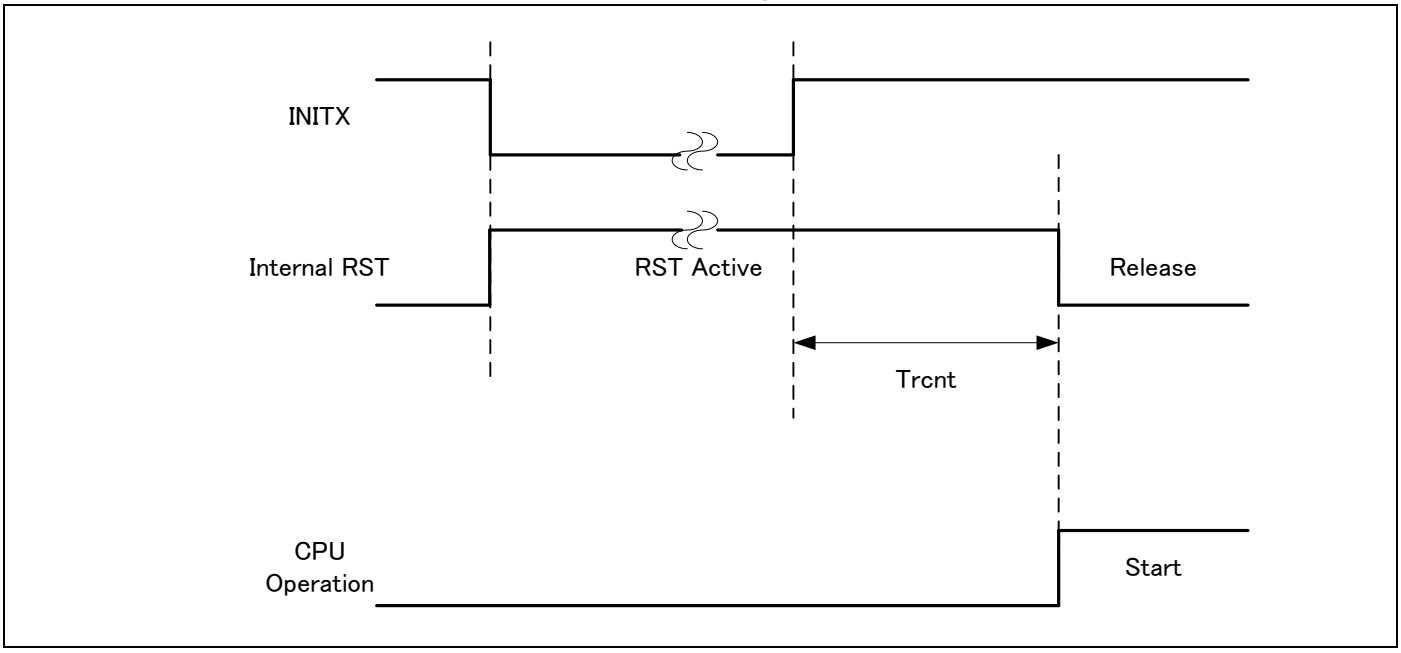
Return count time

(V_{CC} = 2.7 V to 5.5 V, T_A = - 40°C to + 85°C)

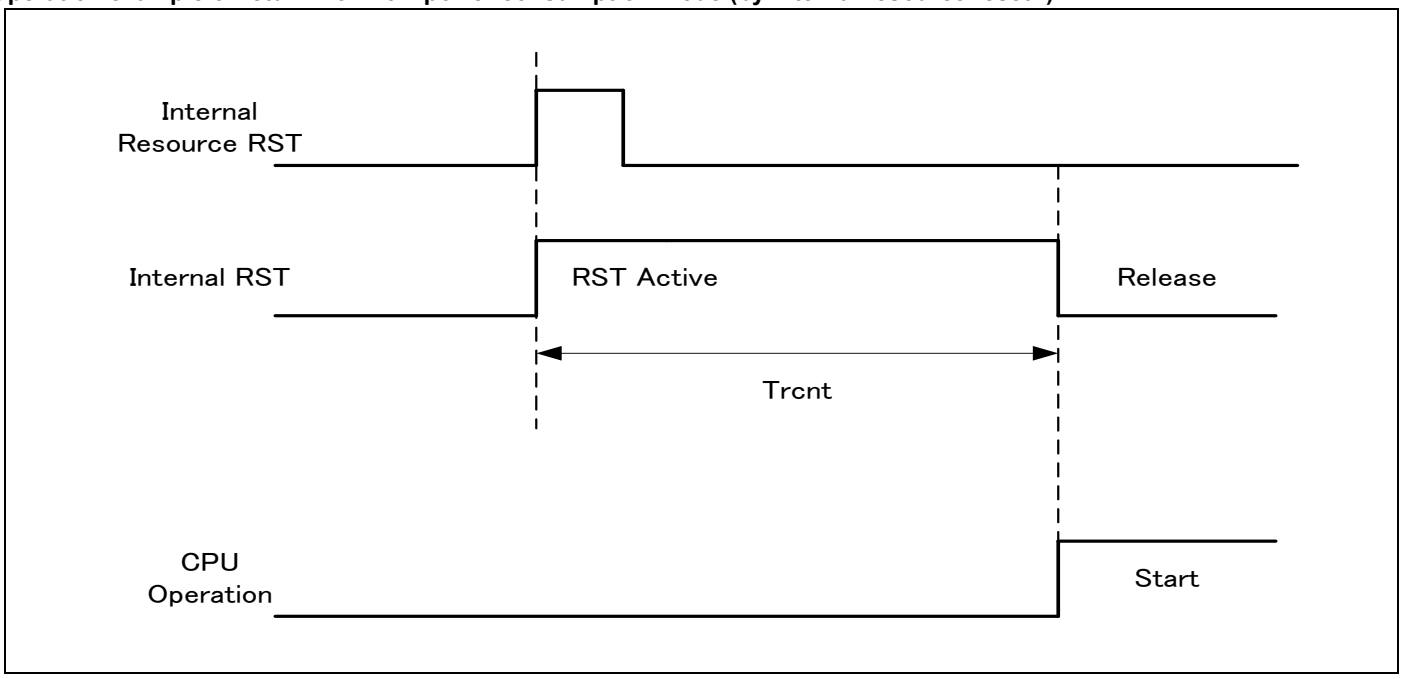
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*1		
SLEEP mode	Trcnt	321	461	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		321	461	µs	
Low-speed CR TIMER mode		441	701	µs	
Sub TIMER mode		441	701	µs	
STOP mode		441	701	µs	

*1: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset[*1])



*1: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

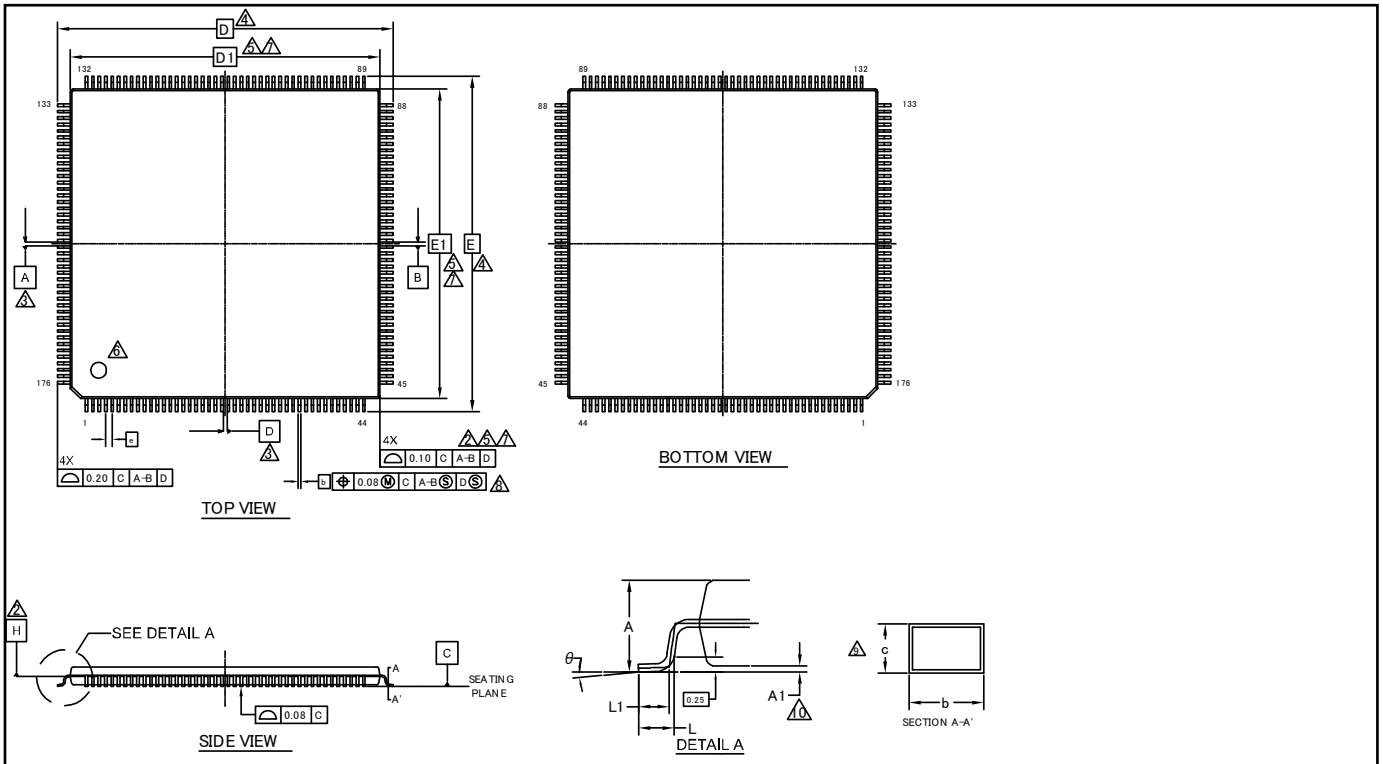
- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual"*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7. Power-on Reset Timing in 12.4. AC Characteristics 12. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
CY9BFD16TBGL-GK7E1	512 KB	64 KB	Plastic · PFBGA 192-pin (0.8 mm pitch), (LBE192)	Tray
CY9BFD17TBGL-GK7E1	768 KB	96 KB		
CY9BFD18TBGL-GK7E1	1 MB	128 KB		

14. Package Dimensions

Package Type	Package Code
LQFP 176	LQP176



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D		26.00 BSC	
D1		24.00 BSC	
e		0.50 BSC	
E		26.00 BSC	
E1		24.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

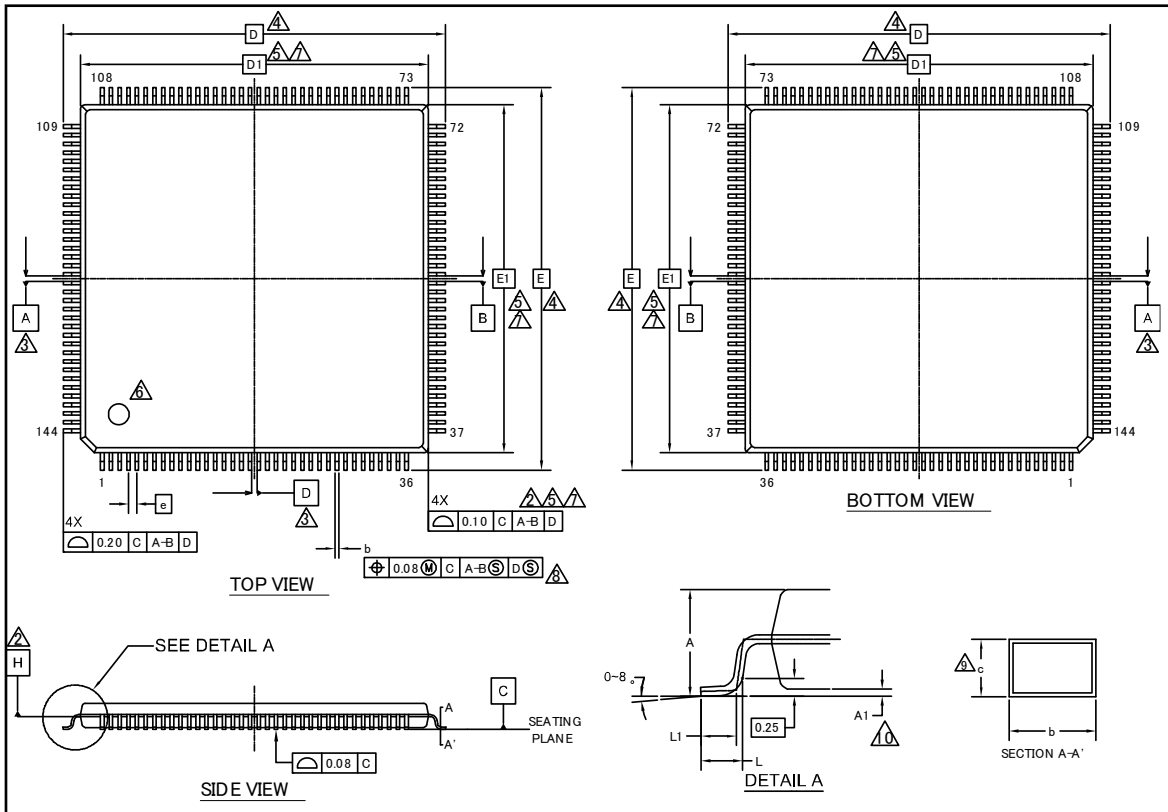
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

002-15150 **

Package Type	Package Code
LQFP 144	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

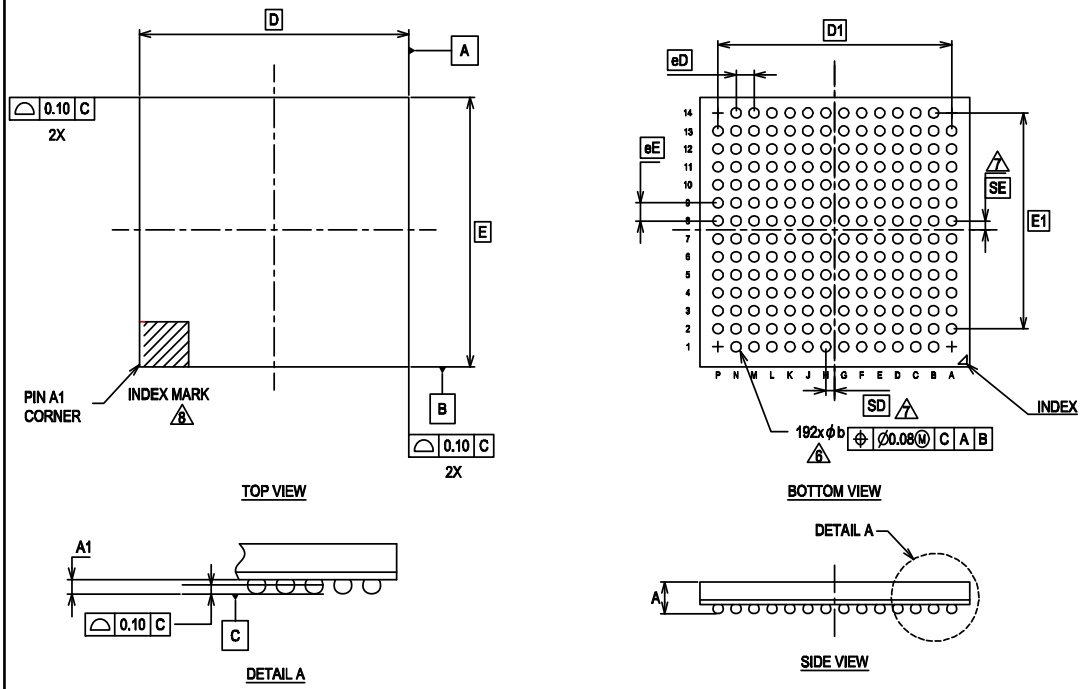
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

002-13015 *A

Package Type	Package Code
FBGA 192	LBE192

LBE192 192 BALL LOW PROFILE FINE PITCH BALL GRID ARRAY PACKAGE



SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	1.45	PROFILE
A_1	0.25	0.35	0.45	TERMINAL HEIGHT
D		12.00 BSC		BODY SIZE
E		12.00 BSC		BODY SIZE
D_1		10.40 BSC		MATRIX FOOTPRINT
E_1		10.40 BSC		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		192		BALL COUNT
Φb	0.35	0.45	0.55	BALL DIAMETER
eD		0.80 BSC		BALL PITCH
eE		0.80 BSC		BALL PITCH
SD / SE		0.40		SOLDER BALL PLACEMENT
		A1,A14,P1,P14		DEPOPULATED SOLDER BALL LOCATIONS

1. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE=0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE= e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0A 002-13493 *A

15. Major Changes

Spansion Publication Number: DS706-00031

Page	Section	Change Results
Revision 1.0		
-	-	Preliminary → Datasheet
1	DESCRIPTION	Corrected the description.
3	FEATURES Multi-function Serial Interface (Max 8channels)	Revised the following description. "4 channels with 16-byte FIFO" →"4 channels with 16steps×9-bit FIFO"
7	PRODUCT LINEUP Multi-function Serial Interface (UART/CSIO/LIN/I²C)	Added the following description. "ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO"
9 to 11	PIN ASSIGNMENT	Added the description of "Note".
55	I/O CIRCUIT TYPE	Added the following description to "Type H". I_{OH} = -20.5mA, I_{OL} = 18.5mA
62 to 64	HANDLING DEVICES	Revised the description of "Power supply pins". Revised the description of "C pin". Added the description of "Base Timer".
65	BLOCK DIAGRAM	Corrected the figure. TIOA: input → input/output TIOB: output → input
77	ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Corrected the value of "Analog reference voltage (AVRH)". Min: AV_{SS} → 2.7V Added the "Smoothing capacitor (C_S)". Added the footnote.
80	3. DC Characteristics (1) Current Rating	Revised the value of "TBD". Revised the unit. Deleted "and estimated values."
83	4. AC Characteristics (1) Main Clock Input Characteristics	Added "Internal operating clock frequency (F_{CM}): Master clock".
85	(4-1) Operating Conditions of Main and USB/Ethernet PLL (In the case of using main clock for input of PLL) (4-2) Operating Conditions of Main PLL (In the case of using high-speed internal CR)	Added "Main PLL clock frequency (F_{CLKPLL})". Added "USB/Ethernet clock frequency ($F_{CLKSPLL}$)".
113	Management Interface	Revised the value of "MDC ↑ → MDIO Hold time". Min: 20 → 0
116	5. 12-bit A/D Converter Electrical characteristics for the A/D converter	Deleted "(Preliminary value)". Added the Symbol. Revised the value of "TBD". Revised the maximum value of "Power supply current (analog + digital)": A/D 1unit operation: Typ: 0.47 → 0.57 When A/D stops: Typ: 0.01 → 0.06 Revised the value of "Reference power supply current (between AVRH to AVSS)" When A/D stops: Typ: 0.01 → 0.06 Deleted the following Pin name. - "Sampling time" - "Compare clock cycle" - "State transition time to operation permission" - "Analog input capacity" - "Analog input resistance" Corrected the value of "Compare clock cycle (Tcck)". Max: 10000 → 2000
119	6. USB Characteristics	Corrected the condition of "Output L level voltage". External pull-down → External pull-up
123	7. Low-voltage Detection Characteristics (2) Interrupt of Low-Voltage Detection	Corrected the value of "LVD stabilization wait time (T_{LVDW})". Max: 2240 × tcyc → 4032 × t_{CYCP}
124	8. Flash Memory Write/Erase Characteristics Erase/write cycles and data hold time	Deleted "(targeted value)".

Page	Section	Change Results
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	Features USB Interface Ethernet-MAC	Added the description of PLL for USB and Ethernet
2	Features USB Interface	Added the size of each EndPoint
3	Features External Bus Interface	Added the description of Maximum area size
9, 10	Pin Assignment	Added SWCLK and SWDIO and SWO
52 to 57	I/O Circuit Type	Added the description of I^2C to the type of E, F, I, L Added about +B input
62	Handling Devices	Added "Stabilizing power supply voltage"
62	Handling Devices Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
63	Handling Devices C Pin	Changed the description
65	Block Diagram	Modified the block diagram
67	Memory Map Memory map(1)	Modified the area of "External Device Area"
68	Memory Map Memory map(2)	Added the summary of Flash memory sector and the note
75, 76	Electrical Characteristics 1. Absolute Maximum Ratings	Added the Clamp maximum current Added the output current of P80, P81, P82, P83 Added about +B input
77	Electrical Characteristics 2. Recommended Operation Conditions	Modified the minimum value of Analog reference voltage Added Smoothing capacitor Added the note about less than the minimum power supply voltage
79, 80	Electrical Characteristics 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Added Flash Memory Current Moved A/D Converter Current
84	Electrical Characteristics 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR
86	Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	Added Time until releasing Power-on reset Changed the figure of timing
88 to 90	Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
97 to 104	Electrical Characteristics 4. AC Characteristics (9) CSIO/UART Timing	Modified from UART Timing to CSIO/UART Timing Changed from Internal shift clock operation to Master mode Changed from External shift clock operation to Slave mode
116	Electrical Characteristics 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage Added Conversion time at AVcc < 4.5 V Modified Stage transition time to operation permission Modified the minimum value of Reference voltage
125 to 128	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
129	Ordering Information	Change to full part number

Note: Please see “Document History” about later revised information.

Document History

Document Title: CY9BD10T Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05629

Revision	ECN	Submission Date	Description of Change
**	–	02/10/2015	Migrated to Cypress and assigned document number 002-05639. No change to document contents or format.
*A	5208926	04/06/2016	Updated to Cypress format.
*B	5560212	03/09/2017	Updated “12.4.7 Power-On Reset Timing”. Changed parameter from “Power Supply rising time(Tr)[ms]” to “Power ramp rate(dV/dt)[mV/us]” and added some comments (Page 83) Added Notes for JTAG (Page 50), Changed “J-TAG” to” JTAG” in “4 List of Pin Functions” (Page 32) Updated Package code and dimensions as follows (Page 8-11, 73, 126-129) FPT-144P-M08 -> LQS144, FPT-176P-M07 -> LQP176, BGA-192P-M06 -> LBE192 Change the name from “USB Function” to “USB Device” (Page 1, 7, 48) Corrected the following statement Analog port input current → Analog port input leak current in chapter 12.5. 12-bit A/D Converter (Page 113) Added the Baud rate spec in “12.4.10 CSIO/UART Timing”.(Page 94, 96, 98, 100) Deleted MPNs below from “13. Ordering Information” (Page 126) MB9BFD16SPMC-GE1, MB9BFD16TBGL-GE1, MB9BFD16TPMC-GE1, MB9BFD17SPMC-GE1, MB9BFD17TBGL-GE1, MB9BFD17TPMC-GE1, MB9BFD18SPMC-GE1, MB9BFD18TBGL-GE1, MB9BFD18TPMC-GE1 Added MPNs below to “13. Ordering Information” (Page 126) MB9BFD16SPMC-GK7E1, MB9BFD16TBGL-GK7E1, MB9BFD16TPMC-GK7E1, MB9BFD17SPMC-GK7E1, MB9BFD17TBGL-GK7E1, MB9BFD17TPMC-GK7E1, MB9BFD18SPMC-GK7E1, MB9BFD18TBGL-GK7E1, MB9BFD18TPMC-GK7E1
*C	5797507	07/11/2017	Adapted new Cypress logo
*D	6013737	01/15/2018	Updated Arm trademark and the last page Updated the figure of LBE192 in 14. Package Dimensions
*E	6054039	02/01/2018	Update Ethernet- MAC error from IEEE1558-2008 (PTP) to IEEE1588-2008 (PTP)
*F	6268602	08/01/2018	Obsoleted
*G	6351925	10/16/2018	Reactivate document. No change.
*H	6881610	05/13/2020	Updated Ordering Information and removed the following Part numbers from the Table: CY9BFD16SPMC-GK7MJE1, CY9BFD17SPMC-GK7MJE1, CY9BFD18SPMC-GK7MJE1 CY9BFD16TPMC-GK7MJE1, CY9BFD17TPMC-GK7MJE1, CY9BFD18TPMC-GK7MJE1 Updated Part Numbers across the document.

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