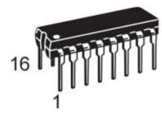
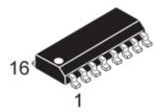
3-to-8 line decoder/demultiplexer

FEATURES

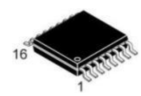
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- ICC category: MSI



DIP-16



SOP-16


TSSOP-16

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC238N	DIP-16	74HC238	TUBE	1000pcs/box
74HC238M/TR	SOP-16	74HC238	REEL	2500pcs/reel
74HC238MT/TR	TSSOP-16	HC238	REEL	2500pcs/reel

GENERAL DESCRIPTION

The 74HC238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled,provide 8 mutually exclusive active HIGH outputs (Y0 to Y7).

The 74HC238 features three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be LOW unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the HC238 to a 1-of-32 (5 lines to 32 lines) decoder with just four HC238 ICs and one inverter.

The 74HC238 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The 74HC238 is identical to the 74HC138 but has non-inverting outputs.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

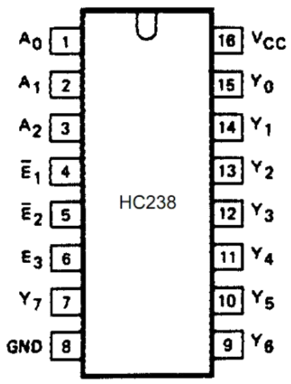


Fig.1 Pin configuration.

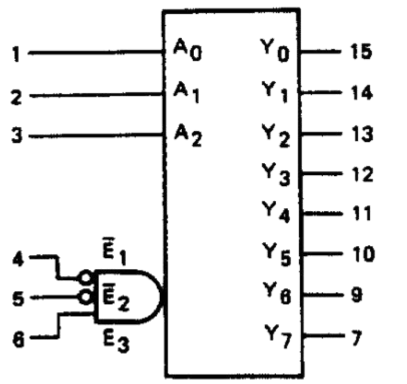


Fig.2 Logic symbol.

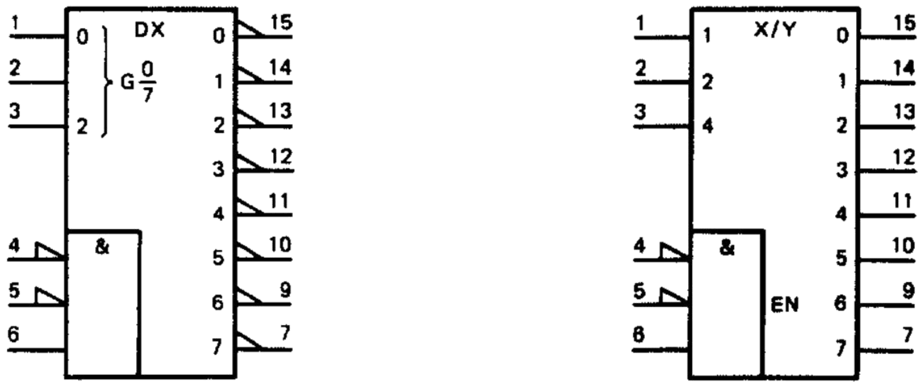


Fig.3 IEC logic symbol.

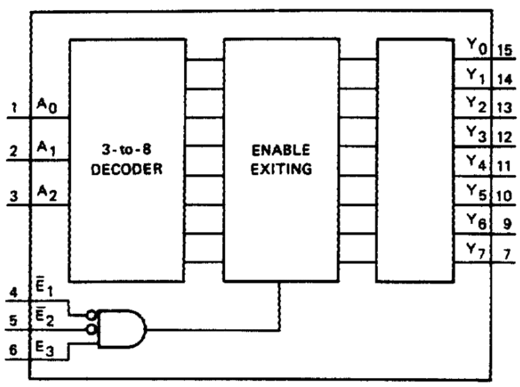


Fig.4 Functional diagram.

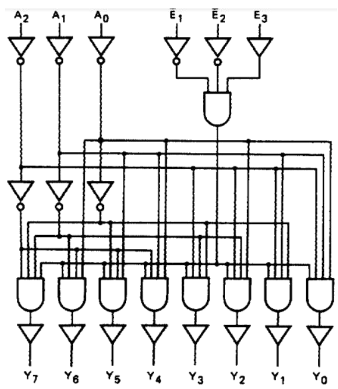


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note

1. H = HIGH voltage level
2. L = LOWvoltage level
3. X = don't care

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n E_3 to Y_n $\overline{E}_n$ to Y_n	C_L = 15 pF; V_{CC} =5 V	 14 16 17	 ns ns ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1and 2	72	pF

Notes

CPD is used to determine the dynamic power dissipation (PD in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum(CL \times VCC \times fo)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

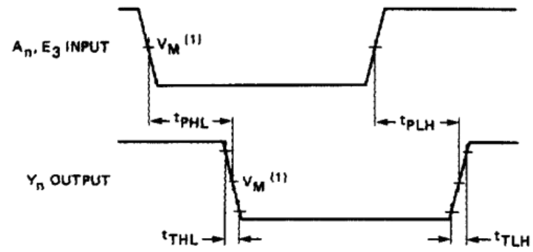
For HC238 the condition is V I = GND to VCC

AC CHARACTERISTICS FOR

GND = 0 V; tr = tf = 6 ns; CL = 50 pF

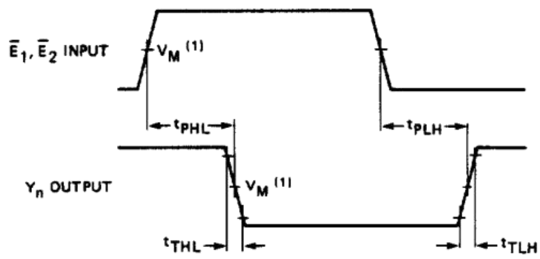
SYMBOL	PARAMETER	T_{amb}(℃)							UNIT	TEST CONDITIONS	
		74HC238								V_{CC}(V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delayA_n toY_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delayE_3 toY_n		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delayE_n toY_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC WAVEFORMS



(1)HC238: V_M = 50%; V_I = GND to V_{CC}.

Fig.6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times.

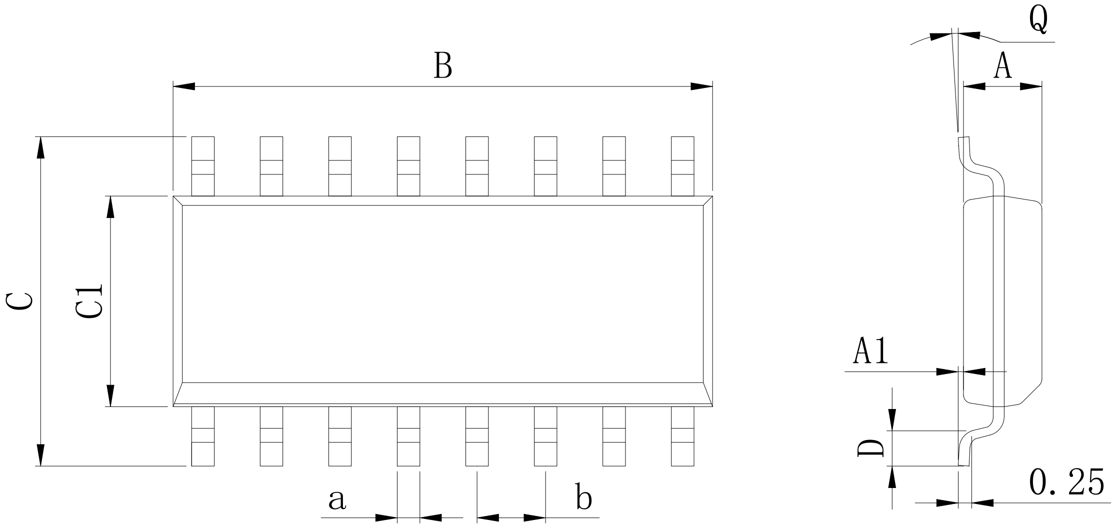


(1)HC238: V_M = 50%; V_I = GND to V_{CC}.

Fig.7 Waveforms showing the enable input ($\overline{E}_n$) to output (Y_n) propagation delays and the output transition times.

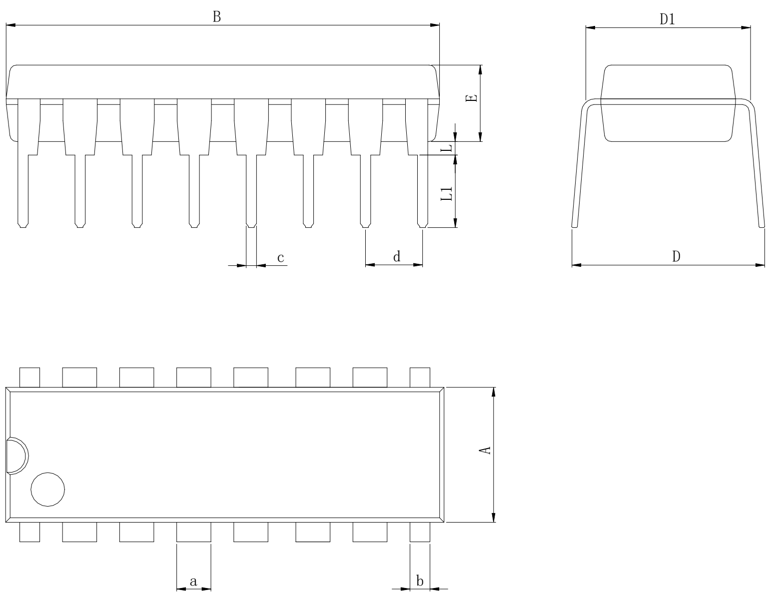
Physical Dimensions

SOP16



Dimensions In Millimeters(SOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

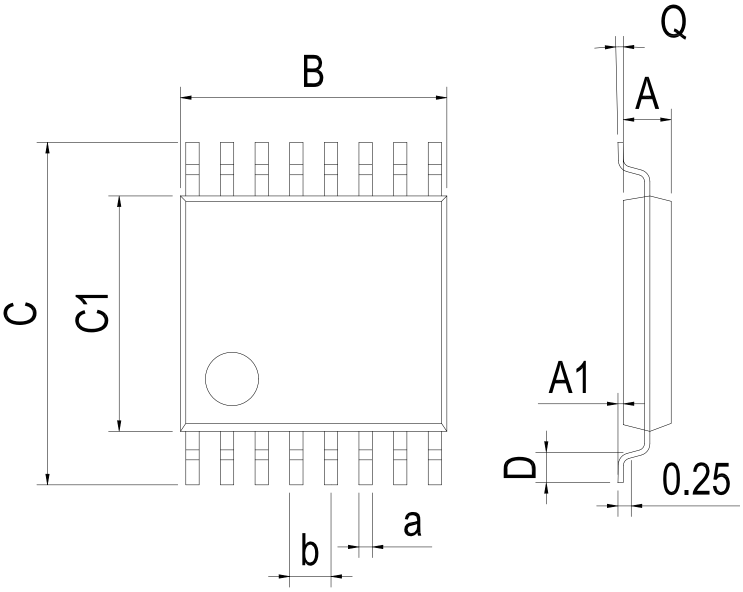
DIP16



Dimensions In Millimeters(DIP16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

Physical Dimensions

TSSOP16



Dimensions In Millimeters(TSSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

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