General Description:

JX-F38P is a high performance 2.0MP CMOS image sensor designed and fabricated with SOI's 2.5um pixel technology. It can deliver images at 30fps in full HD mode.

The JX-F38P consists of a 1928 x 1088 active pixel sensor (APS) array with on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 dual-data lane serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

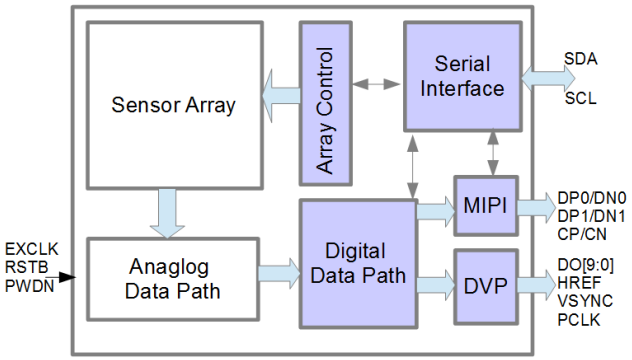
Features:

- Automatic functions:
  - ABLC – Automatic Black Level Calibration
- Programmable controls:
  - Gain, exposure, frame rate and size
  - Image mirror and flip
  - Window panning and cropping
  - I2C slave ID
- Output formats:
  - DVP parallel interface
  - MIPI CSI2 (dual lane)
- Data formats:
  - 10-bit RAW RGB
- Others
  - 50/60Hz flick noise cancellation
  - Frame sync
  - Register group write capability
  - Black sun spot cancellation

Key Specifications:

Optical format		1/3.2"
Active Pixels		1928H x 1088V
Pixel size		2.5 x 2.5 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		12.5 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		FHD: 1920x1080 @30fps HDR: 1920x1080@15ps (MIPI), 2 frames staggered output
Supply voltage	**Analog**	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.0V (1.8V nominal)
Power consumption	**Active**	103.8 mW
	Standby	Typ.: 300 uA
Output Formats		10-bit RGB Raw Data
Sensitivity		2700 mV/lux-sec
Max SNR		38.5 db
Dynamic range		79.2 db
Dark Current		5.0 mV/sec @ 45 °C
Operating junction temperature		-30 °C to 85 °C
Stable image junction temperature		60 °C

Functional Block:



Component Order Information:

Part Number	Description
JX-F38P-C1-D3	CSP, DVP interface
JX-F38P-C1-M3	CSP, MIPI interface

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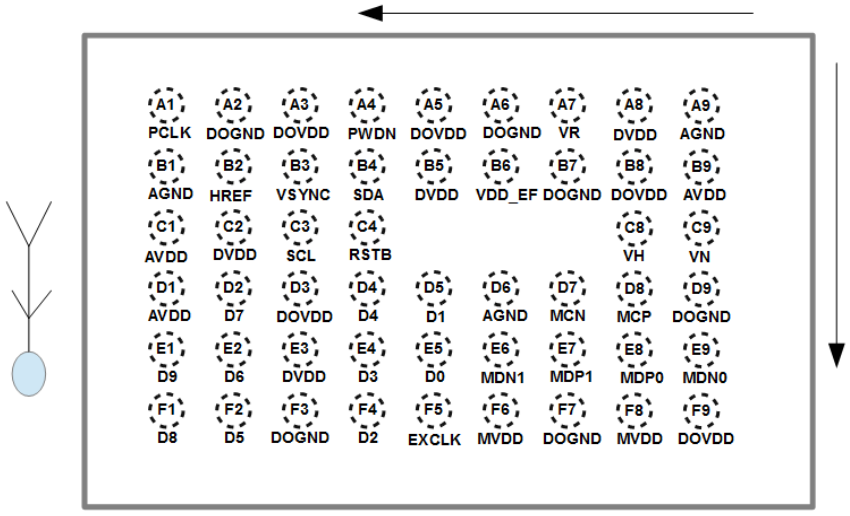
Pin Diagram:

JX-F38P's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1: JX-F38P CSP top view



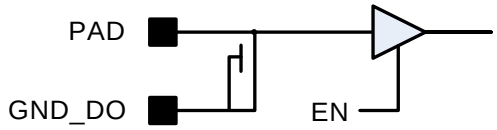
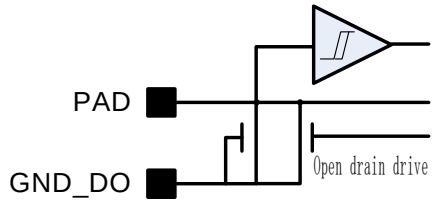
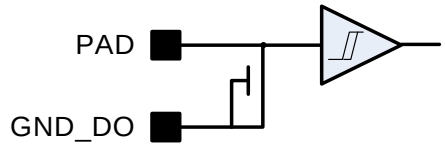
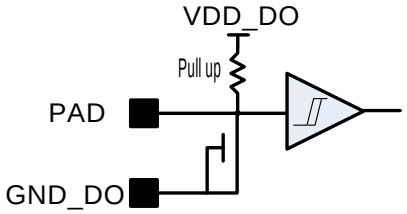
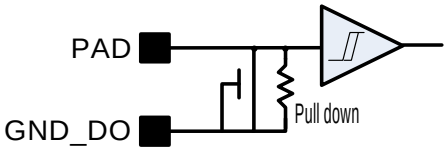
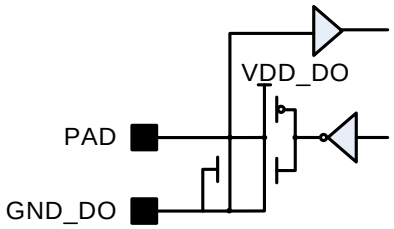
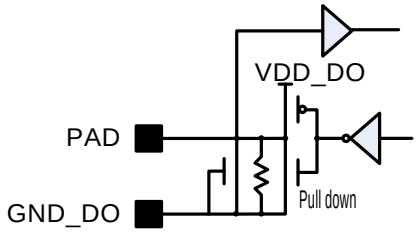
In order to prevent the sun stripe effect, please put F9 pad at the right-bottom corner of PCB layout and set sensor operating at mirror-flip mode. Above placement and operating setting also can get the positive direction image. For sensor placement and operating mode, several settings can have effect on image output direction. These registers include SYS, H_Mirror, V_Flip. Please consult your SOI AE for further information.

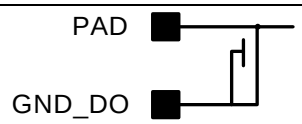
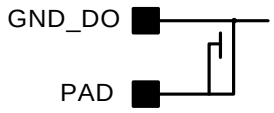
Table 1: Pin Description

Pin number	Pin name	Pin type	Description
A1	PCLK	I/O	DVP Pixel clock output.
A2	DOGND	Supply	Digital I/O ground
A3	DOVDD	Supply	Digital I/O supply voltage.
A4	PWDN	Input	System power down control. High active.
A5	DOVDD	Supply	Digital I/O supply voltage.
A6	DOGND	Supply	Digital I/O ground
A7	VR	Reference	Analog Reference
A8	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
A9	AGND	Supply	Analog ground
B1	AGND	Supply	Analog ground
B2	HREF	I/O	Line data valid signal output.
B3	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also, can be programmed as frame synchronize input
B4	SDA	I/O	Serial data, pull to DOVDD with a 4.7k Ω resistor
B5	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
B6	VDD_EF	Supply	Analog supply for Efuse; Need floating.
B7	DOGND	Supply	Digital I/O ground
B8	DOVDD	Supply	Digital I/O supply voltage.
B9	AVDD	Supply	Analog supply voltage.
C1	AVDD	Supply	Analog supply voltage.
C2	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
C3	SCL	Input	Serial interface clock input.
C4	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
C5			
C6			
C7			
C8	VH	Reference	Internal analog reference.
C9	VN	Reference	Internal analog reference.
D1	AVDD	Supply	Analog supply voltage.
D2	D7	I/O	DVP data output bit 7
D3	DOVDD	Supply	Digital I/O supply voltage.
D4	D4	I/O	DVP data output bit 4
D5	D1/SID1	I/O	DVP data output bit 1. I2C Slave ID programming bit<1>, default pull down internally. I2C slave ID can be programmed as “80/81”, “84/85”, “88/89” or ”8C/8D” for write and read.
D6	AGND	Supply	Analog ground
D7	MCN	I/O	MIPI clock lane negative output.
D8	MCP	I/O	MIPI clock lane positive output.
D9	DOGND	Supply	Digital I/O ground
E1	D9	I/O	DVP data output bit 9
E2	D6	I/O	DVP data output bit 6
E3	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
E4	D3	I/O	DVP data output bit 3
E5	D0/SID0	I/O	Pixel data output bit 0. I2C Slave ID programming bit<0>, default pull down internally.

E6	MDN1	I/O	MIPI data lane 1 negative output.
E7	MDP1	I/O	MIPI data lane 1 positive output.
E8	MDP0	I/O	MIPI data lane 0 positive output.
E9	MDN0	I/O	MIPI data lane 0 negative output.
F1	D8	I/O	DVP data output bit 8
F2	D5	I/O	DVP data output bit 5
F3	DOGND	Supply	Digital I/O ground
F4	D2	I/O	DVP data output bit 2
F5	EXCLK	Input	System clock input.
F6	MVDD	Supply	MIPI supply voltage. Connect to DVDD.
F7	DOGND	Supply	Digital I/O ground
F8	MVDD	Supply	MIPI supply voltage. Connect to DVDD.
F9	DOVDD	Supply	Digital I/O supply voltage.

Table2: I/O Equivalent Circuit Diagram

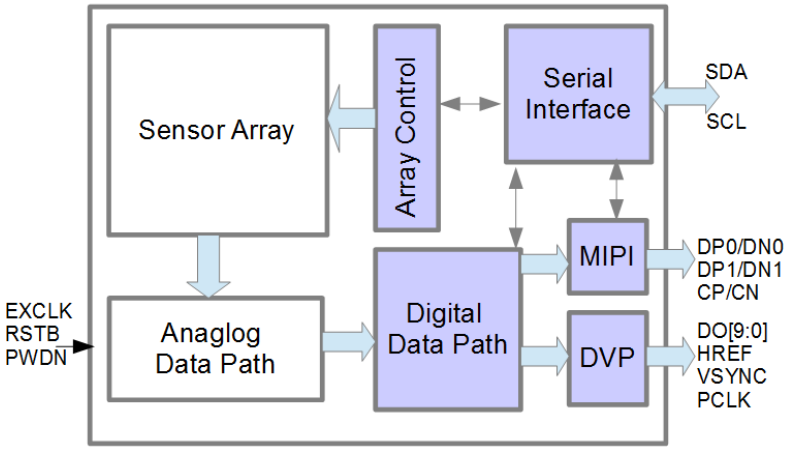
Symbol	Equivalent Circuit
EXCLK	
SDA	
SCL	
RSTB	
PWDN	
D9,D8,D7,D6,D5, D4,D3,D2,HREF,VS, PCLK	
D1,D0	

MDP1,MDN1, MDP0,MDN0,MCP, MCN,VH,VR	
VN	

Functional Overview:

The JX-F38P is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Figure 2 illustrates the sensor's block diagram.

Figure 2. Functional Block Diagram



User can access and program JX-F38P sensor internal registers through the two-wire serial bus. The core of the sensor is a 1928x1088 pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-F38P pixel array consists of a 1928-column by 1112-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3,4 for JX-F38P's Pixel array structure). The first 24 rows are optical black row for black level calibration. Outside of the 1920x1080 active pixels, there are several boundary pixels:4 rows on top, 4 rows at the bottom, 4 columns on the right, and 4 columns on the left. Please note that only performance of the active image area is defined in the outgoing specifications, performance of dummy columns and rows are not guaranteed as same as the active image. The detailed pixel array arrangement and default read out direction is noted in the following two figures:

Figure 3: Pixel array structure

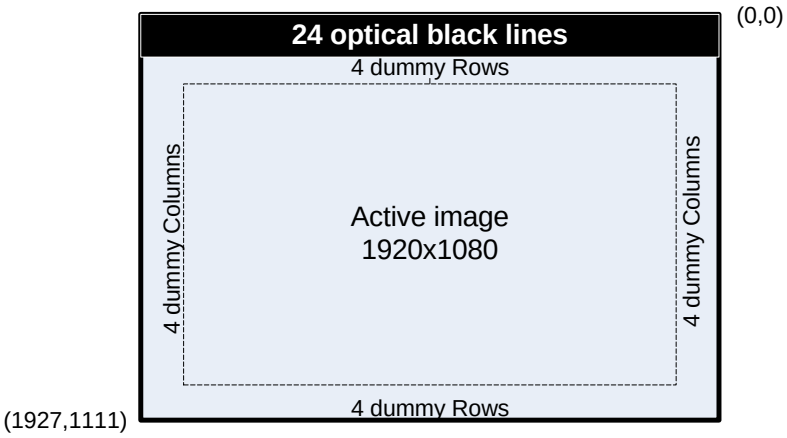
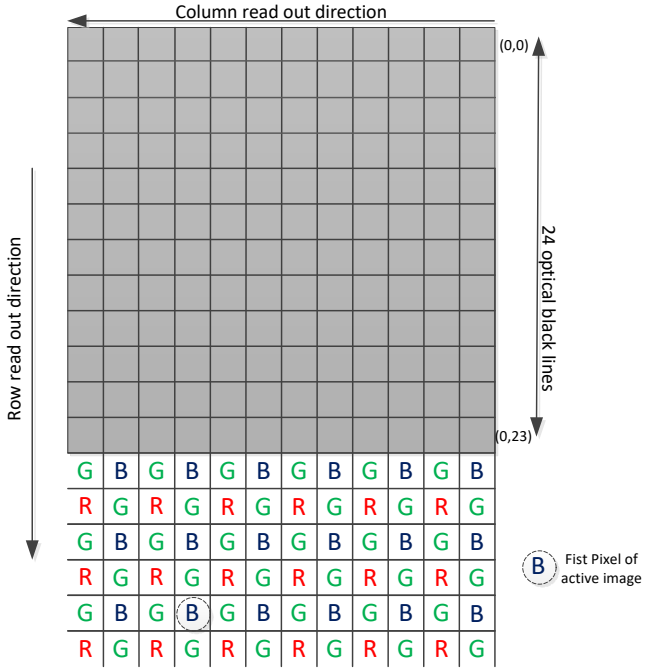


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1080 lines (rows) of 1920 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-F38P default frame timing is illustrated as figure 6.

Figure 5: Row data output timing

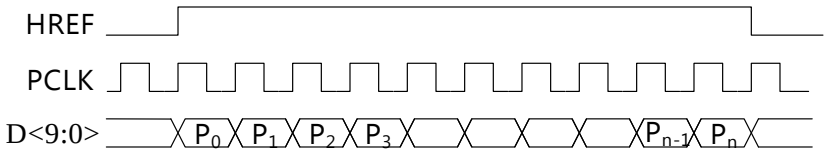
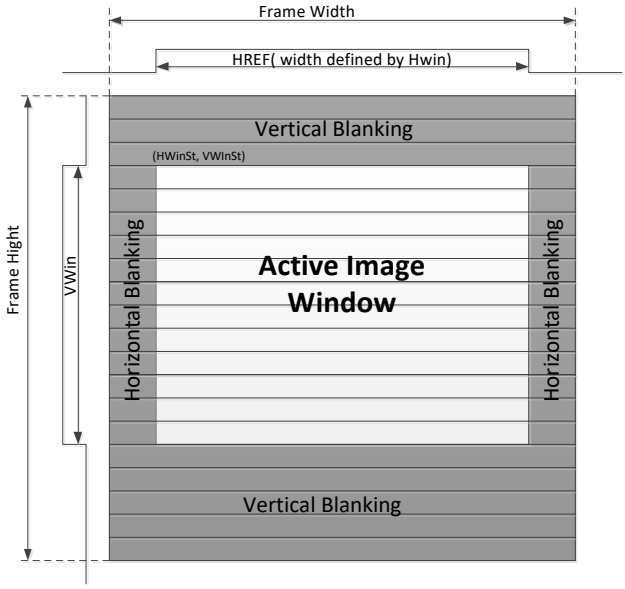


Figure 6: Default frame timing



As shown above in Figure 6, a line (row) period can be calculated as Trow = Frame_width * Thclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-F38P provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, Haddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

HDR mode

JX-F38P support HDR mode, user can set 2 different exposure time and output 2 frame data (long and short exposure) in staggered output mode. Figure 7,8,9 are diagrams to illustrate frame output timing under this mode.

Figure 7: HDR frame timing in DVP output

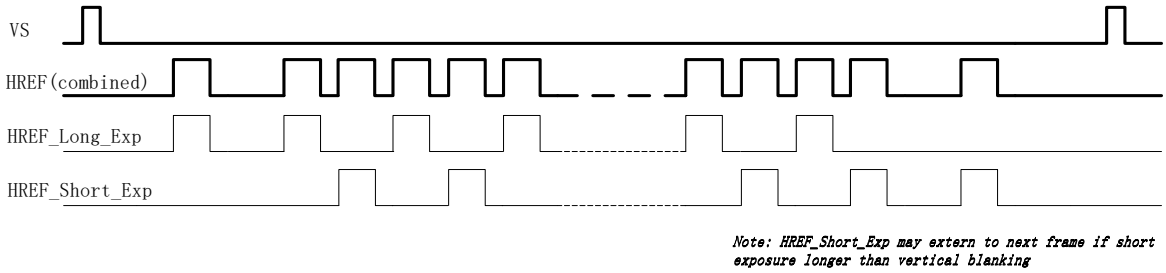


Figure 8: HDR frame timing with VC in MIPI output

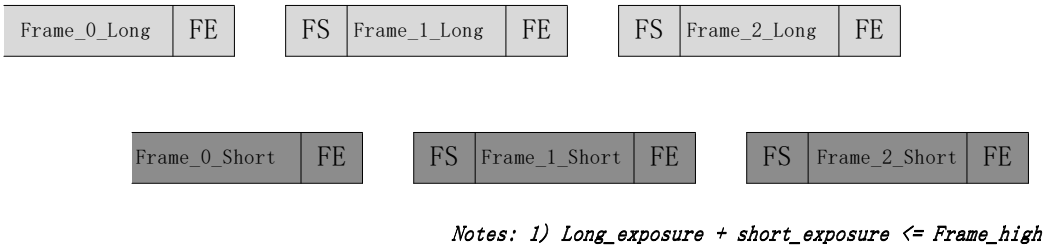
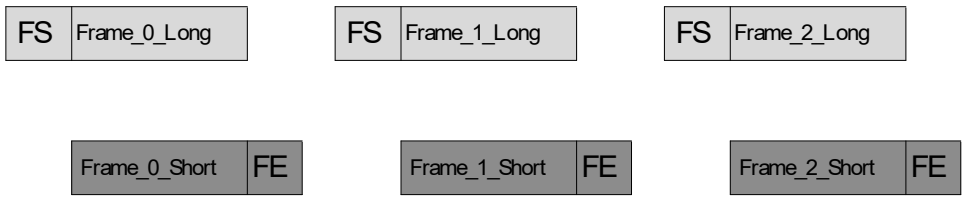


Figure 9: HDR frame timing without VC in MIPI output



Test Pattern Output:

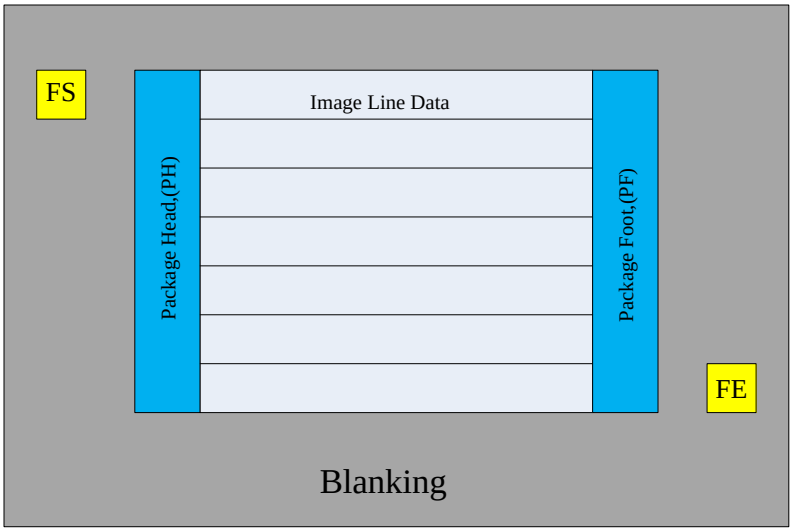
JX-F38P can output following test patterns as described below:

1) Walking “1” test pattern: for most sensor module connectivity test, JX-F38P provides walking “1” test pattern.

MIPI interface:

JX-F38P supports MIPI CSI-2 compliant interface. It has one pair of differential clock lane and two pairs of differential data lane. JX-F38P can output raw8 or raw10 mode through the MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

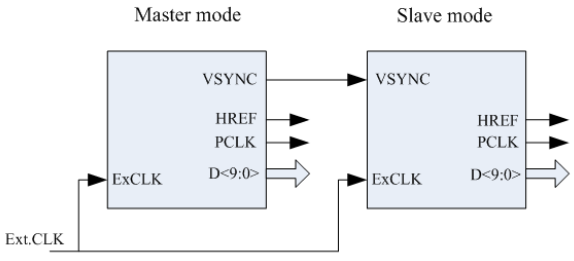
Figure 10: MIPI interface frame timing



Frame Synchronization:

JX-F38P provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-F38P will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 11 shows the ways to realize frame synchronization.

Figure 11: Frame Synchronization illustration



Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock –SCL and Serial Data – SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 12: I2C Timing chart

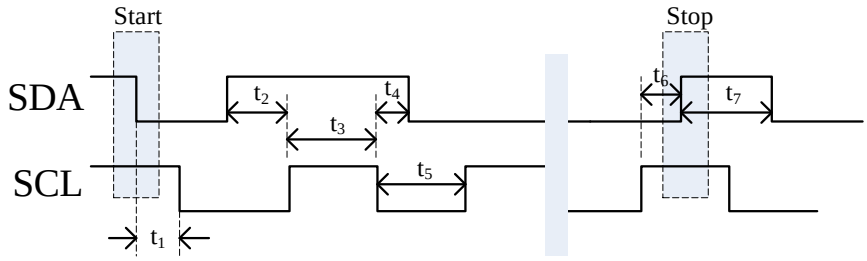


Table 3: I2C timing characteristic

Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0.2	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

Single Write Mode operation

S	Slave-ID	W	A	Address (8bit)	A	DATA	P

Multiple Write Mode (Register address is increased automatically) operation

S	Slave-ID	W	A	Address (8bit)	A	DATA	P	…

…	DATA	A	…	DATA	A	P

Single Read Mode operation

S	Slave-ID	W	A	Address (8bit)	A	P

S	Slave-ID	R	A	DATA	NA	P

Multiple Read Mode (Register address is increased automatically) operation

S	Slave-ID	W	A	Address (8bit)	A	P

S	Slave-ID	R	A	DATA	A	…

…	DATA	A	DATA	NA	P	…

S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition.
JX-F38P slave ID is programmable, default is 0x80/81 for write and read. User can program DVP data bit<1:0> for other configuration. The slave ID program table is list below:

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Register Writing:

In order to avoid register writing process for one frame being split into two frames by mistake, the register writing should be written as early as possible after VYSNC failing edge.

Register Group Write Function:

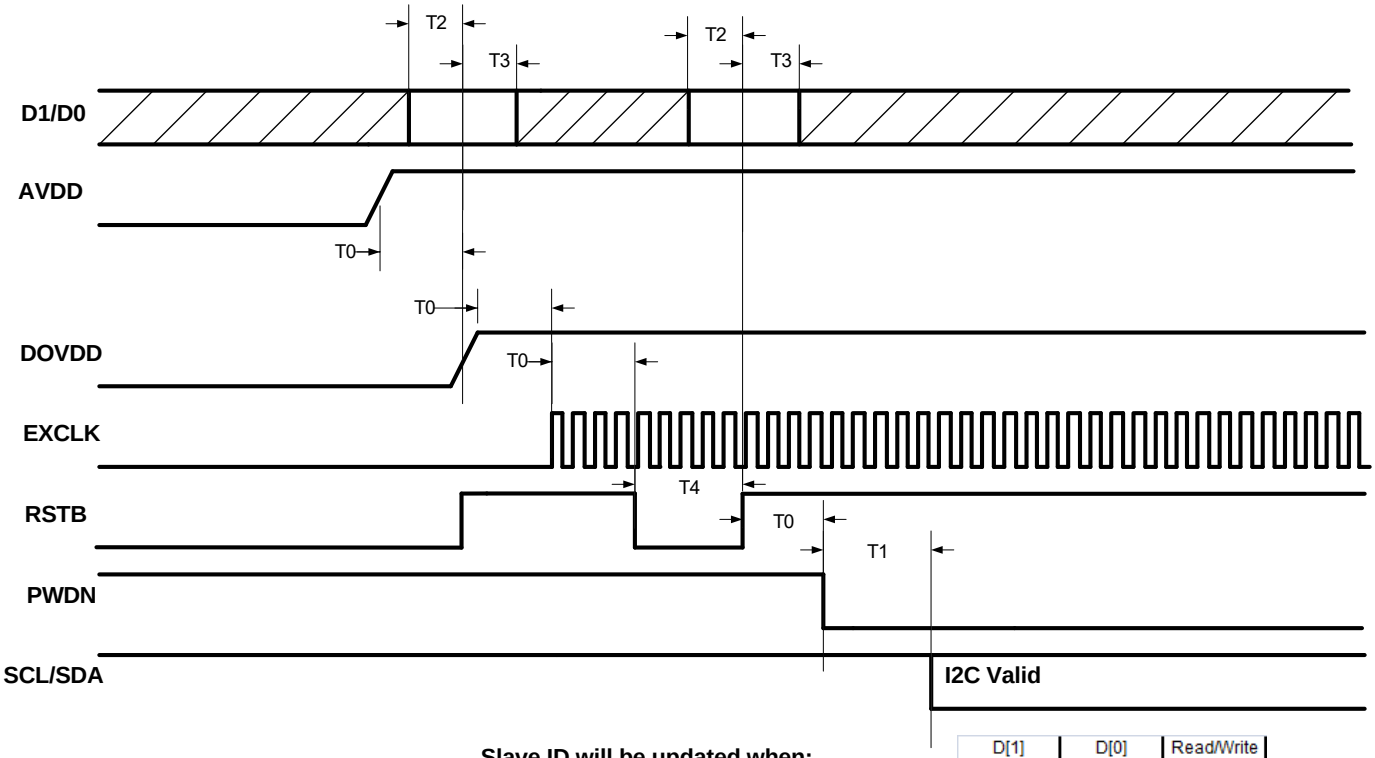
JX-F38P provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-F38P will auto write back group register content at next vertical sync period and reset Reg0x1F[7] JX-F38P can update up to 32bytes of registers.

User can monitor Reg0x1F[7] to make sure group write procedure is finished or not. The monitor I2C read process should not occurs at vertical sync period to prevent conflict with register group write process.

Power on/off sequence:

Figure 13 shows a reference power up sequence of JX-F38P.

Figure 13. Power up sequence for JX-F38P



Note:
1. T0 >= 0 us
2. T1 >= 8192 EXCLK cycles
3. T2>= 1ms
4. T3>= 1ms
5. T4>= 10ms

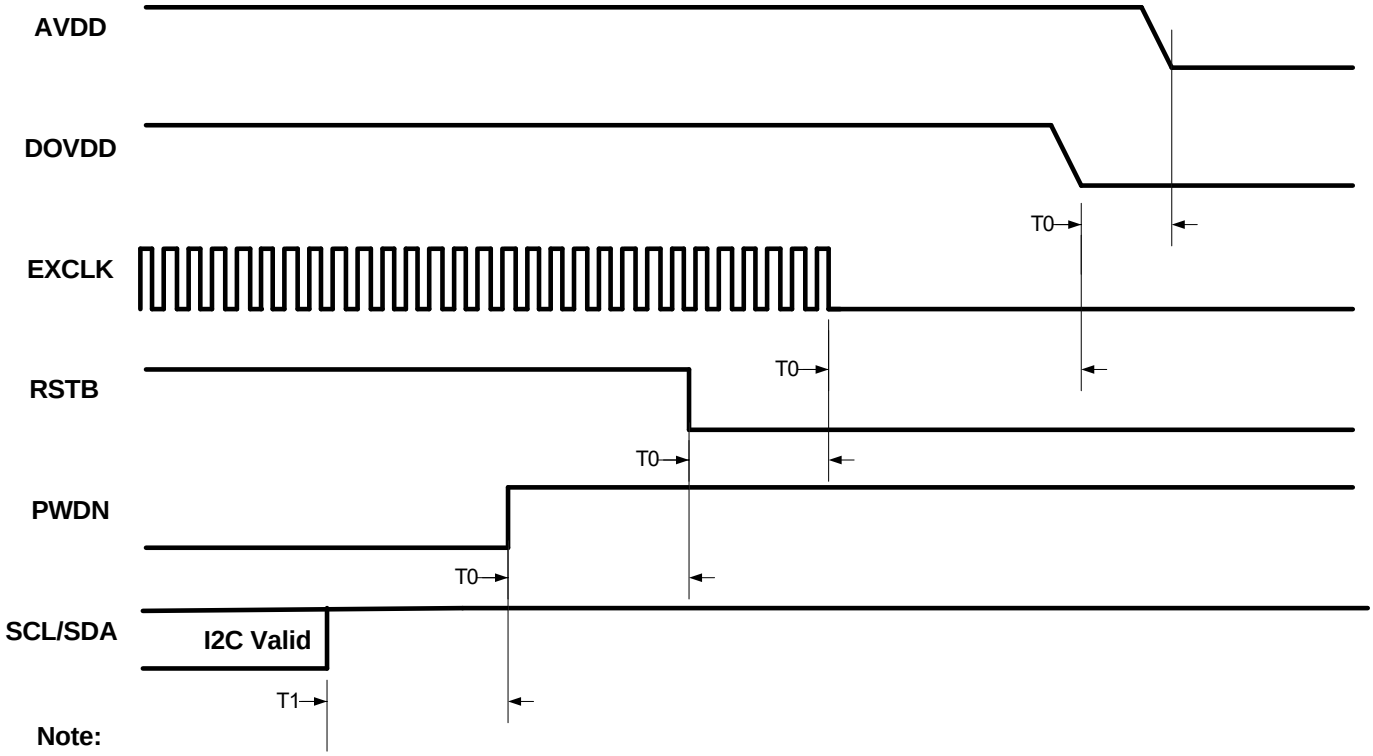
Slave ID will be updated when:
1. Power up (DVDD/DOVDD)
2. Hardware reset pin: Low -> High
3. Software reset : Reg0x12[7]=" 1"

Please stable D1/D0 when issue above commands.

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Figure 14 shows a reference power down sequence of JX-F38P.

Figure 14. Power down sequence for JX-F38P



Note:
1. T0 >= 0 ns
2. T1 >= 512 EXCLK cycle

Electrical Characteristics:

Table 4. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	3.0	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_{AS}	Ambient Storage Temperature	-40 ~ 125	ºC

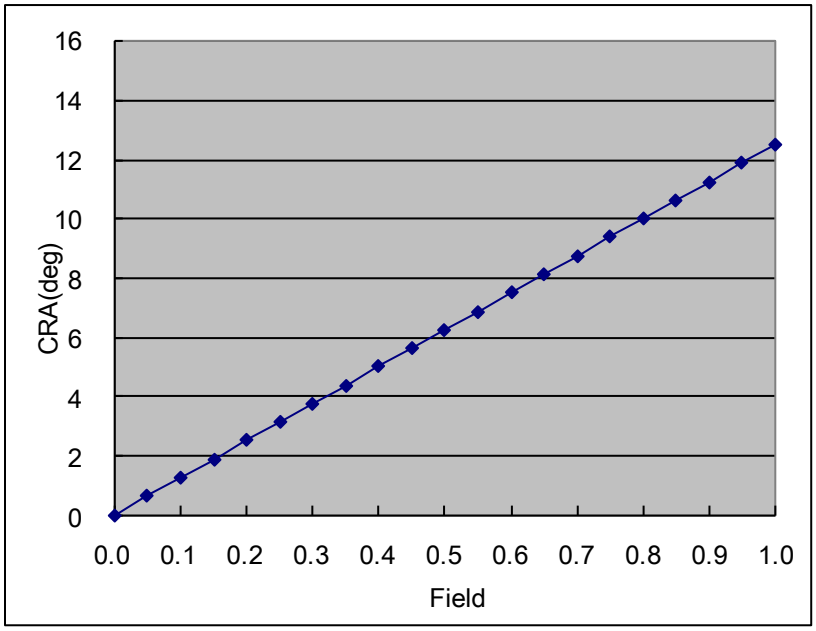
Table 5. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.0	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, MVDD short to DVDD; DVP output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps FHD without digital I/O loading)		25		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps FHD)		21		mA
Power consumption (Internal DVDD, MVDD short to DVDD; MIPI output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps MIPI2L FHD)		28		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps MIPI2L FHD)		21		mA
Ipwrdn	HW PWDN Pin active		300		uA

CRA Specifications:

JX-F38P is designed with a linear chief ray angle curve as shown in Figure 15. The shifting of the color filter and micro lenses on the sensor is critical to accommodate the ever-shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 15. CRA Curve for JX-F38P



Field	CRA
0.00	0.000
0.05	0.625
0.10	1.250
0.15	1.875
0.20	2.500
0.25	3.125
0.30	3.750
0.35	4.375
0.40	5.000
0.45	5.625
0.50	6.250
0.55	6.875
0.60	7.500
0.65	8.125
0.70	8.750
0.75	9.375
0.80	10.000
0.85	10.625
0.90	11.250
0.95	11.875
1.00	12.500

Mechanical Specifications:

JX-F38P is available in CSP packaged component. Figure 16 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip. BGA Center = (-2.505um, 68.27um); Optical Center = (-1.49um, 32.185um);

Figure 16. CSP Top, Bottom, Side View

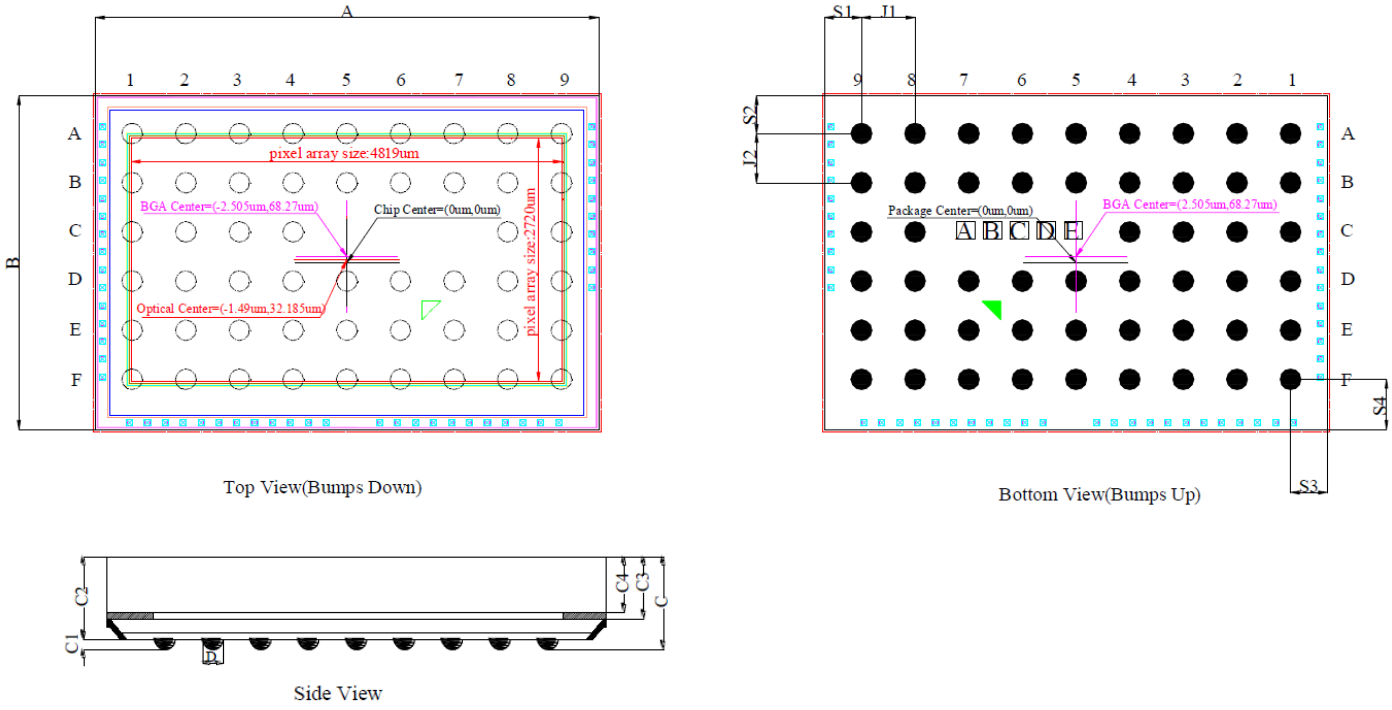
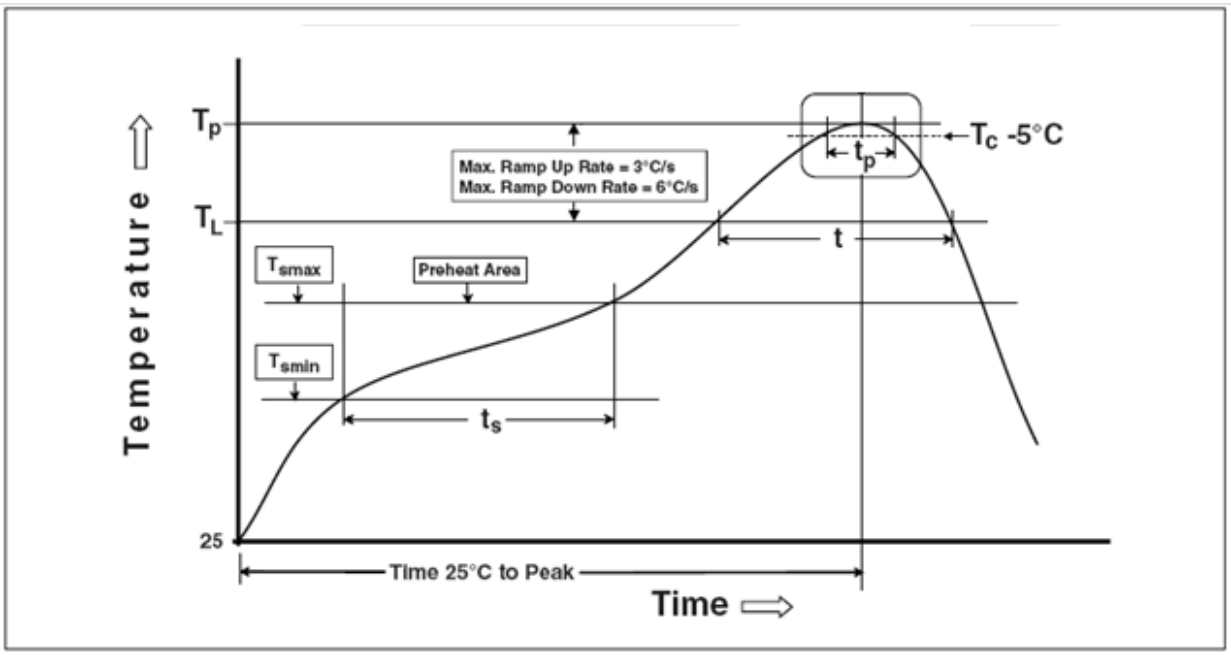


Table 6. Dimensions for JX-F38P CSP package (in mm)

	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	5.626	5.601	5.651	0.22150	0.22051	0.22248
Package Body Dimension Y	B	3.734	3.709	3.759	0.14701	0.14602	0.14799
Package Height	C	0.770	0.710	0.830	0.03031	0.02795	0.03268
Ball Height	C1	0.130	0.100	0.160	0.00512	0.00394	0.00630
Package Body Thickness	C2	0.640	0.605	0.675	0.02520	0.02382	0.02657
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Glass Thickness	C4	0.400	0.385	0.415	0.01575	0.01516	0.01634
Ball Diameter	D	0.230	0.200	0.260	0.00906	0.00787	0.01024
Total Ball Count	N	51					
Pins pitch X axis	J1	0.600					
Pins pitch Y axis	J2	0.550					
Edge to Pin Center Distance along X1	S1	0.415505	0.385505	0.445505	0.01636	0.01518	0.01754
Edge to Pin Center Distance along Y1	S2	0.423730	0.393730	0.453730	0.01668	0.01550	0.01786
Edge to Pin Center Distance along X1	S3	0.410495	0.380495	0.440495	0.01616	0.01498	0.01734
Edge to Pin Center Distance along Y1	S4	0.560270	0.530270	0.590270	0.02206	0.02088	0.02324

IR Reflow:

Recommended IR-reflow profile and condition



Profile Feature	Green Assembly
Preheat & Soak Temperature min (T_{Smin}) Temperature min (T_{Smax}) Time (T_{Smin} to T_{Smax}) (t_S)	 150℃ 200℃ 90-150 seconds (Optimal 100)
Average ramp-up rate(Tsmax to T_P)	3℃/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	217℃ 60-150 seconds (Optimal 120)
Peak package body temperature (T_P)*	240 +/-5℃
Time (t_P) within 5℃ of the specified classification temperature (T_C)	10~30 seconds
Average ramp-down rate (T_P to Tsmax)	6℃/second max.
Time 25℃ to Peak temperature	8 minutes max.

Note:

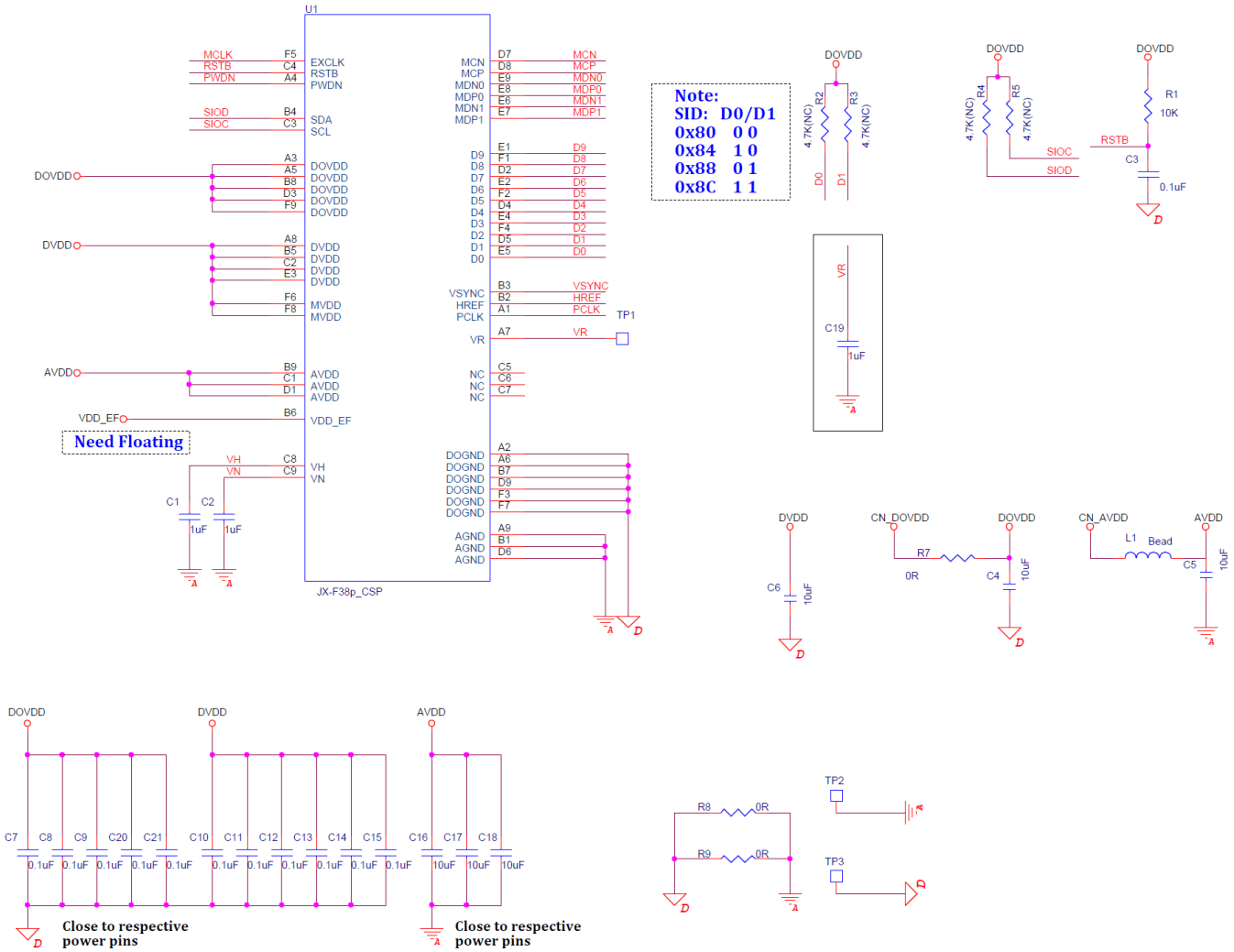
1, Maximum number of reflow cycles=3.

2, N2 gas reflow or control O2 gas ppm<500 as recommendation.

CSP Module Schematic (Reference):

Figure 17 shows reference schematics for CSP module.

Figure 17. Reference schematic for CSP module



Register Descriptions:

I2C Slave ID

The I2C slave ID is selectable by the initial state of pin D[0] and pin D[1].

Pin D[1]	Pin D[0]	Slave ID (Read/Write)
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Sensor ID

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0A	PIDH	08	R	PIDH[7:0]:Product ID MSBs.
0B	PIDL	44	R	PIDL[7:0]: Product ID LSBs.

System Control

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, "1": initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. Default : "0": normal mode SYS[6]: Sleep mode on/off selection, "1": sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. Default : "0" : normal mode SYS[5]: mirror image on/off, "1": mirrored image output, "0": normal image output SYS[4]: flip image on/off, "1": flipped image output, "0": normal image output. SYS[3]: HDR mode on/off selection. "0": normal mode, "1": HDR mode. SYS[1]: vertical skip or full mode selection. "0" : full mode,"1":vertical skip mode SYS[0]: Horizontal down sample mode enable.
65	RAMP3	37	RW	RAMP3 [3:0]: Second stage black sun reference control. Strength: (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
69	PWC3	BB	RW	PWC3[3]: Second stage black sun switch on/off enable, "0": always off. "1": Black sun will switch to second stage when analog gain greater than 2x.
6A	PWC4	1B	RW	PWC4[3:0]: first stage black sun control. Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
80	DigData	01	RW	DigData[7]: frame sync function enable DigData[6]: DVP data output sequence adjustment

AGC and AEC

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 00 to 3F, Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)

01	EXP	1F	RW	Exposure line LSBs, EXP [7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8].; Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Line}

Black Level Control

Address (Hex)	Register Name	Default (Hex)	R/W	Description
49	BLC_TGT	10	RW	Black level calibration target level. BLC_TGT[7]: sign bit."0" positive; "1" negative BLC_TGT[6:0]: target level.
4A	BLCCtrl	05	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10 BLCCtrl[4]: BLC_R bit 10 BLCCtrl[1]: BLC action option. "0": Sensor do BLC only when triggered. "1": always do BLC. BLCCtrl[0]: auto BLC function on/off selection. "0": sensor stop calculate black value. "1": sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}

Frame Size and Window Control

Address (Hex)	Register Name	Default (Hex)	R/W	Description
20	FrameW	00	RW	Sensor frame time width LSBs; FrameW[7:0]
21	FrameW	05	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width
22	FrameH	65	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	04	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	Hwin	C0	RW	Image horizontal output window width LSBs: Hwin[7:0]
25	Vwin	38	RW	Image vertical output window high LSBs: Vwin[7:0]
26	HVWin	43	RW	Image output window horizontal and vertical MSBs. { Vwin[11:8],Hwin[11:8]}

27	HwinSt	A5	RW	Image horizontal output window start position LSBs. HwinSt[7:0]
28	VwinSt	15	RW	Image vertical output window start position LSBs. VwinSt[7:0]
29	HVWinSt	04	RW	Image output window horizontal and vertical start position MSBs. {VwinSt[11:8],HwinSt[11:8]}

DVP Interface

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	DVP1	40	RW	DVP control 1. DVP1[6]: Sensor sun spot elimination control, "1": disable sun spot elimination, "0": enable sun spot elimination. DVP1[5:4]: SRAM read out clock delay control. (after SRAM) DVP1[1:0]: DVP test mode output option. "00": DVP output normal image data. "01": DVP[9:0] = Output 10-bit walk "1" test pattern
0D	DVP2	50	RW	DVP control 2. DVP2[3:2]: PAD drive capability. "00": min, "11": max.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. "1": enable output. "0": tri-state output.
1E	DVP4	10	RW	DVP control 4 DVP4[7]: PCLK polarity control. "0": data output at rising edge of PCLK, "1":data output at falling edge of PCLK DVP4[6]: HREF polarity control. "0": positive, "1": negative DVP4[5]: VSYNC polarity control. . "0": positive, "1": negative DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8] . "1": enable output. "0": tri-state output.

MIPI Interface

Address (Hex)	Register Name	Default (Hex)	R/W	Description
70	Mipi1	C9	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx Mipi1[4:2]: Tck-pre Mipi1[1]: Mipi 8/10 bit mode switch, "0": 10-bit, "1": 8-bit mode
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero Mipi2[4:0]: Tck-zero
72	Mipi3	C8	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare Mipi3[4:0]: Tck-post
73	Mipi4	63	RW	Mipi timing control 4 Mipi4[7]: Mipi pixel clock option Mipi4[6:4]: Ths-trail Mipi4[3:0]: Tck-trail
74	Mipi5	03	RW	Mipi timing control 5 Mipi5[1]: Mipi continues mode or strobe mode selection "1" free run; "0" Normal; Mipi5[0]: Mipi interface sleep on/off Mipi should wait a complete frame than enter sleep mode. "1" Sleep mode enable; "0" Normal;

75	Mipi6	2B	RW	Mipi data type ID;
76	Mipi7	40	RW	Mipi word count LSBs
77	Mipi8	0B	RW	Mipi word count MSBs

HDR

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	SYS	00	RW	SYS[3]: HDR mode on/off selection. “0”: normal mode, “1”: HDR mode.
05	SAEC0	1F	RW	Short exposure lines in HDR mode, SAEC[7:0]: LSB of short exposure lines in HDR mode, each bit equals to 1 lines.
06	SFramSt	1F	RW	SFramSt [7:0]:Short exposure frame start position in HDR mode ; each bit equals to 2 lines, short exposure packet start at SFramSt *2 + 1 lines relate to long exposure packet.
08	SAEC1	00	RW	SAEC1 [0]: SAEC[8] MSB of short exposure lines in HDR mode, with Reg05.

I2C Group Write

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	GLat	00	RW	Group latch control Glat[7]: Group write trigger. “1”: system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. “0”: inactive group write function.
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.1	Sep 14,2021	Initial release of JX-F38P preliminary datasheet
R1.0	Mar 10,2022	Update key spec, power consumption info.