Applications Note:SY5850D/E

Single Stage Controller
For Dimmable LED Lighting
Preliminary datasheet

General Description

SY5850D/E is a controller for Buck-Boost/Flyback topology targeting at LED lighting applications.

It is compatible with leading edge/trailing edge/no dimmer application. It adopts proprietary techniques to identify different type dimmers and achieve excellent compatibility.

High power factor can be achieved without any dimmer. Quasi-resonant valley turned-on is adopted for high efficiency operation. Reliable short/open LED protection are integrated

Ordering Information

SY5850 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5850DFHC	SSOP10	----
SY5850EFHC	SSOP10	----

Features

- Excellent compatibility with different dimmer
- Excellent compatibility for low power application
- Fast start up, <500ms
- QR-mode operation for high efficiency
- High power factor, PF>0.9 without dimmer
- Reliable short/open LED protection
- Package SSOP10

Applications

- LED lighting with leading edge/trailing edge/no dimmer
- Option Specification

SY5850D	for high power application
SY5850E	for low power application

Typical Applications

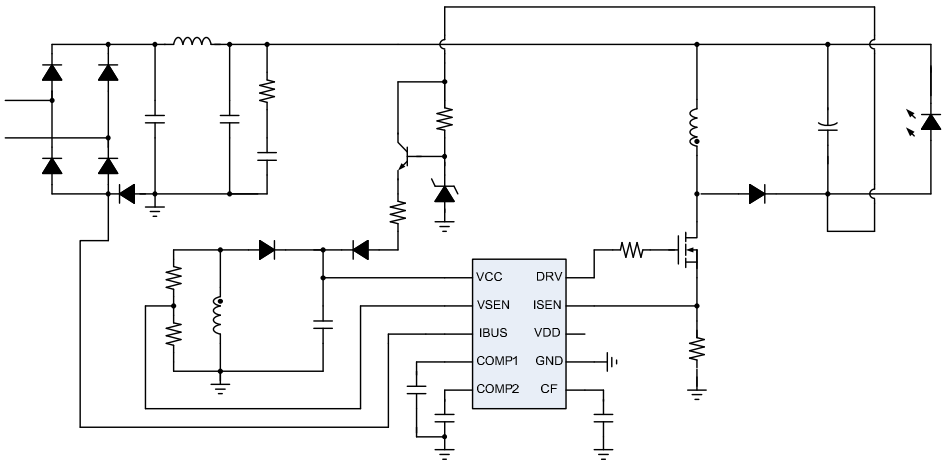


Figure 1. Buck-Boost Topology

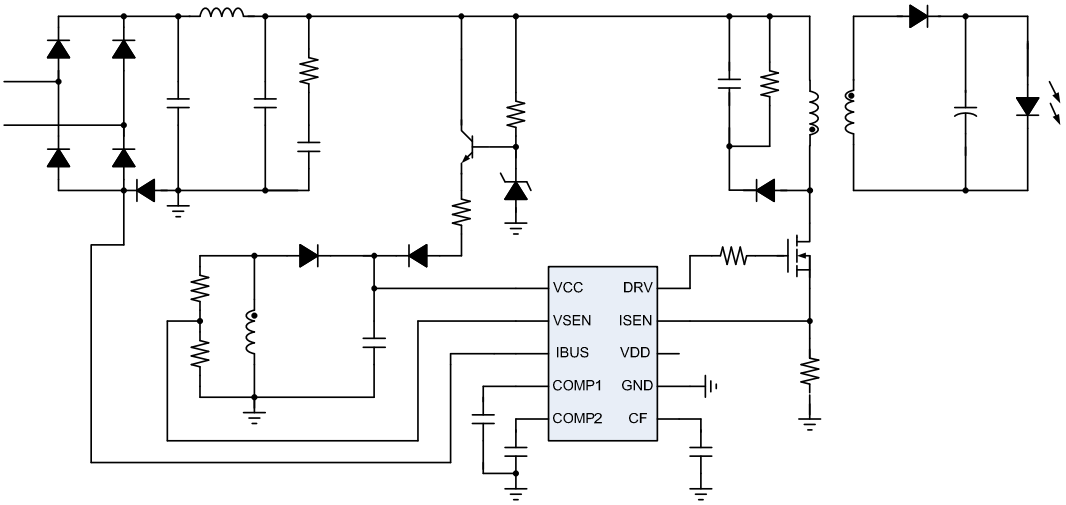
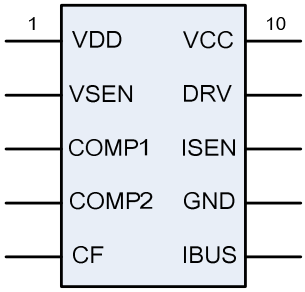


Figure 2. Flyback Topology

Pinout (top view)



(SSOP10)

Top Mark: BCSxyz for SY5850D (device code: **BCS**, ***x=year code, y=week code, z= lot number code*****)**
BCTxyz for SY5850E (device code: **BCT**, ***x=year code, y=week code, z= lot number code*****)**

Pin number	Pin Name	Pin Description
1	VDD	Internal bias voltage output pin. This pin is left outside for fine tune on compatibility
2	VSEN	Connect this pin to resistor divider on aux-winding: Inductor current zero-crossing detection; Output voltage sense for logic control and OVP; Inductor voltage valley detection; Dimmer type detection.
3	COMP1	Connect a capacitor to this pin: Feedback loop control for positive half
4	COMP2	Connect a capacitor to this pin: Feedback loop control for negative half
5	CF	Connect a capacitor to filter out conduction angle information
6	IBUS	Input current detection pin. In leading mode, holding current control when the dimmer is ON and re-fire control when the dimmer is OFF; In trail mode, detect dimmer OFF to adjust BUS voltage to improve the compatibility.
7	GND	Ground pin
8	ISEN	Current sense pin for output current regulation. Connect this pin to current sense resistor
9	DRV	Gate driver of MOSFET
10	VCC	Bias supply for IC

Absolute Maximum Ratings (Note 1)

VCC ---------- -0.3V~26V
I_{VCC} ---------- 10mA
DRV ---------- -0.3V~VCC
VSEN ---------- -0.3V~30V
IBUS ---------- -0.6V~0.6V
COMP1, COMP2, VDD, CF, ISEN ---------- -0.3V~3.6V
Power Dissipation, @ TA = 25°C SSOP10 ---------- 1.1W
Package Thermal Resistance (Note 2)
SSOP10, θ_{JA} ---------- 88°C/W
SSOP10, θ_{JC} ---------- 45°C/W
Maximum Junction Temperature ---------- 160°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Junction Temperature Range ---------- -40°C to 150°C
Storage Temperature Range ---------- -65°C to 150°C

Block Diagram

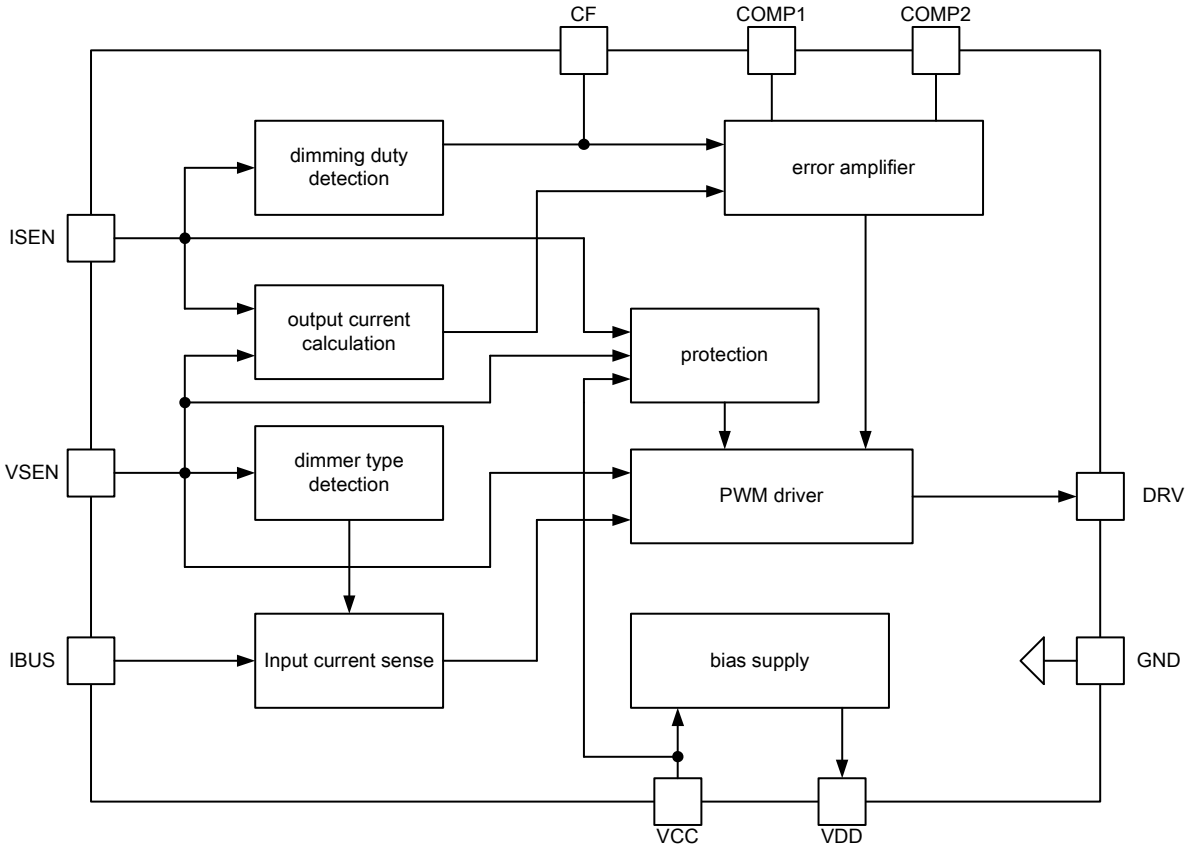


Figure3. Block Diagram

Electrical Characteristics

(V_{VCC} = 15V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power supply section						
VCC turn-on threshold	$V_{VCC,ON}$			10		V
VCC turn-off threshold	V_{VCCOFF}			7		V
VCC OVP voltage	$V_{VCC,OVP}$			22		V
Start up current	I_{ST}	$V_{VCC}<V_{VCC,OFF}$		15		μA
Operation current	I_{OP}	C_L=1nF, f=40kHz, I_{VDD}=0		1		mA
Shunt current in OVP mode	$I_{VCC,OVP}$	$V_{VCC}>V_{VCC,OVP}$		5		mA
VDD section						
Output voltage	V_{VDD}			3		V
Source current	I_{VDD}				1	mA
Current feedback modulator section						
Internal reference voltage	V_{REFI}			300		mV
ISEN pin Section						
Current limit Voltage	$V_{ISEN,LIM}$			0.4		V
CC feedforward coefficient	K_2			0.1		
CC feedforward resistor	R_{k2}			110		Ω
Blanking time for ON time	$t_{ON,MIN}$			800		ns
Limit for conduction angle detection	$V_{ISEN,A}$			50		mV
VSEN pin Section						
OVP voltage threshold	$V_{VSEN,,OVP}$			1.5		V
Fast start up threshold	$V_{VSEN,ST}$			0.6		V
Blanking time for OFF time	$t_{OFF,MIN}$			2		μs
Current error threshold for leading edge dimmer detection	$I_{FFV,E}$			200		μA
PWM output section						
Gate driver voltage	V_{DRV}			12		V
source current	I_{SOURCE}			60		mA
sink current	I_{SINK}			250		mA
Max ON Time	$t_{ON,MAX}$	Option D, dimmer ON/OFF		12/12		μs
		Option E, dimmer ON/OFF		6/6		
Max OFF Time	$t_{OFF,MAX}$	dimmer ON/OFF		150/6		μs
Minimum switch period	$t_{S,MIN}$			5		μs
IBUS section						
Threshold1 in leading mode	I_{IBUS1}			30		mA
Threshold2 in leading mode	I_{IBUS2}			200		μA
Threshold3 in trailing mode	I_{IBUS3}			22		mA
Maximum operation time with holding current each cycle in leading mode	t_{OP}	Option E		4		ms
		Option D		10		ms
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

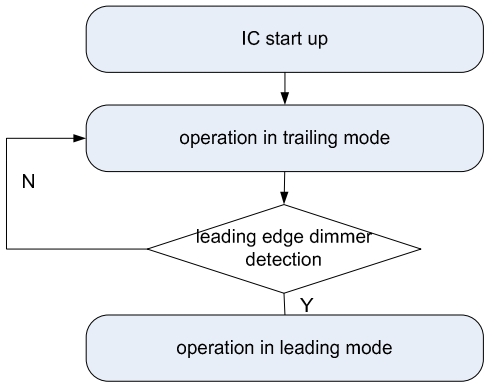
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn to 10V.

Operation

Operation flow

SY5850D/E provides different operation modes for different dimmer types.



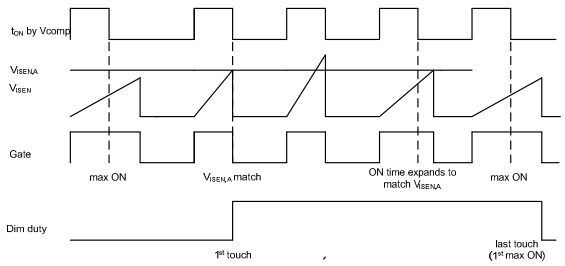
Trailing mode:

SY5850D/E detects the ON/OFF information of dimmer, and discharges the input capacitor quickly when dimmer OFF is detected, which ensures the compatibility for trailing edge dimmer.

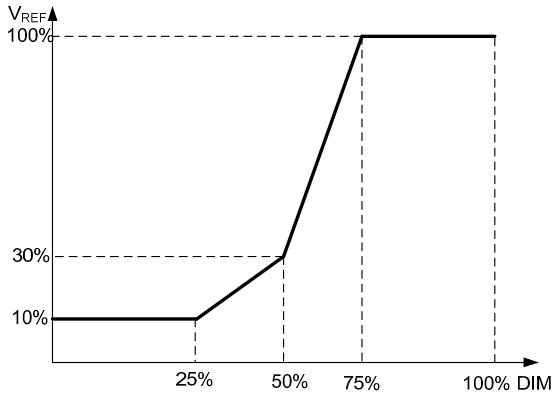
Leading mode:

SY5850D/E guarantees the input current higher than the holding current of leading edge dimmer. To achieve low power application, active shut down function is added on option E.

Conduction angle detection



The threshold $V_{ISEN,A}$ on ISEN pin is applied to detect the conduction duty. t_{ON} is controlled by V_{COMP} generally to achieve high PF, which is relatively stable. If V_{ISEN} cannot reach $V_{ISEN,A}$ by V_{COMP}, t_{ON} will expand to reach $V_{ISEN,A}$ till max t_{ON}. When V_{ISEN} is higher than $V_{ISEN,A}$, dimmer ON is identified; when V_{ISEN} is lower than $V_{ISEN,A}$, although max t_{ON} is output, dimmer OFF is identified. The dim duty is transferred to output current by the curve below.



Dimming Curve (V_{REF} vs DIM)

Dimmer Type Detection

The input BUS voltage information is detected by VSEN when the MOSFET is ON.

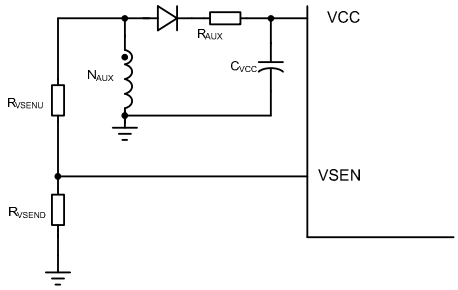


Fig. voltage detection and feedback

When the MOSFET is ON, VSEN pin is clamped to zero internally, the current sourcing from VSEN to the auxiliary winding is proportional to BUS voltage, which is named as I_{FFV}.

$$I_{FFV} = V_{BUS} \cdot \frac{N_3}{N_1} \cdot \frac{1}{R_{VSENU}}$$

I_{FFV} is sampled and hold each switching cycle. If current I_{FFV} is larger than the last switching cycle by $I_{FFV,E}$, which is taken as sharp rising slope, the leading edge dimmer is detected. After start up, IC operates in trailing mode initially; once leading edge dimmer is detected, it enters into leading mode and latches the leading mode.

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN-ON}, the internal blocks start to work and PWM output is enabled.

The output voltage is feedback by VSEN pin, which is taken as V_{FB}. If V_{FBV} is lower than certain threshold $V_{VSEN,ST}$, which means the output voltage is not built up, V_{COMP} is pulled up to high clamped; if V_{FBV} is higher than $V_{VSEN,ST}$, V_{COMP} is under charge of the internal gain modulator.

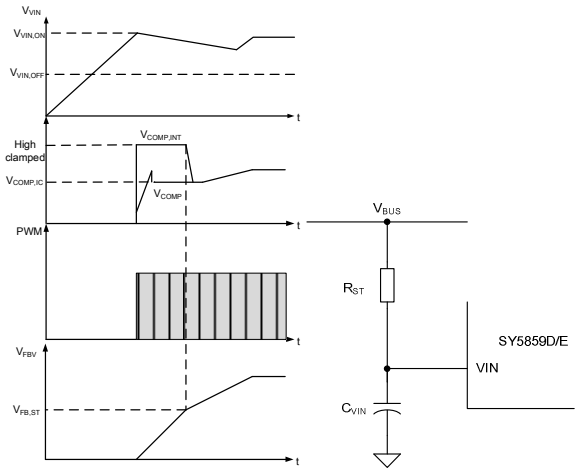


Fig. Start up

This operation is aimed to build up enough output voltage for auxiliary winding bias supply as quickly as possible. It is enabled only one time just when V_{VIN} is over $V_{VIN,ON}$.

V_{COMP} is pre-charged by internal current source to $V_{COMP,IC}$ and hold at this level until fast start up process is finished.

The startup resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN-OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Primary-side constant-current control

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler, which reduces the circuit cost. The switching waveforms are shown in blow.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S}$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of Flyback transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

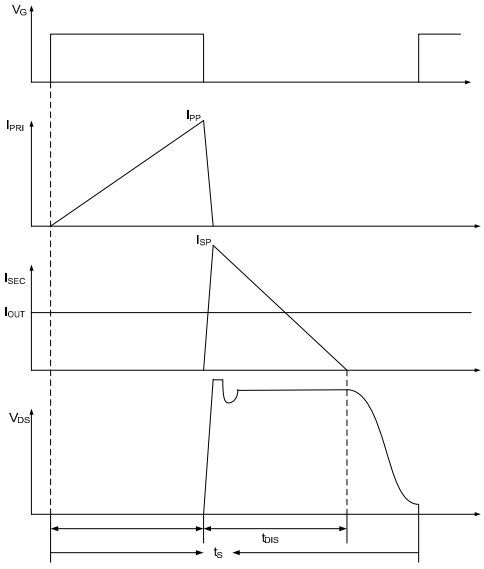


Fig. switching waveforms

$$I_{SP} = N_{PS} \times I_{PP} \quad (4)$$

Where N_{PS} is the turns ratio of primary to secondary of the Flyback transformer.

Thus, I_{OUT} can be represented by

$$I_{OUT}=\frac{N_{PS}\times I_{PP}}{2}\times\frac{t_{DIS}}{t_S}$$

The primary peak current I_{PP} and inductor current discharge time t_{DIS} can be detected by Source and VSEN pin, which is shown in blow. These singals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal

$$V_{REF}=I_{PP}\times R_S\times\frac{t_{DIS}}{t_S}\times k_1$$

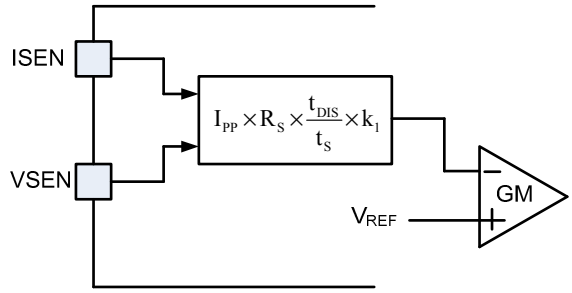


Fig. Output current detection diagram

Finally, the output current I_{OUT} can represented by

$$I_{OUT}=\frac{V_{REF}\times N_{PS}}{R_S\times 2\times k_1}$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1=3, and V_{REF} are all internal constant parameters, I_{OUT} can be programmed by N_{PS} and R_S.

$$R_S=\frac{V_{REF}\times N_{PS}}{I_{OUT}\times 2\times k_1}$$

then

$$R_S=\frac{k\times V_{REF}\times N_{PS}}{I_{OUT}},\ k=\frac{1}{2k_1}$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Buck-boost/Flyback converter.

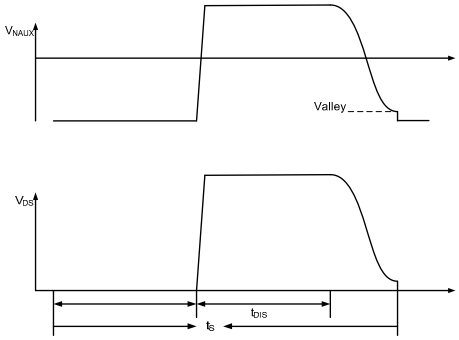


Fig. QR mode operation

The voltage across drain and source of the MOSFET is reflected by the auxiliary winding of the transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the MOSFET is at voltage valley, the MOSFET would be turned on.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

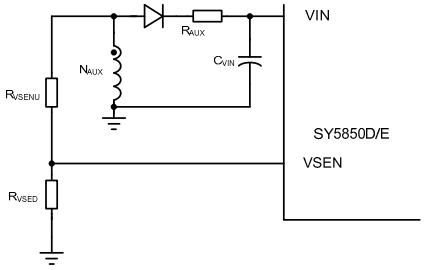


Fig. OVP&OLP

The output voltage is reflected by the auxiliary winding voltage of the Flyback transformer, and both VSEN pin and VIN pin provide over voltage protection function. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VIN} exceeds $V_{VIN,OVP}$ or V_{VSEN} exceeds $V_{VSEN,OVP}$, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source $I_{VIN,OVP}$. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{SEN\_OVP}}{V_{OVP}}=\frac{R_{VSEND}}{R_{VSENU}+R_{VSEND}}$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}} \geq \frac{N_{AUX}}{N_S}$$

Where V_{OVP} is the output over voltage specification; R_{VSENU} and R_{VSEND} compose the resistor divider. The turns ratio of N_S to N_{AUX} and the ratio of R_{VSENU} to R_{VSEND} could be induced from equation above.

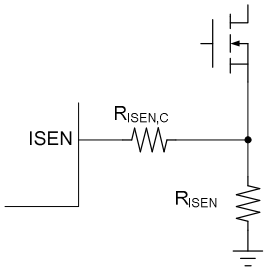


Fig. feed-forward resistor

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned ON until maximum off time $t_{OFF,MAX}$ is matched. If MOSFET is turned ON by $t_{OFF,MAX}$ 64 times continuously, IC will be shut down and enter into hiccup mode.

If the output voltage is not low enough to disable valley detection in short condition, V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Line regulation modification

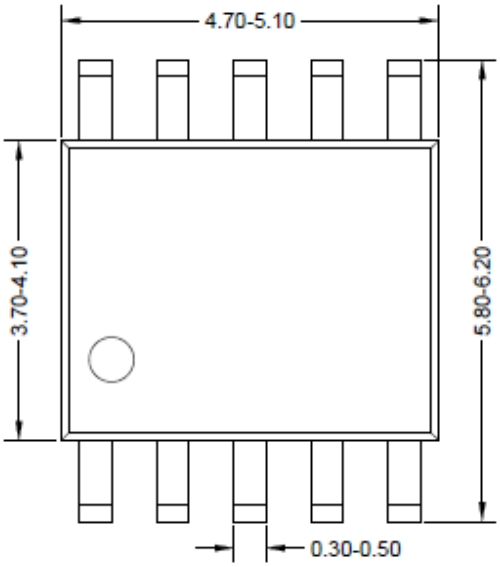
The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage $\Delta V_{ISEN,C}$ is added to ISEN pin during ON time to improve such performance. This $\Delta V_{ISEN,C}$ is adjusted by the upper resistor of the divider connected to VSEN pin.

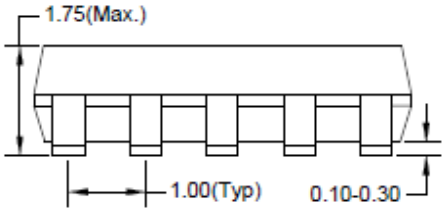
$$\Delta V_{ISEN,C} = (V_{BUS} - V_{OUT}) \times \frac{N_{AUX}}{N} \times \frac{1}{R_{VSEN,U}} \times K_2 \times (R_{K2} + R_{ISEN,C})$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient; R_{k2} is an internal feed-forward resistor; auxiliary resistor $R_{ISEN,C}$ can be added to enhance feed-forward effects.

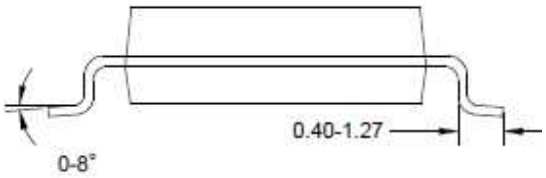
SSOP10 Package outline



Top view



Side view A



Side view B

Notes: **All dimension in MM and exclude mold flash & metal burr.**