GENERAL DESCRIPTION

OB3674x is an active transition-mode (TM) power factor correction (PFC) switch for AC-DC switching mode power supply applications.

OB3674x build-in a demagnetization detector to ensure TM operation, a current sensing comparator with built-in leading-edge blanking, and an input voltage sense block to automatically set follow output voltage.

OB3674x offers great protection coverage including system over-voltage protection (OVP) to eliminate runaway output voltage due to load removal, VDD under voltage lockout (UVLO), cycle-by-cycle current limiting, Inductor short protection (ISP).

With added system open loop protection feature, OB3674x shuts down system when the feedback loop is open.

OB3674x is offered in SOP7 and ASOP6 package.

FEATURES

- Follower or constant boost structure with single winding PFC inductor
- Standby power loss <300mW
- Dynamic output over voltage protection< 8%
- High power factor (PF>0.95)
- THD <10%
- High precise constant voltage
- Inductor short protection
- Open loop protection
- OTP
- Fast start-up (<0.5s)
- Cycle by cycle current limit (OCP)

APPLICATIONS

- LED lighting
- AC-DC SMPS

TYPICAL APPLICATION

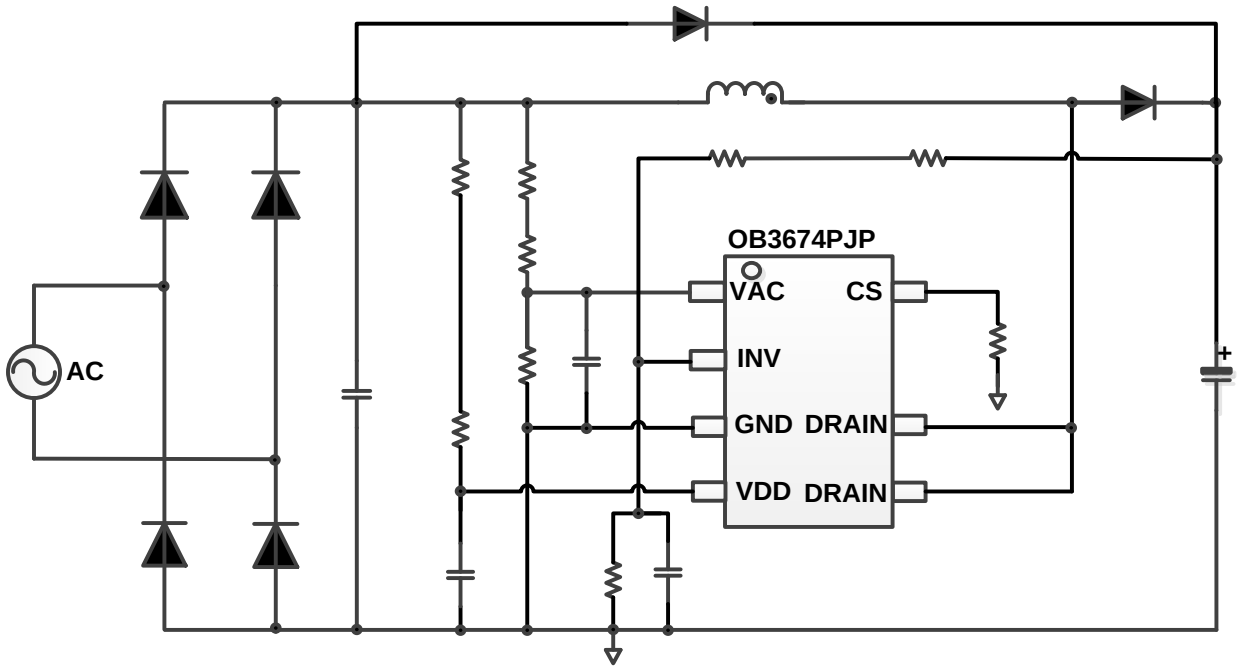


Figure1: OB3674PJP Typical Application Schematic

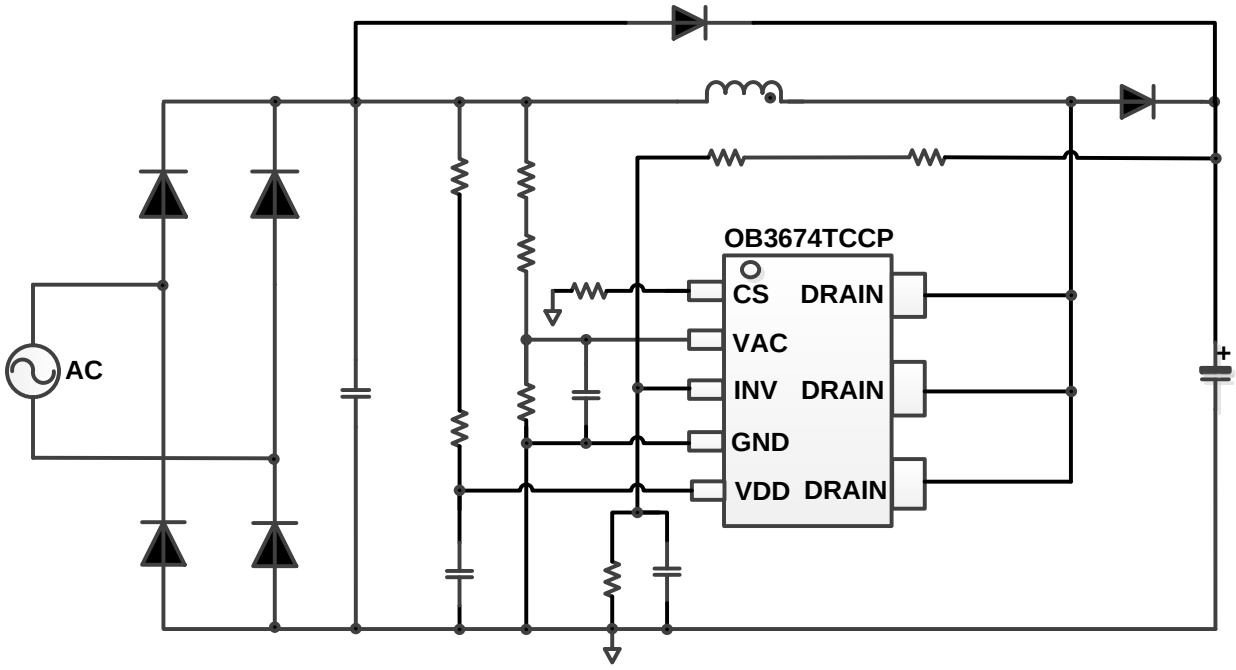
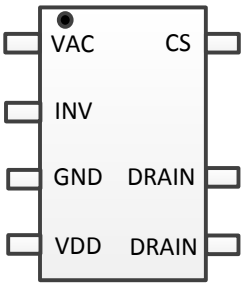


Figure2: OB3674TCCP Typical Application Schematic

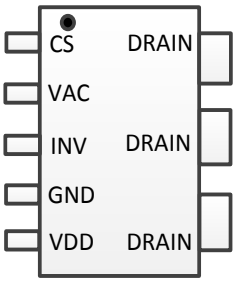
GENERAL INFORMATION

Terminal Assignment

The pin map is shown as below for SOP7.



The pin map is shown as below for ASOP6.



Ordering Information

Part Number	Description
OB3674PJP-J	SOP7, Halogen-free in Tube
OB3674PJPA-J	SOP7, Halogen-free in T&R
OB3674TCCP-J	ASOP6,Halogen-free in Tube
OB3674TCCPA-J	ASOP6,Halogen-free in T&R

Package Dissipation Rating

Package	RθJA (℃/W)
SOP7	95
ASOP6	73

Absolute Maximum Ratings

Symbol	Parameter	Value
VDD	DC Supply Voltage	-0.3 to 30 V
DRAIN	DRAIN Voltage	-0.3 to DRAIN_BV
INV/VAC/CS	Analog Inputs & Outputs	-0.7 to 7V
Tj	Min/Max Operating Junction Temperature	-40 to 150℃
T_A	Operating Ambient Temperature	-20 to 85℃
Tstg	Min/Max Storage Temperature	-55 to 150℃
Lead Temperature	(Soldering, 10secs)	260℃

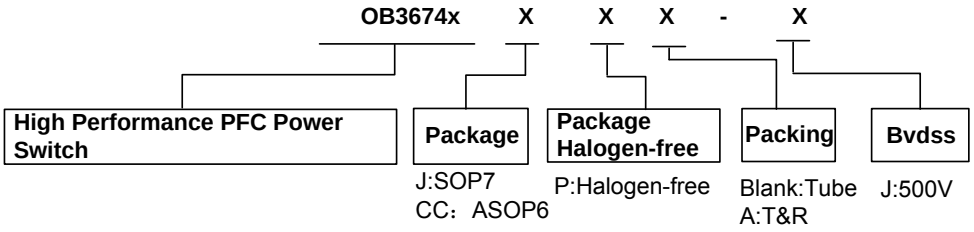
Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

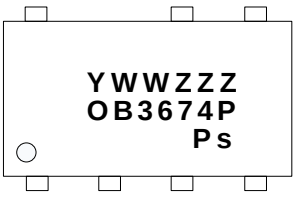
Output Power Table

Product	176Vac~264Vac Input
OB3674PJP-J	44W
OB3674TCCP-J	60W

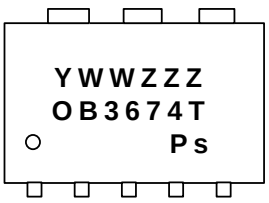
Note: Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50℃ ambient and 60℃ temperature rise.
Higher output power is possible with extra added heat sink or air circulation to reduce thermal resistance.

Marking Information





Y: Year Code
WW: Week Code (01-52)
ZZZ:Lot Code
P:Halogen-free Package
S: Internal Code(Optional)

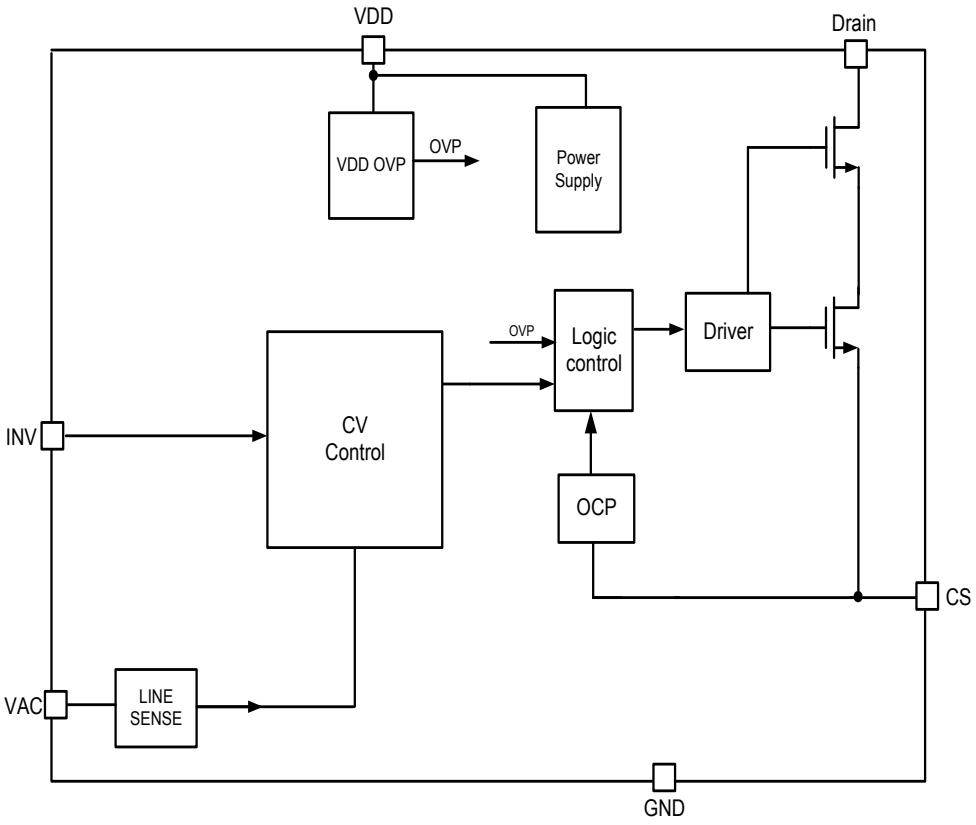


Y: Year Code
WW: Week Code (01-52)
ZZZ:Lot Code
P: Halogen-free Package
s: Internal Code

TERMINAL DESCRIPTIONS

Pin Num （PJP）	Pin Num （TCCP）	Pin Name	I/O	Description
1	2	VAC	O	Boost mode set pin. Connect to resistor divider from system input for follower boost mode or floating for constant boost mode.
2	3	INV	I	Inverting input of Error Amplifier. Connect to resistor divider from system output.
3	4	GND	P	Ground Pin.
4	5	VDD	P	DC supply voltage.
5,6	6	DRAIN	O	Drain of power MOSFET.
7	1	CS	I	Current sense input Pin.

BLOCK DIAGRAM



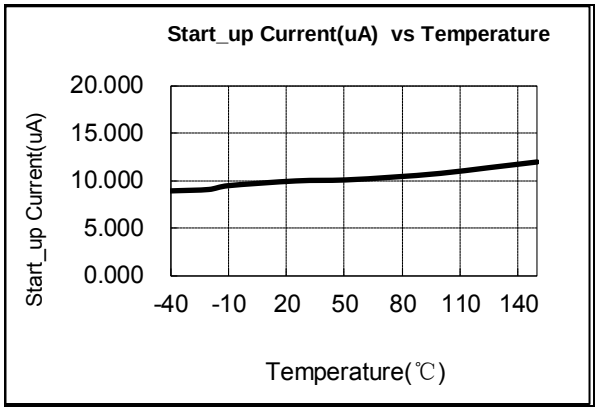
ELECTRICAL CHARACTERISTICS

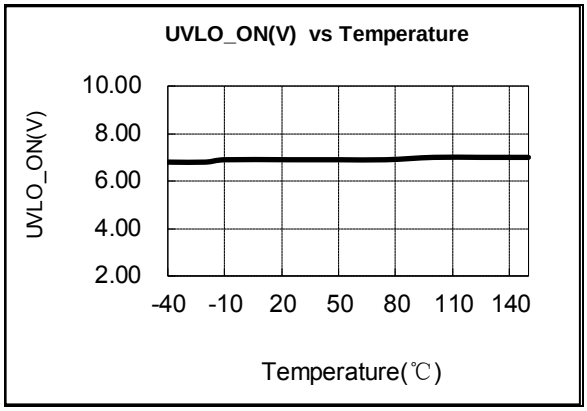
(T_A = 25℃ VDD= 12V if not otherwise noted)

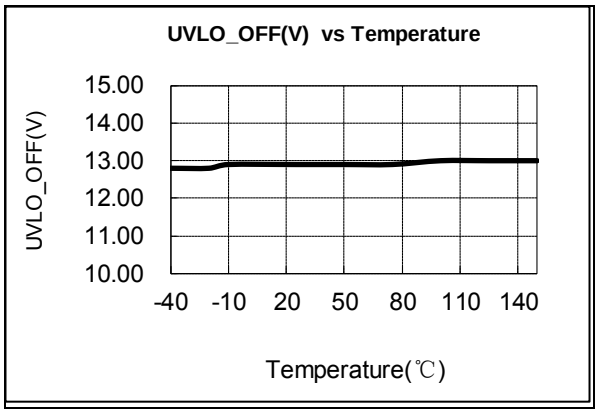
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD) Section						
Ist	Start-up current	VDD=UVLO_OFF-1V			13.5	uA
I_{OP}	Static current	VDD=14V		550	700	uA
UVLO(ON)	VDD under voltage lockout enter	VDD falling	6	6.8	7.6	V
UVLO(OFF)	VDD under voltage lockout exit	VDD rising	11.6	12.8	14	V
Vdd_clamp	VDD clamp			17		V
CV Section						
Frequency range	Clamped high operational frequency			230		KHz
	Clamped low operational frequency			25		KHz
Max-off time		1V>CS>0.125V		150		uS
		CS>1V		450		uS
		CS<0.125V		20		uS
Max-on time				30		uS
Vth_dch	Dynamic OVP		2.565	2.7	2.835	V
Vth_follower	Follower reference	VAC=2.28V	2.45	2.5	2.55	V
Vth_cv_up_clamp	Up clamp threshold voltage of CV	VAC=3V	2.45	2.5	2.55	V
Min_off	Min off time	CS>100mV		1.2		us
		CS<100mV		0.7		us
Vth_ol	Threshold voltage of open loop			0.3		V
Thermal section						
OTP	OTP ON			165		℃
OTP_recover	OTP OFF			115		℃
CS Section						
Vth_ocp	Over current threshold		0.585	0.65	0.715	V
Vth_isp	Inductor short threshold			1		V

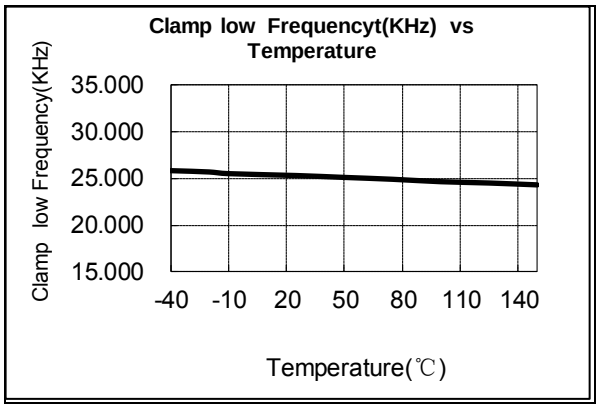
Product \ Parameter	**DRAIN_BV (V)** DRAIN-CS Breakdown Voltage		
	Min	Typ.	Max
OB3674PJP-J	530		
OB3674TCCP-J	530		

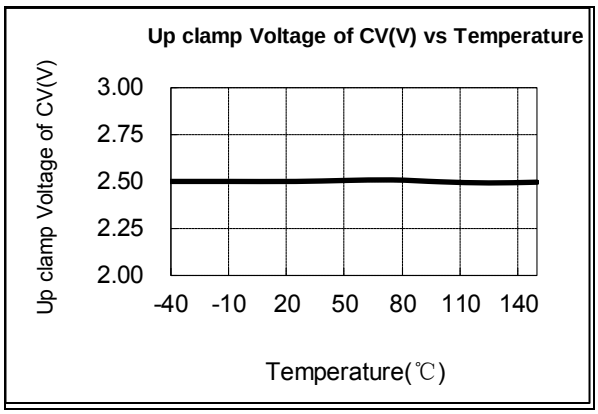
CHARACTERIZATION PLOTS

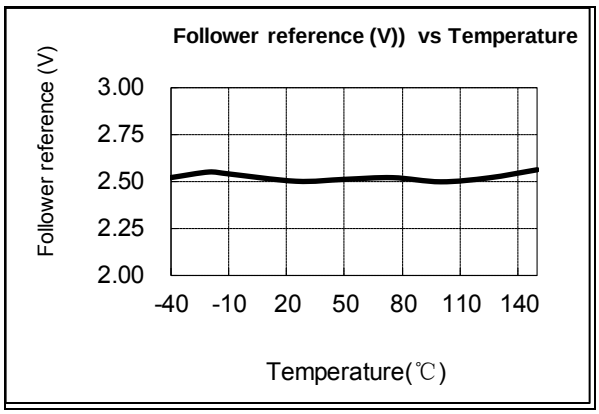












OPERATIONAL DESCRIPTION

OB3674x is an active transition-mode (TM) power factor correction (PFC) switch. The transition mode control greatly reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

- **Start up**

Startup process is realized by charging VDD capacitor. When VDD voltage reaches up to UVLO (OFF), the system starts to operate. A 17V (typical) clamp circuit is applied to clamp VDD voltage. The typical startup current of OB3674x is 10uA. An internal VDD power supply unit is integrated in OB3674X. After startup, if the voltage of VDD lowers than 14V, VDD power supply unit charges up the VDD voltage automatically.

- **Output Voltage Follower**

OB3674x build-in line sense unit and Constant Voltage (CV) unit to provide output voltage follower function. A resistor divider is connected to VAC pin between input line and GND, using to detect the voltage of input line. The line sense unit samples the peak of voltage of VAC to provide a follower reference voltage Vac_pk. INV pin is connected to a resistor divider from output line. The voltage of INV is compared to Vac_pk+0.22V to regulate the output voltage in internal CV unit.
Refer to the equation 1, output voltage is

$$\text{Voutput} = k \times (\text{Vac\_pk} + 0.22\text{V}) \quad (1)$$

Where, k is the radio of INV dividing resistor. Vac_pk is clamped up at 2.28V and is clamped down at 1.105V.
If VAC pin is floating, Vac_pk is set at 2.28V constantly and output voltage follower function is disabled.

- **Dynamic Output Over Voltage Protection**

The Dynamic OVP is designed in OB3674x for output fast transient protection. When the output voltage exceeds the value which correspond to an INV voltage larger than 1.08*(Vac_pk+0.22V), the GATE output is turned off and OB3674x is disabled. When INV voltage reach below 1.04*(Vac_pk+0.22V), the operation of OB3674x is resumed.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting (OCP) is offered in OB3674x. The current is detected by a sense resistor connected between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to wheel diode reverse recovery. The current limiting comparator is disabled at this blanking time and thus the MOSFET cannot be turned off during this blanking time.

- **Protection Controls**

OB3674x ensures good reliability design through its good protection coverage. Output dynamic and static over-voltage protection (OVP), VDD under voltage lockout (UVLO) , System open protection (SOP), cycle-by-cycle current limiting, Inductor short protection (ISP) and output gate clamp are standard features provided by OB3674x.

- **System Open Loop Protection**

The function of system open loop protection is provided in OB3674x. If the voltage of INV pin is below 0.3V (typical,) the switching will be stopped. In this way, the system output voltage cannot be increased too high (only the rectified line voltage), and the pre-converter will be protected from damage.

- **Over temperature protection**

Over temperature protection is offered in OB3674x. When temperature of the device rises above 165℃ (typical),The device stops switching immediately, When temperature of the device is below 115℃(typical), The device back to normal switching.

- **PCB layout Consideration**

The signal ground of R4, R5, C3, C4and U1(GND) must be connected to the ground of C2,and then C2 ground connected to ground of C1 shortest and separately. The C2 two pins connected to U1 must be shortest as possible,
The ground of Co must be connected to the ground of C1 separately.
The power ground of Rcs must be connected to the ground of C1 separately, and the route must be shortest.
As shown in figure layout below, the green and wiring of components connected to the U1 pin must be as short as possible. That green signal wiring must kept away from blue high voltage wiring and high frequency signal connected point and wiring.
The blue wiring connected to L1, D6and Drain(U1) must be as short as possible. All components connected to U1 should be nearly around.
Minimize the area of the following power loops.

a) The power loops of V+→C1→V-.
b) The power loops of C1+→L1→(Drain)U1 →Rcs→C1-.
c) The power loops of L1→D6→Co→C1→ L1.

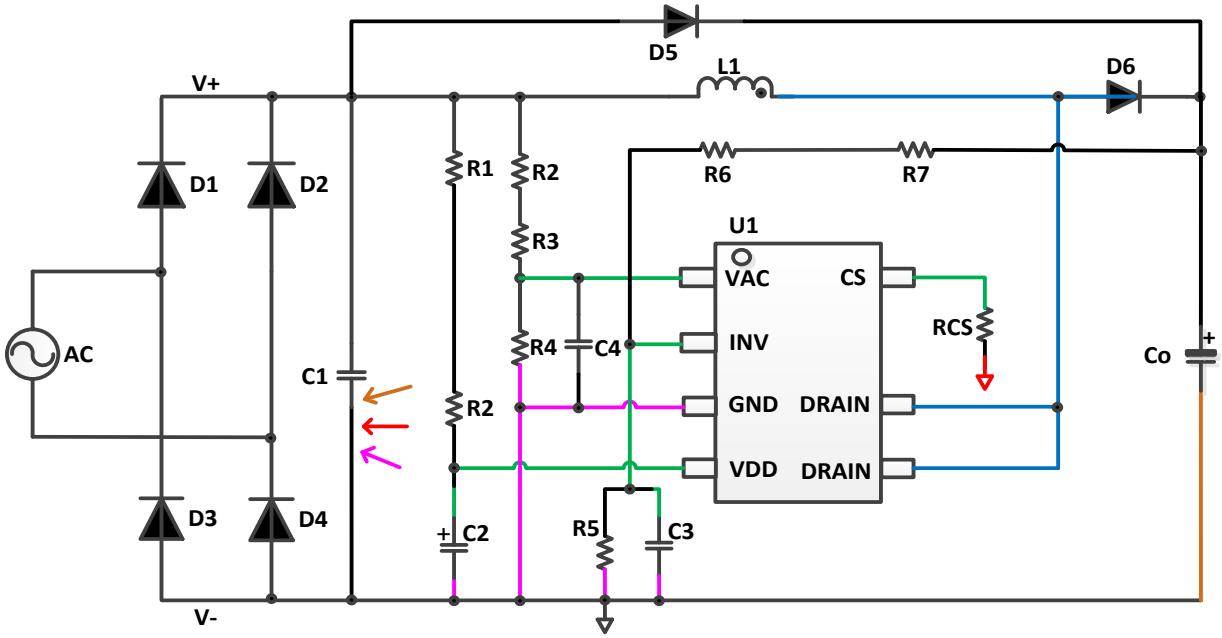
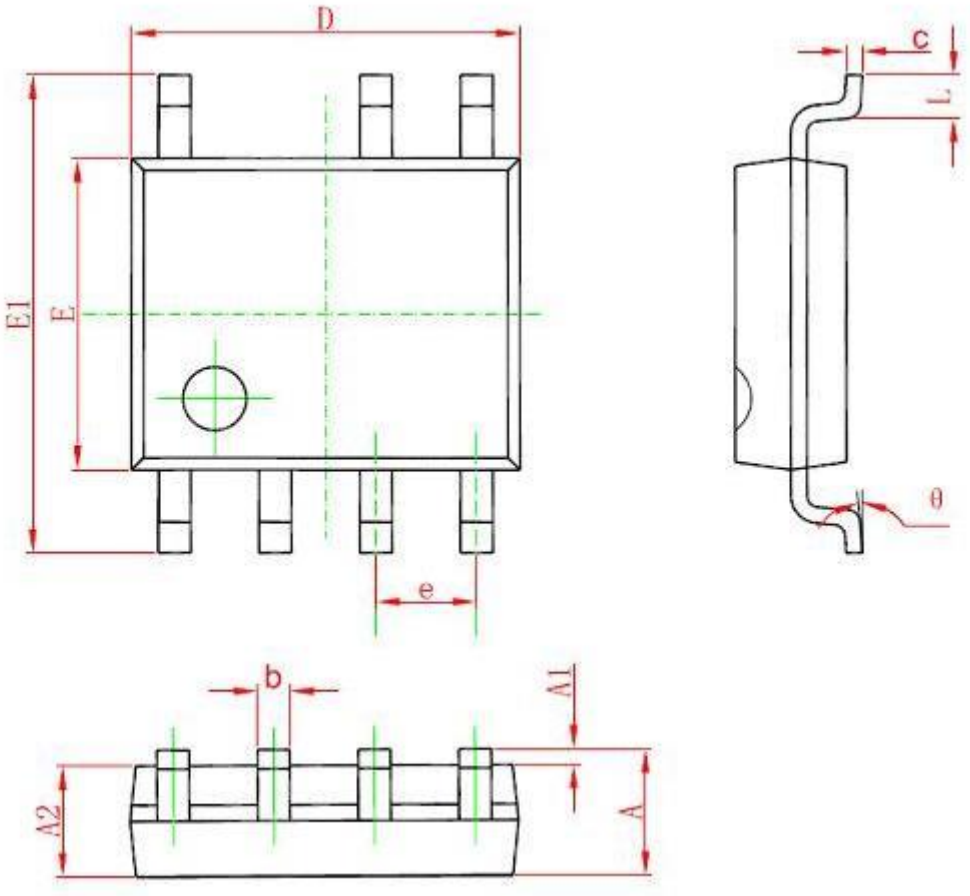


Figure layout

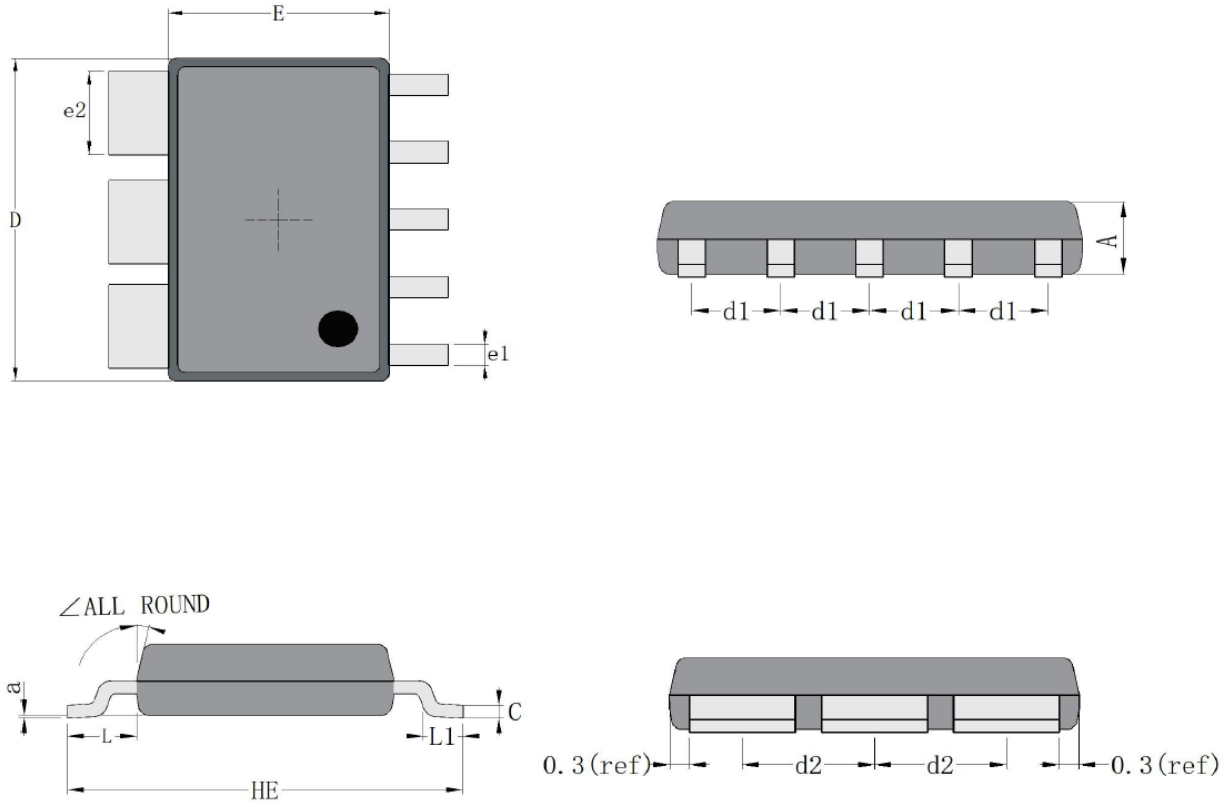
PACKAGE MECHANICAL DATA

SOP7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.700	4.100	0.146	0.161
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

ASOP6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.05	1.25	0.041	0.049
C	0.15	0.22	0.006	0.009
D	6.00	6.40	0.236	0.252
E	3.70	4.10	0.146	0.161
HE	5.90	6.10	0.232	0.240
d1	1.25	1.35	0.049	0.053
d2	1.95	2.05	0.077	0.081
e1	0.35	0.45	0.014	0.018
e2	1.55	1.65	0.061	0.065
L	0.95	1.15	0.037	0.045
L1	0.40	0.80	0.016	0.031
a	0.20 (REF)		0.008 (REF)	

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