GENERAL DESCRIPTION

OB2001xK is a high performance and tightly integrated secondary side synchronous rectifier for switch mode power supply system. It combines a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier at the secondary side of Flyback converter, which can reduce heat dissipation, increases output current capability and efficiency and simplify thermal design. OB2001xK can support low system output voltage down to 2V at constant current mode.

It is suitable for multiple mode applications including discontinuous conduction mode and quasi-resonant mode. With its versatility and optimization, OB2001xK can be used in various switch mode power supply topologies including secondary-side control topology and primary-side control topology.

From the information on the secondary side of the isolation transformer, OB2001xK generates a driving signal with dead time with respect to the primary side PWM signal to turn the integrated N-channel SR switch on and off in proximity of the zero current transition. It is optimized for 5V output voltage.

The externally adjustable minimum on time and property off time control scheme effectively avoid the ring impact induced by parasitic elements so that a reliable and noise free operation of the SR system is insured.

OB2001xK is offered in SOP8 package.

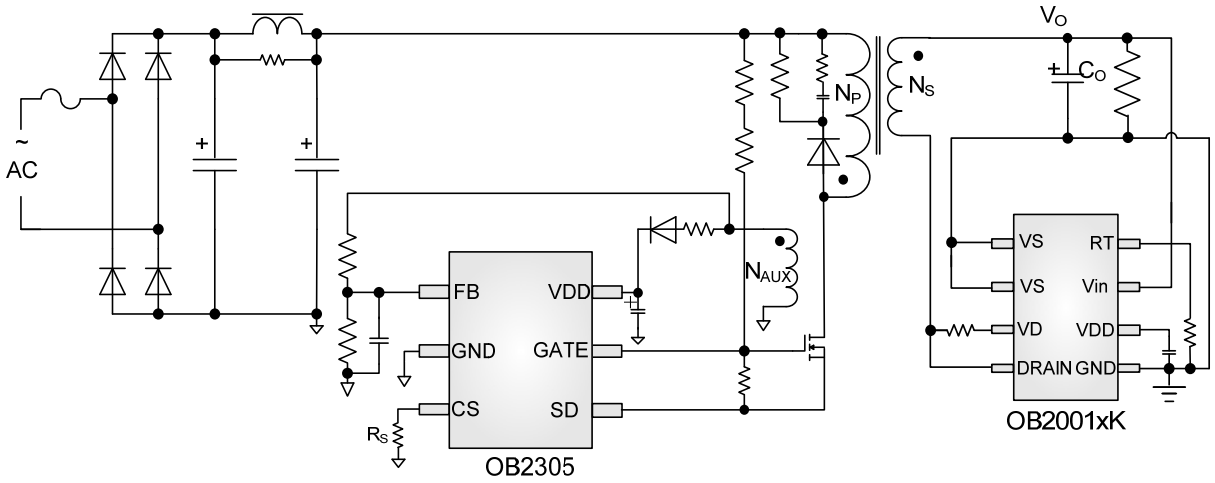
FEATURES

- Secondary-side synchronous rectifier optimized for 5V output system
- Suitable for DCM, QR operation
- Accurate secondary side MOSFET Vds sensing
- Low cost small size CC/CV mode support
- Up to 200kHz operation frequency
- Output voltage overshoot control
- VDD UVLO protection

APPLICATIONS

- AC/DC 5V adaptors
- Cell phone charger
- 5V Bias supply
- Low voltage rectification circuits

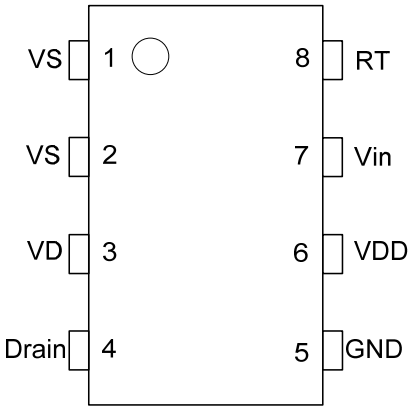
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2001xK is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB2001WKCP	SOP8, Halogen-free in Tube
OB2001WKCPA	SOP8, Halogen-free in T&R

Package Dissipation Rating

Package	RθJA(℃/W)
SOP8	90

Absolute Maximum Ratings

Parameter	Value
Vin pin	-0.6V to 7V
VDD pin	-0.6V to 7V
VD pin	-2.5V to 50V Note2
VS pin	-0.6V to 7V
RT pin	-0.6V to 7V
Drain pin	-0.6V to BVdss Note3
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-20 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

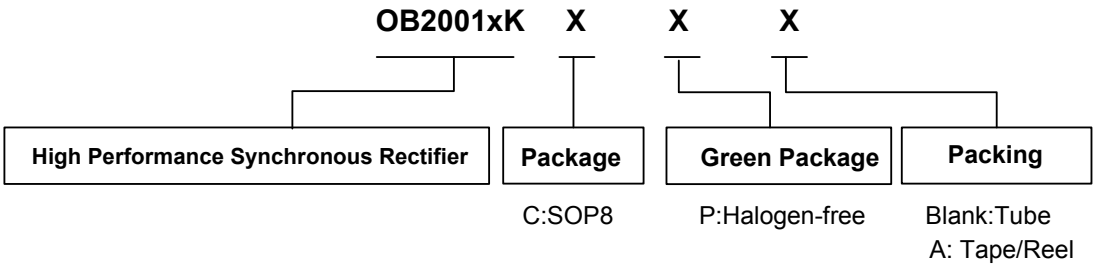
Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note2: -2.5V applies to minimum duty cycle during normal operation only.

Note3: -0.6V is self-clamped

Recommended Operating Range

Symbol	Parameter	Min/Max
VDD	VDD Supply Voltage	4V to 5.5V



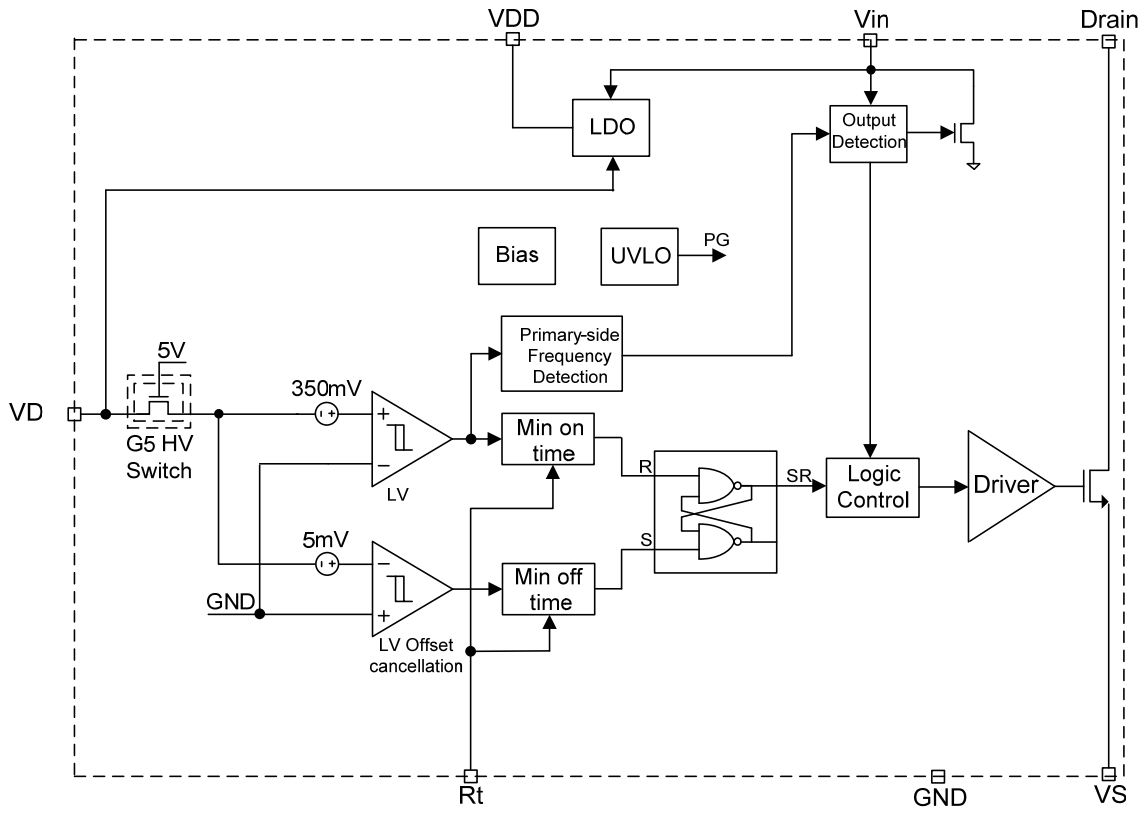
Marking Information

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Halogen-free Package
K:Character Code
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VS	I	This pin is connected to external n-channel MOSFET source
VD	I	This pin is connected to external n-channel MOSFET drain
Drain	I/O	SR Mosfet drain pin. This pin is connected to secondary-side winding of transformer
GND	P	Ground.
VDD	P	Power Supply
Vin	I	System output voltage detection
RT	O	Minimum on time control pin. A resistor is connected from this pin to GND

BLOCK DIAGRAM



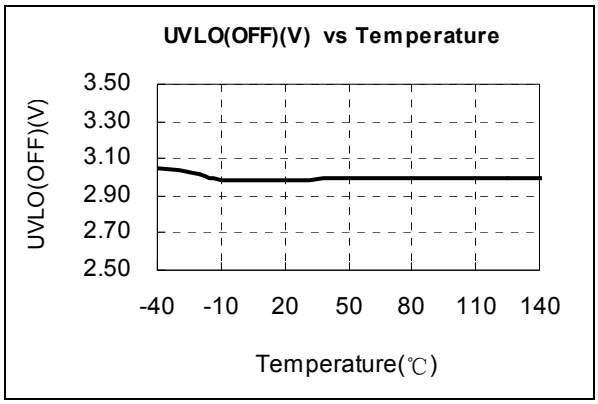
ELECTRICAL CHARACTERISTICS

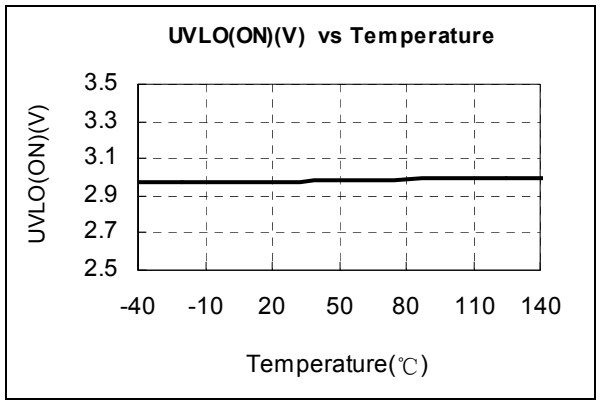
(T_A = 25℃, VDD=5V, unless otherwise noted)

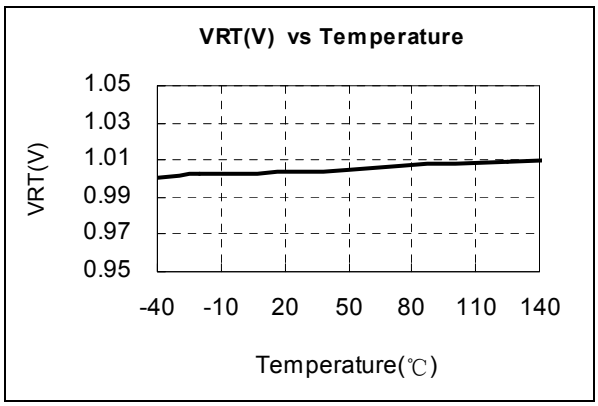
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I_VDD_operation	Operation current	Frequency@VD=65KHz,VDD=5V		1.5	2.0	mA
		Frequency@VD=2KHz,VDD=5V		0.5	0.7	mA
VDD_regulation_mini	Minimum VDD regulation voltage			4.2		V
UVLO(ON)	VDD Under Voltage Lockout Entry		2.8	3.0	3.2	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		2.9	3.1	3.3	V
VD Detection Section						
Vth_SR_act	SR MOSFET turn on threshold voltage detection at VD			-350		mV
Vth_SR_deact	SR MOSFET turn off threshold voltage detection at VD			-5		mV
Tdelay_on	SR MOSFET turn-on propagation delay				100	ns
Tdelay_off	SR MOSFET turn-off propagation delay				75	ns
T_minimum_on	SR MOSFET minimum on time	RT=25KΩ		1.9		us
RT Section						
Vrt	Voltage reference at RT pin		0.95	1	1.05	V
Overshoot Control Section						
Vin_High_clamp_1st	System output 1st overshoot clamp control trigger voltage at Vin with SR frequency lower than 7.5KHz			5.65		V
Vin_High_clamp_2nd	System output 2nd overshoot clamp control trigger voltage at Vin			6.15		V
IVin_High_clamp	System output overshoot clamp current at Vin			70		mA

SR Mosfet Section						
Parameter / **Product**	**BVdss(V)** MOSFET Drain-Source Breakdown Voltage			**Rds,on(mΩ)** On resistance		
	Min	Typ.	Max	Min	Typ.	Max
OB2001WK	40				15	

CHARACTERIZATION PLOTS







Operation Description

OB2001xK is a high performance and versatile synchronous rectifier. It can emulate the behavior of Schottky diode rectifier which directly reduces power dissipation of the traditional rectifiers and indirectly reduces primary-side loss due to compounding of efficiency gains.

Startup and under voltage lockout(UVLO)
OB2001xK implements UVLO function during startup. When VDD rises above UVLO(off), the IC wakes up from under voltage lock out state and enter normal operation. When VDD drops below UVLO(on), the IC enter under voltage lock out state again and the SR gate is pulled low by 10K resistor on chip. In addition, there is a hysteresis window between UVLO(off) and UVLO(on) to make system work reliably.

Synchronization rectifier
OB2001xK controls the turn-on and turn-off of synchronization rectifier MOSFET (SR MOSFET) by detection of drain-source voltage. When demagnetization of transformer starts, the secondary-side current will flow through the body diode of SR MOSFET and the voltage at the drain will drop to about -700mV. As soon as OB2001xK detects this negative voltage, the driver voltage is pulled high to turn on the SR MOSFET after very short delay time about 100nS, refer to Fig.1.
After the SR MOSFET is turned on, the drain voltage of SR MOSFET begins to rise based on its Rdson and secondary-side current. The drain voltage becomes higher with demagnetization going on. When the drain voltage rises above -5mV, the driver voltage will be pulled down to ground very quickly, refer to Fig.1

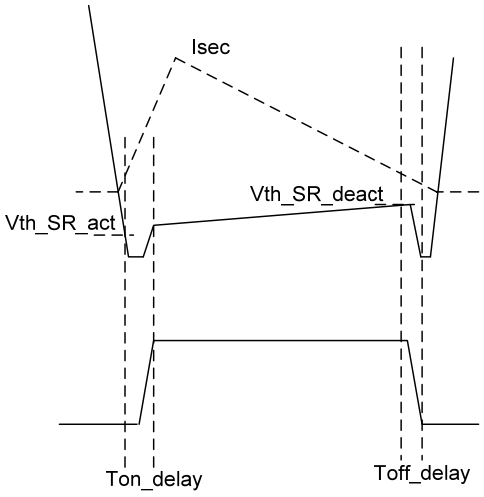


Fig.1 SR MOSFET turn-on and turn-off timing

Adjustable minimum on time
OB2001xK offers adjustable minimum on time control. This timer can avoid effectively false turn-off due to high frequency interference caused by parasitic element at the start of secondary-side demagnetization.

Tonmin=8*RT*10E(-11)

Adaptive minimum off time
At the end of demagnetization, SR MOSFET will be turn off. The remaining current will flow through body diode again, which may result in negative voltage (about -700mV) appears at drain and SR MOSFET will turn on again. In addition, the resonance oscillation between the magnetization inductance and parasitic capacitance after demagnetization may cause negative drain voltage. These may turn on SR MOSFET by mistake. To avoid above mis-turn-on of SR MOSFET, constant minimum off time can be used to screen it. But it may disturb SR MOSFET operation. For reliable SR operation, proprietary adaptive minimum off time control is implemented in OB2001xK, which can guarantee reliable synchronous rectification operation in DCM, QR.

Output overshoot clamp
For poor system design, there is usually output overshoot during startup and load transient. To facilitate system design, OB2001xK can detect output overshoot condition and prevent overshoot happen. When output voltage rises to meet the inner threshold, OB2001xK will open a discharge path from Vin to ground to clamp the system output voltage, so the system output overshoot can be prevented.

PCB Layout Consideration
The following rules should be followed in OB2001xK PCB Layout:
The Area of Power Loop: The area of the secondary current loop including the OB2001xK and the output capacitor should be as small as possible to reduce EMI radiation. And the PCB trace must be wide and short for thermal consideration.
Ground Path: The VS pin should be shorted directly to the GND pin under the bottom of OB2001xK before single point connected to the negative node of the output capacitor (Pink region as shows in Fig.3). This increases the copper area at the bottom of OB2001xK for heat dissipation and reduce the impedance between VS pin and GND pin.
Bypass Capacitor: The bypass capacitor on VDD should be placed as close as possible to the VDD

pin. And the negative node of VDD capacitor should be connected directly to the GND pin (White region as shows in Fig.3).

VD pin and Drain pin: The resistor in the Fig.3 is recommended to be placed between the VD pin and the Drain pin for improving the ESD ability. The recommended value of the resistor is 10ohm with package type of 0805. No trace under this resistor is required (Green region as shows in Fig.3).

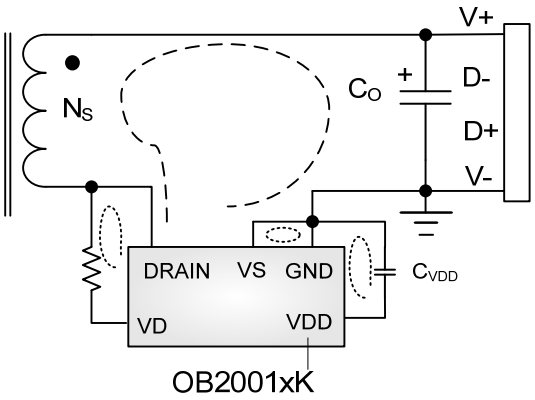


Fig.2 Proper Loop at the Secondary Side of the Flyback with OB2001xK

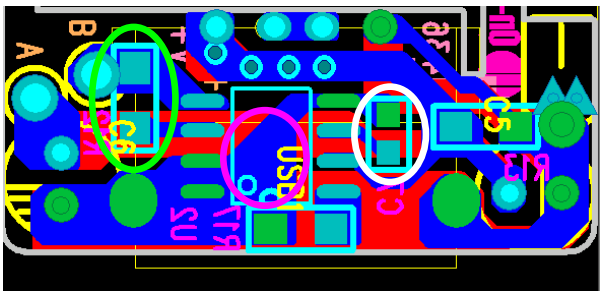
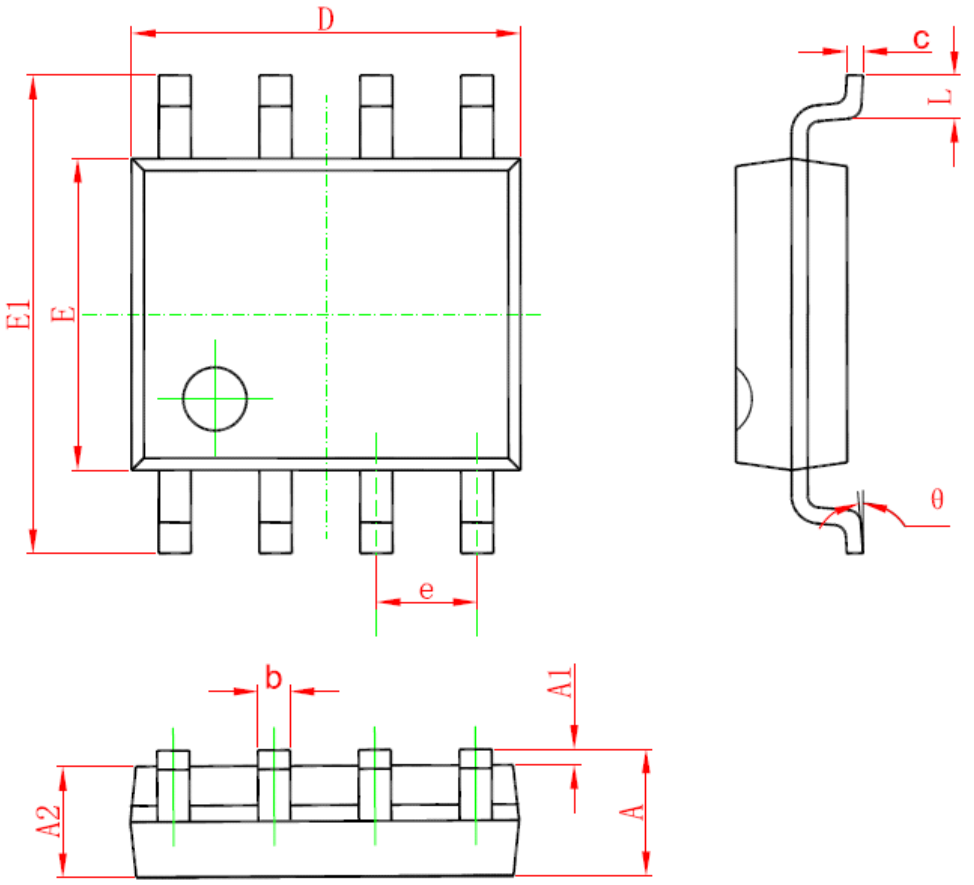


Fig.3 Recommend PCB Layout of OB2001xK

PACKAGE MECHANICAL DATA
SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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