

GENERAL DESCRIPTION

OB3619Ex is a high power factor, low THD, and highly integrated buck regulator with advanced features to provide high efficiency control and high precision constant current output for LED lighting applications.

The proprietary CC control scheme is used and the system can achieve high power factor with constant on-time control scheme. Quasi-resonant (QR) operation and clamping frequency greatly improves the system efficiency. The advanced start-up technology is used to meet the start-up time requirement (<0.5s). The constant output current is compensated for tolerance of transformer inductance variation.

OB3619Ex offers comprehensive protection coverage with auto-recovery features including LED open loop protection, LED short circuit protection, cycle-by-cycle current limiting, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

OB3619Ex is offered in SOP7 package.

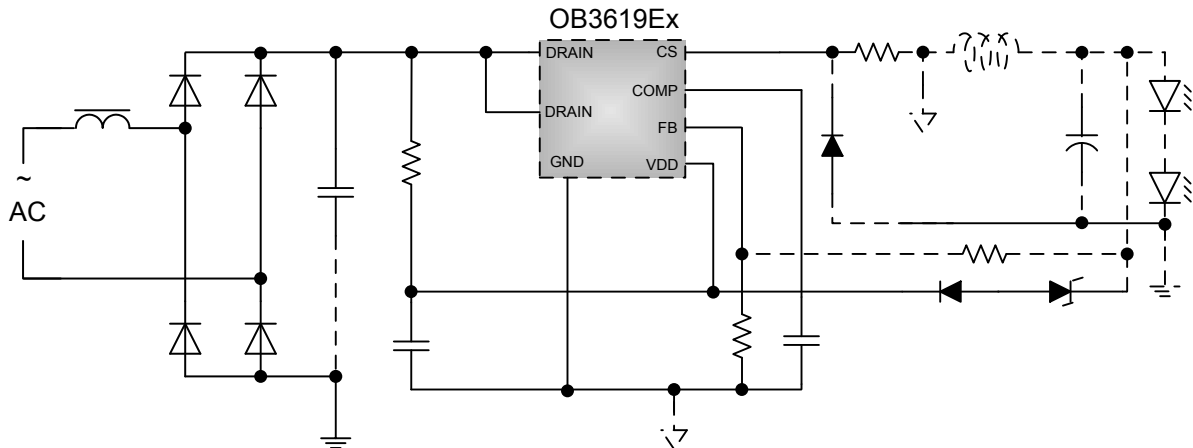
FEATURES

- High PF (>0.9)
- Low THD (<15%)
- High precision constant current regulation at universal AC input
- Fast start-up (<0.5s)
- Low system cost and high efficiency
- Quasi-resonant operation
- Programmable CC regulation
- LED short circuit protection
- LED open loop protection
- Cycle-by-cycle current limiting
- Built-in leading edge blanking (LEB)
- VDD under voltage lockout with hysteresis
- VDD over voltage protection
- Over temperature protection (OTP)
- Thermal fold-back control

APPLICATIONS

- LED lighting

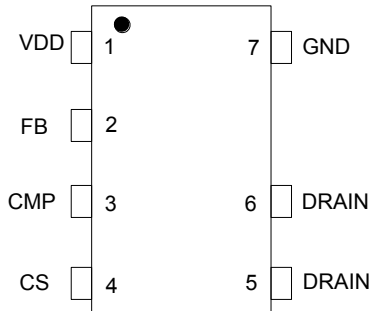
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for SOP7.



FB Input Voltage	-0.3 to 7V
COMP Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _J	-40 to 150 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Description
OB3619ENJPA-H	SOP7, Halogen-free in T&R
OB3619EPJPA-H	SOP7, Halogen-free in T&R
OB3619ETJPA-H	SOP7, Halogen-free in T&R
OB3619EUJPA-H	SOP7, Halogen-free in T&R
OB3619EPJPA-N	SOP7, Halogen-free in T&R

Note: All Devices are offered in Halogen-free Package if not otherwise noted.

Package Dissipation Rating

Package	RθJA (°C/W)
SOP7	95

Absolute Maximum Ratings

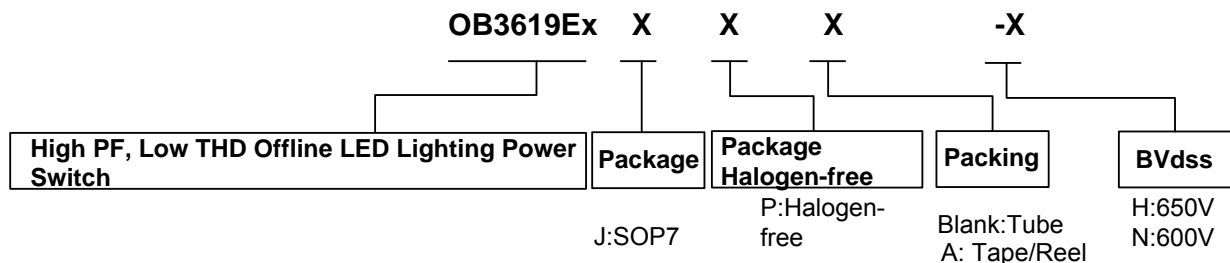
Parameter	Value
VDD Voltage	-0.3 to 40V
Gate Voltage	-0.3 to 40V
CS Input Voltage	-0.3 to 7V

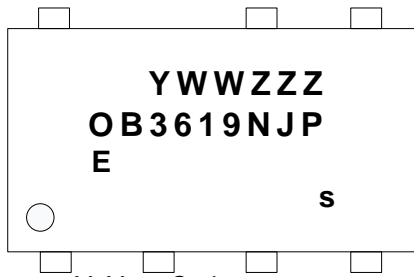
Output Power Table

Product	Condition	90Vac~264Vac Input	220Vac ±20% Input
OB3619ENJPA-H	I _{out} ≤0.2A	8.5W	15.5W
OB3619EPJPA-N	I _{out} ≤0.25A	12W	20W
OB3619EPJPA-H	I _{out} ≤0.25A	12W	20W
OB3619ETJPA-H	I _{out} ≤0.3A	15W	25W
OB3619EUJPA-H	I _{out} ≤0.4A	23W	43W

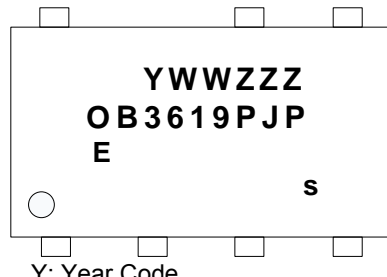
Note: Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50°C ambient and 60°C temperature rise. Higher output power is possible with extra added heat sink, air circulation and decrease output current to reduce thermal resistance.

Marking Information

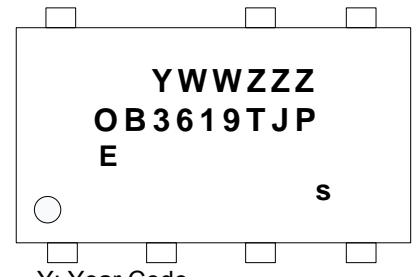




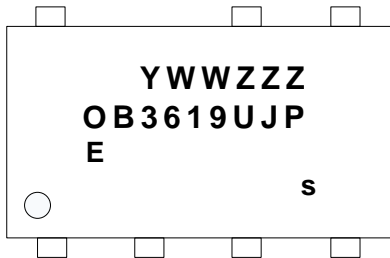
Y: Year Code
 WW: Week Code (01-52)
 ZZZ:Lot Code
 J: SOP7
 P:Halogen-free Package
 E:Character code
 S: Internal Code(Optional)



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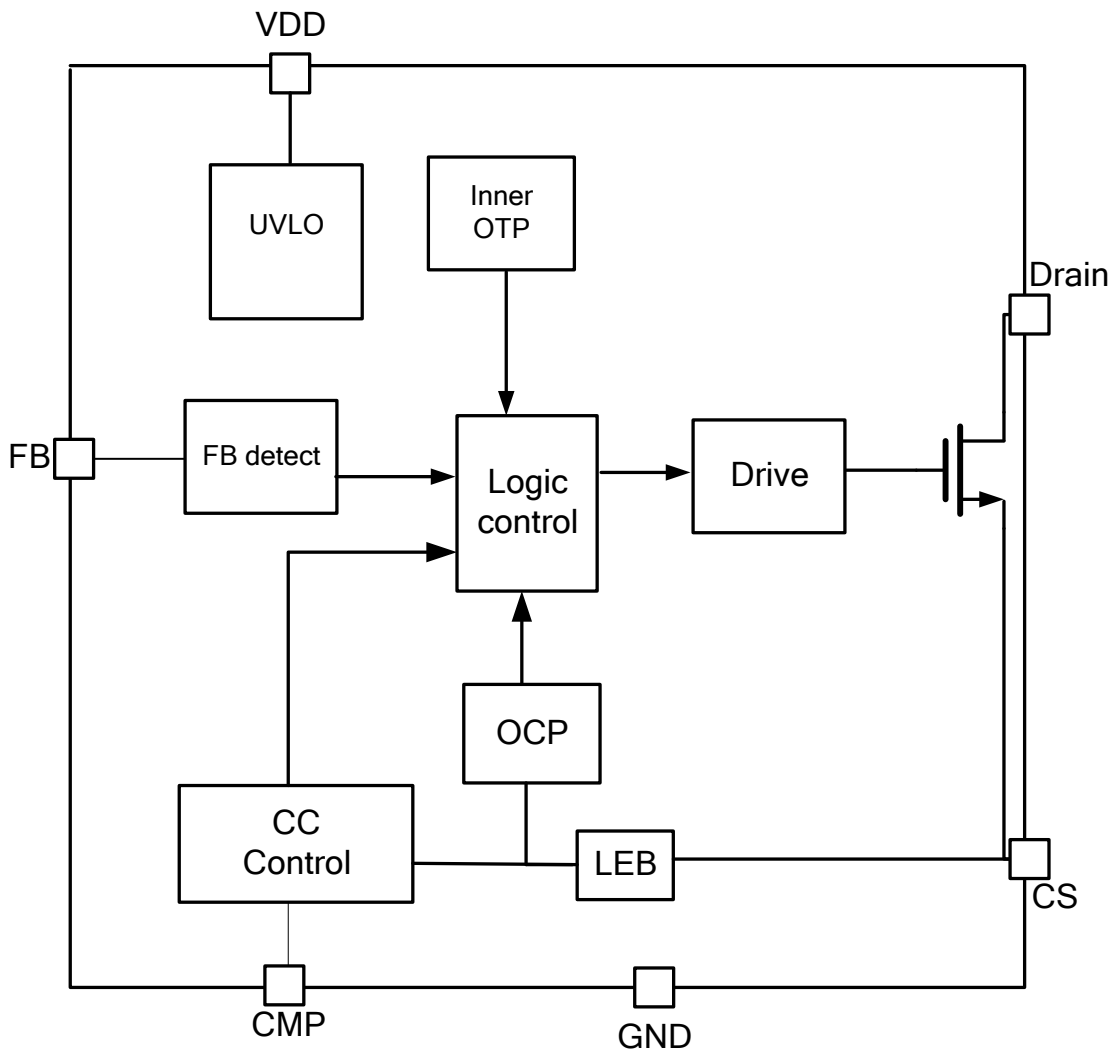


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TERMINAL ASSIGNMENTS SOP8

Pin Num	Pin Name	I/O	Description
1	VDD	P	Power supply Input.
2	FB	I	Voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
3	CMP	O	Loop compensation pin. A capacitor is connected between CMP and GND.
4	CS	I	Current sensing terminal.
5,6	DRAIN	I/O	Drain of power MOSFET.
7	GND	P	Power Ground.

BLOCK DIAGRAM



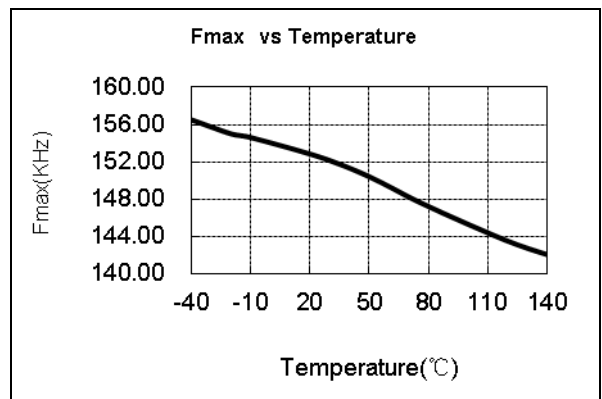
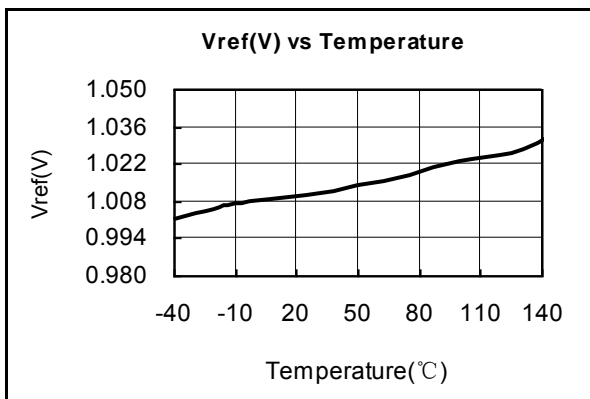
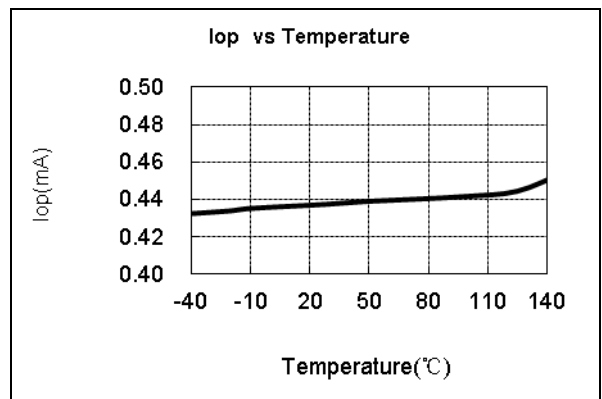
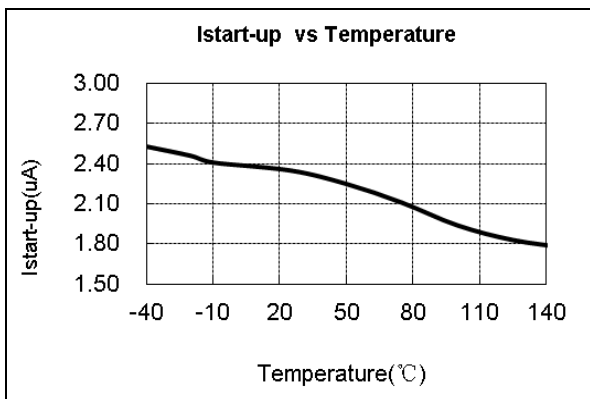
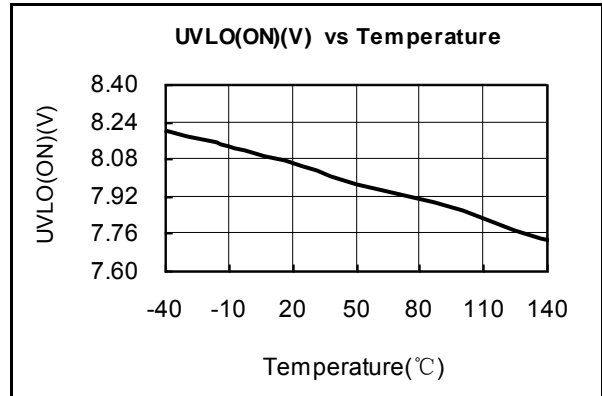
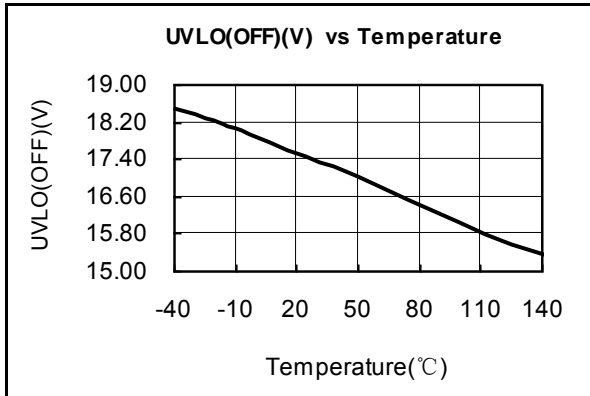
ELECTRICAL CHARACTERISTICS

(TA = 25°C, VDD=20V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD) Section						
I _{start-up}	Start up current	VDD=UVLO(OFF)-1V		3	7	uA
I _{op}	Operation current	VDD=20V, no loading		0.4	0.6	mA
UVLO(OFF)	VDD under voltage lockout exit		16	18	20	V
UVLO(ON)	VDD under voltage lockout enter		7	8	9	V
VDD_OVP	VDD Over Voltage Protection		30	32	34	V
Current Sense Input Section						
TLEB	LEB time			0.4		us
V _{th_ocp}	Over Current Threshold	FB>0.25V	1.05	1.1	1.15	V
		FB<=0.25V		0.5		V
FB Input Section						
V _{out_ovp}	Output Over Voltage Protection		1.42	1.5	1.58	V
V _{out_scp}	Output Short Circuit Protection			0.25		V
I _{FB}	Maximum Sink current from FB				2	mA
QR Section						
F _{max}	Maximum Clamping Frequency			150		KHz
T _{off_max}	Maximum Off Time			100		us
T _{off_min}	Minimum Off Time	CS>0.15V		2		us
		CS<=0.15V		0.5		us
T _{on_max}	Maximum On Time			25		us
Error Amplifier Section						
V _{ref}	Error Amplifier Reference Voltage		0.196	0.200	0.204	V
G _m	Error Amplifier Transconductance			40		uS
V _{clamp_cmp}	CMP Pin Down_clamp Voltage			1.0		V
Gate Driver Section						
V _{ol}	Output Low Level	I _{out} =10mA			1	V
V _{oh}	Output High Level	I _{out} =10mA	6			V
V _{clamp}	Output Up-Clamping Voltage		10	12	14	V
T _r	Rising Edge Time	C _l =1nF		90		ns
T _f	Falling Edge Time	C _l =1nF		30		ns
OTP Section						
T _{TF}	Thermal regulation threshold			145		°C
OTP	Over Temperature Protection			170		°C

Product	Parameter	BV _{dss} (V) MOSFET Drain-Source Breakdown Voltage		
		Min	Typ.	Max
OB3619ENJPA-H		650		
OB3619EPJPA-H		650		
OB3619ETJPA-H		650		
OB3619EUJPA-H		650		
OB3619EPJPA-N		600		

CHARACTERIZATION PLOTS



OPERATION DESCRIPTION

OB3619Ex is a high power factor, low THD, and highly integrated buck regulator with advanced features to provide high efficiency control and high precision constant current output for LED lighting applications.

OB3619Ex works at Quasi-Resonant operation with maximum working frequency clamping, which can improve the efficiency of LED lighting system design.

Start up Control

The advanced start-up technology is used in OB3619Ex to meet the start-up time requirement (<0.5s). Low start-up current is designed in OB3619Ex so that VDD could be charged up above UVLO threshold with small charging current.

At the startup, the capacitor at CMP pin is pulled up quickly. OB3619Ex operates at open loop and over-current protection is set cycle-by-cycle until it senses the output voltage by FB pin up to about 0.6V. After that OB3619Ex operates in close loop and the transconductance of error amplifier is set to 40uS (typical).

LED Constant Current Regulation

OB3619Ex uses the constant current control method to accurately control the LED current. It detects LED current and forces the average LED current equals to the ratio of reference voltage to resistance at CS pin as shown in the equation below:

$$I_{LED} = \frac{V_{ref}}{R_{CS}}$$

Rcs — the sensing resistor connected between the MOSFET source and the GND pin of IC.

Vref — the internal reference voltage.

PFC and THD

The duration of the turn on period t_{on} is generated by comparing an internal fixed saw-tooth wave with the voltage on the CMP pin. During steady state operation, the voltage on the CMP pin V_{cmp} is slowly varying due to a large external capacitor connected at the CMP pin, therefore the turn on time t_{on} is constant. In a buck topology, constant turn on time and quasi-resonant operation provide high power factor (PF) and low total harmonic distortion (THD).

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting (OCP) is offered in OB3619Ex. The switching current is detected by a sense resistor connected between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse

recovery so that the external RC filter is no longer required. The current limit comparator is disabled at this blanking time and thus the external MOSFET cannot be turned off during this blanking time.

Quasi-Resonant Operation

OB3619Ex performs quasi-resonant detection through FB pin by monitoring the voltage activity on the auxiliary windings in series with external resistors. When the stored energy of the transformer is fully released to the output, the voltage at FB pin decreases. When FB pin voltage falls below 0.05V (typical), an internal FB comparator is triggered and a new PWM switching cycle is initiated following the FB triggering.

VDD Over Voltage Protection

VDD is supplied with transformer auxiliary winding output. When VDD is higher than 32V (typical), VDD OVP protection is triggered and GATE is shut down, and the device enters power on startup sequence thereafter.

Thermal Fold-back Protection

OB3619Ex provides thermal fold-back function to control LED output current. When temperature is up to 145 °C (typical) and the output current of system will be adjusted according to the sensed temperature. The output current will be reduce to about half of the setting value at 165 °C (typical). Over temperature protection is offered in OB3619Ex. When temperature rises above 170 °C (typical), the device will stop working.

LED Short Circuit Protection

When LED string is short, the positive plateau of auxiliary winding voltage is also near zero and the FB voltage is low. If the voltage at FB pin is lower than a threshold of approximately 0.25V (typical), the IC will work at minimum frequency and the threshold voltage of OCP is reduced to 0.5V (typical). The power dissipation is greatly reduced in this way.

LED Open Circuit Protection

When the LED string open circuit happens, the positive plateau of auxiliary winding voltage increases and the FB pin voltage is high. If the voltage at FB pin is higher than a threshold of approximately 1.5V (typical), the IC will shut down and enter power on startup sequence thereafter.

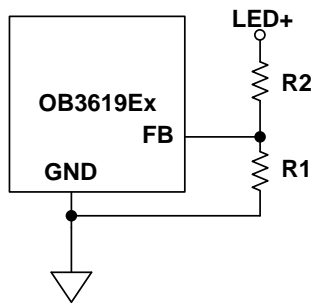


Figure2 FB Section Circuit

$$V_{OVP} = \frac{R1 + R2}{R1} \times V_{out_ovp}$$

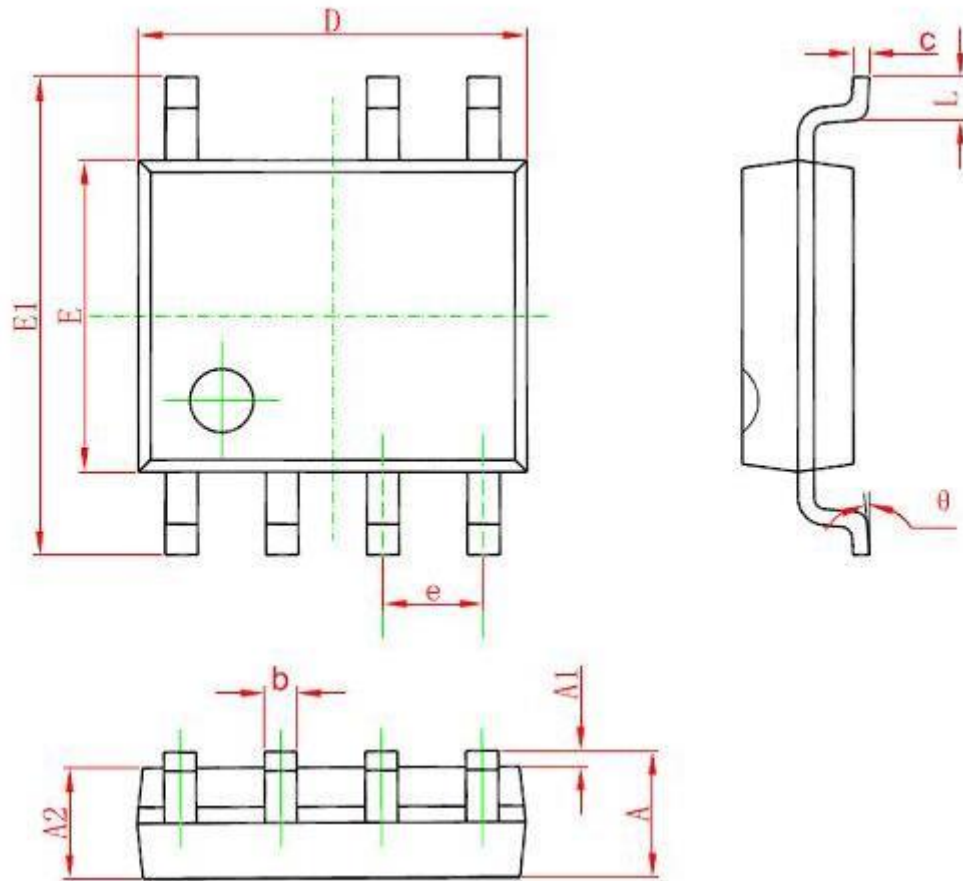
R2 — The resistor connected between the FB pin and the Output, the value suggested is 200Kohm~330Kohm

Gate Driver

The GATE pin is connected to the gate of an external power switch. An internal 12V (typical) clamp is added for MOSFET gate protection at high VDD voltage. When VDD voltage drops below UVLO (ON), the GATE pin is internally pulled low to maintain the off state.

PACKAGE MECHANICAL DATA

7/8-Pin Plastic SOP (SOP7/8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.700	4.100	0.146	0.161
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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