

## 4A Opto-Compatible Single Channel Isolated Gate Drive

### GENERAL DESCRIPTION

The SLMi350 is an opto-compatible, single channel, isolated gate driver for IGBTs, MOSFETs with 4A source and 7A sink peak output current and 3750V<sub>RMS</sub> reinforced isolation rating. SLMi350 can drive both low side and high side power FETs. Key features and characteristics bring significant performance and reliability upgrades over standard optocoupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, and small pulse width distortion.

The input stage is an emulated diode which means long term reliability and excellent aging characteristics compared to traditional LEDs. It is offered in a DIP8GW package with >7.0mm creepage and clearance. A mold compound from material group I which has a comparative tracking index (CTI) >600V. SLMi350's high performance and reliability makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

### FEATURES

- 4A source output current
- 7A sink output current
- 120ns (Max.) propagation delay
- 25ns (Max.) part-to-part delay matching
- 35ns (Max.) pulse width distortion
- 150kV/us (Min.) common mode transient immunity (CMTI)
- Gate drive supply range from 14 V to 40 V
- 30V reverse polarity voltage handling capability on input stage
- Pin to pin compatible to optocoupler isolated gate drivers
- DIP8GW package with >7.0mm creepage and clearance
- Junction temperature, T<sub>J</sub>: -40°C to +150°C
- Safety certifications (Planned)
  - 3750V<sub>RMS</sub> isolation for 1 minute per UL 1577
  - DIN V VDE 0884-11

### APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

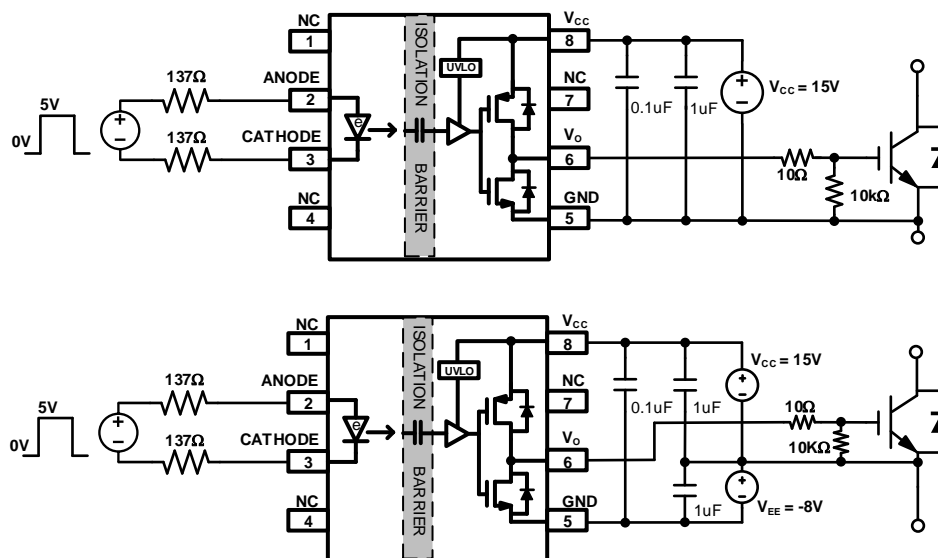


Figure 1. SLMi350 Single and Bipolar Power Supplies Application Circuit to Drive IGBT

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**PIN CONFIGURATION**

Package	Pin Configuration (Top View)
DIP8GW	

**PIN DESCRIPTION**

No.	Pin	Description
1	NC	No Connection
2	ANODE	Anode
3	CATHODE	Cathode
4	NC	No Connection
5	GND	Ground
6	V <sub>o</sub>	Gate Drive Output
7	NC	No Connection
8	V <sub>cc</sub>	Positive Power Supply Rail

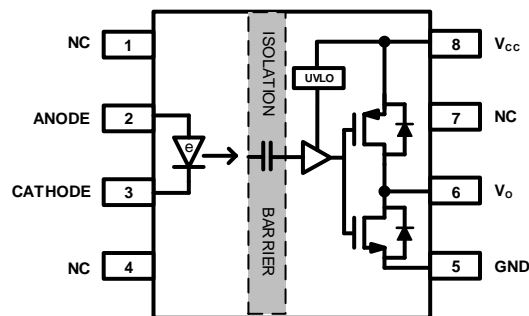
**FUNCTIONAL BLOCK DIAGRAM**


Figure 2. SLMi350 Functional Block Diagram

**ORDERING INFORMATION**

Order Part No.	Package	QTY
SLMi350DB-DG	DIP8GW, Pb-Free	1000/Reel

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min	Max	Units
$I_{F(AVG)}$	Average Input Current		25	mA
$V_R$	Reverse Input Voltage		30	V
$V_{CC}$	Output supply voltage		45	V
$T_J$	Junction temperature	-40	150	°C
$T_S$	Storage temperature	-55	150	°C

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Definition	Min	Max	Units
$V_{CC}$	Output Supply Voltage	14	40	V
$I_F(ON)$	Input Diode Forward Current (Diode "ON")	7	16	mA
$V_F(OFF)$	Anode Voltage - Cathode Voltage (Diode "OFF")	-30	0.9	V
$T_J$	Junction temperature	-40	150	°C
$T_A$	Ambient temperature	-40	125	°C

**ESD RATINGS**

Symbol	Definition	Value	Units
$V_{ESD}$	HBM	±4000	V
	CDM	±2000	V

**PACKAGE SPECIFICATIONS**

Symbol	Definition	Min	Typ	Max	Units
R <sub>IO</sub>	Resistance (Input Side to Output Side)		10 <sup>12</sup>		Ω
C <sub>IO</sub>	Capacitance (Input Side to Output Side)		1.6		pF
C <sub>IN</sub>	Input Capacitance		30		pF

**INSULATION SPECIFICATIONS**

Symbol	Definition	Value	Units
CLR	External clearance	7	mm
CPG	External creepage	7	mm
DTI	Distance through the insulation	>16	um
CTI	Comparative tracking index	>600	V
	Material Group	I	
	Overvoltage category		
	Rated mains voltages ≤150V <sub>RMS</sub>	I-IV	
	Rated mains voltages ≤300V <sub>RMS</sub>	I-IV	
	Rated mains voltages ≤450V <sub>RMS</sub>	I-III	
	Rated mains voltages ≤600V <sub>RMS</sub>	I-III	
	Rated mains voltages ≤1000V <sub>RMS</sub>	I-II	
<b>DIN V VDE 0884-11<sup>(1)</sup></b>			
V <sub>IOWM</sub>	Maximum isolation working voltage	891	V <sub>pk</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	6000	V <sub>pk</sub>
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	891	V <sub>pk</sub>
q <sub>pd</sub>	Apparent charge	≤5	pC
	Climatic Category	40/125/21	
	Pollution Degree	2	
<b>UL1577<sup>(1)</sup></b>			
V <sub>ISO</sub>	Isolation Voltage	3750	V <sub>RMS</sub>

1.Certification planned

**ELECTRICAL CHARACTERISTICS (DC)**

$V_{CC}=15V$  and  $T_A=25^{\circ}C$  unless otherwise specified. All min and max specifications are at  $T_A=-40^{\circ}C$  to  $125^{\circ}C$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>INPUT</b>						
$I_{FLH}$	Input Forward Threshold Current Low to High			2.1		mA
$V_F$	Input Forward Voltage	$I_F=10mA$		2.2		V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	$I_F=10mA$		0.5		mV/ $^{\circ}C$
$V_R$	Input Reverse Breakdown Voltage	$I_R=10\mu A$	30			V
<b>OUTPUT</b>						
$I_{OH}$	High Level Peak Output Current	$V_{CC}=15V, I_F=10mA$ $C_{VCC}=10\mu F,$ $C_{LOAD}=220nF$		4		A
$I_{OL}$	Low Level Peak Output Current	$V_{CC}=15V, V_F=0V,$ $C_{VCC}=10\mu F,$ $C_{LOAD}=220nF$		7		A
$V_{OH}$	High Level Output Voltage	$I_F=10mA, I_O=-20mA$ "with respect to $V_{CC}$ "		30		mV
$V_{OL}$	Low Level Output Voltage	$V_F=0V, I_O=20mA$		17		mV
$R_{DS\_OH}$	High Output Transistor $R_{DS}$			1.5		$\Omega$
$R_{DS\_OL}$	Low Output Transistor $R_{DS}$			0.85		$\Omega$
$I_{CC\_H}$	Output Supply Current (Diode On)	$I_F=10mA, I_O=0mA$		1.7		mA
$I_{CC\_L}$	Output Supply Current (Diode Off)	$V_F=0V, I_O=0mA$		1.4		mA
<b>UNDER VOLTAGE LOCKOUT</b>						
UVLOR	Under Voltage Lockout $V_{CC}$ rising	$I_F=10mA,$	11	12.5	13.5	V
UVLOF	Under Voltage Lockout $V_{CC}$ falling	$I_F=10mA$	10	11.5	12.5	V
UVLOHYS	Under Voltage Lockout Hysteresis			1.0		V

**SWITCHING CHARACTERISTICS (AC)**

$V_{CC} = 15V$  and  $T_A = 25^{\circ}C$  unless otherwise specified. All min and max specifications are at  $T_A = -40^{\circ}C$  to  $125^{\circ}C$

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
$t_{PLH}$	Propagation delay, Low to High	$C_{LOAD}=1nF, f_{sw}=20kHz,$ (50% Duty Cycle), $V_{CC}=15V$		80	120	ns	
$t_{PHL}$	Propagation delay, High to Low			80	120	ns	
$t_r$	Turn on rise time				8		ns
$t_f$	Turn off fall time				6		ns
$t_{PWD}$	Pulse Width Distortion					35	ns
$t_{PDD}$	Propagation Delay Difference Between Any Two Parts				25	ns	
$t_{UVLO\_REC}$	UVLO Recovery Delay	$V_{CC}$ Rising from 0V to 15V		22	30	us	
$CMTI_H$	Output High Level Common Mode Transient Immunity	$I_F=10mA, V_{CM}=1000V,$ $V_{CC}=15V, T_A=25^{\circ}C$	150	200		kV/us	
$CMTI_L$	Output Low Level Common Mode Transient Immunity	$V_F=0V, V_{CM}=1000V,$ $V_{CC}=15V, T_A=25^{\circ}C$	150	200		kV/us	

**PARAMETER MEASUREMENT INFORMATION**

**Propagation Delay, Rise Time and Fall Time**

Figure 3 shows the propagation delay from the input forward current  $I_F$  to  $V_{out}$ . This figure also shows the circuit used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times and the propagation delays  $t_{PDHL}$  and  $t_{PDHL}$ .

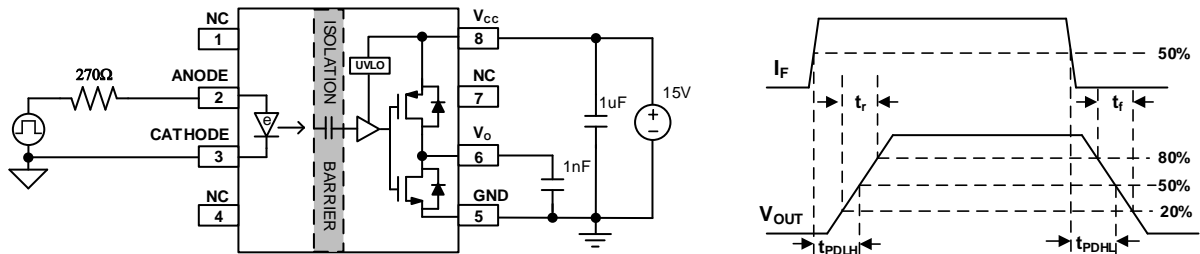


Figure 3. Propagation Delay, Rise Time and Fall Time

**$I_{OH}$  and  $I_{OL}$  Testing**

Figure 4 shows the circuit used to measure the output drive current  $I_{OL}$  and  $I_{OH}$ . A load capacitance of 220nF is used at the output. The peak  $dv/dt$  of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

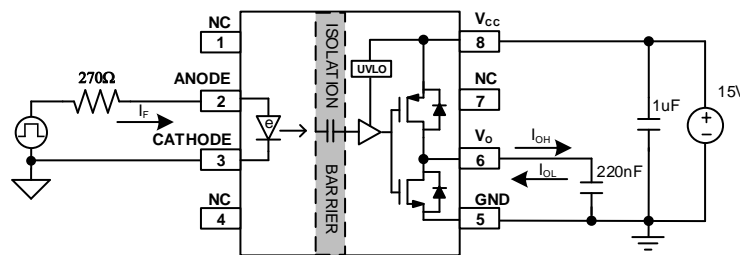


Figure 4.  $I_{OH}$  and  $I_{OL}$

**CMTI Testing**

Figure 5 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V. The test is performed with  $I_F=10mA$  ( $V_{OUT}= High$ ) and  $V_F=0mA$  ( $V_{OUT}= Low$ ).

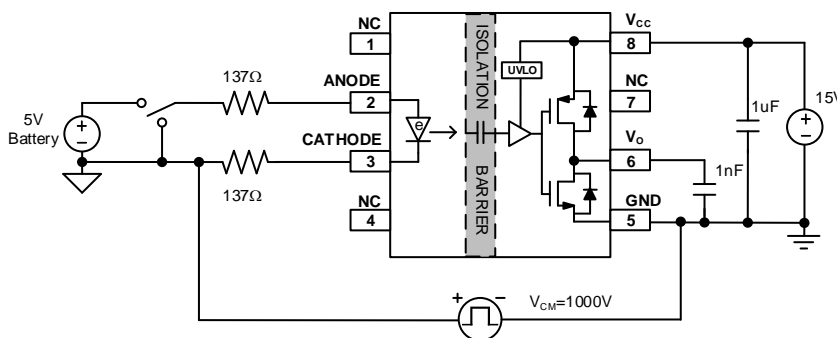


Figure 5. CMTI Test Circuit



## FEATURE DESCRIPTION

SLMi350 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs and MOSFETs. It has 4A source and 7A sink peak output current capability with maximum output driver supply voltage of 40V. The inputs and the outputs are galvanically isolated. SLMi350 is offered in an industry DIP8/DIP8GW package with >7.0mm creepage and clearance. The reinforced isolation rating is 3750V<sub>RMS</sub> for 60s. It is pin-to-pin compatible with standard optocoupler isolated gate drivers. While standard optocoupler isolated gate drivers use an LED as the input stage, SLMi350 uses an emulated diode as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV SiO<sub>2</sub> capacitors in full differential configuration that not only provides reinforced isolation but also offers the min. common mode transient immunity >150kV/us. The e-diode input stage along with capacitive isolation technology gives SLMi350 several performance advantages over standard optocoupler isolated gate drivers.

- Since the emulated diode does not use light emission for its operation, the reliability, and aging characteristics of SLMi350 are naturally superior to those of standard optocoupler isolated gate drivers.
- Higher ambient operating temperature range of 125°C, compared to only 105°C for most optocoupler isolated gate drivers.
- The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature.
- Higher common mode transient immunity than optocoupler isolated gate drivers.
- Smaller propagation delay than optocoupler isolated gate drivers.
- Due to superior process controls achievable in capacitive isolation compared to optocoupler isolation, there is less part-to-part skew in the prop delay, making the system design simpler and more robust
- Smaller pulse width distortion than optocoupler isolated gate drivers

### Input Stage

The input stage of SLMi350 is an emulated diode. When the emulated diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current,  $I_F$ , flows into the e-diode. The forward voltage drop across the e-diode is 2.2V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7mA to 16mA. When  $I_F$  exceeds the input forward threshold current  $I_{FLH}$  (2.1mA typ), the  $V_{OUT}$  is driver high. If the  $I_F$  is lower than  $I_{FLH}$ , or the voltage between Anode and Cathode is reverse biased, the  $V_{OUT}$  is driven low.

The reverse breakdown voltage of the e-diode is up to 30V. The large reverse breakdown voltage of the e-diode enables SLMi350 to be operated in interlock architecture as shown in Figure 6. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown in Figure 6 and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs as shown in Figure 7. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

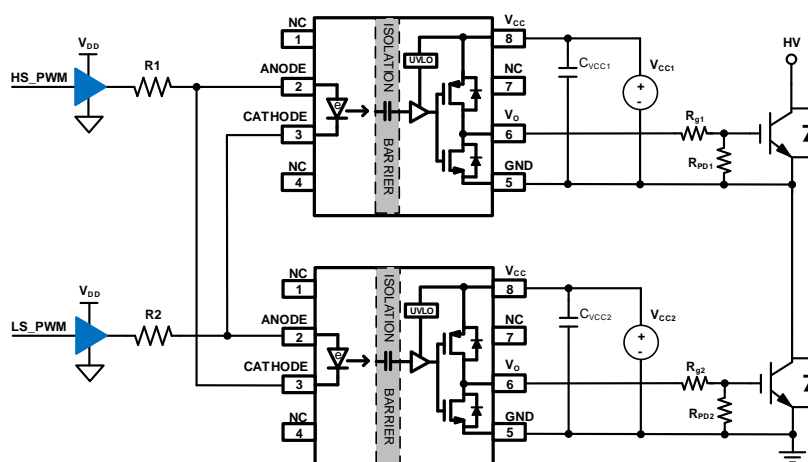
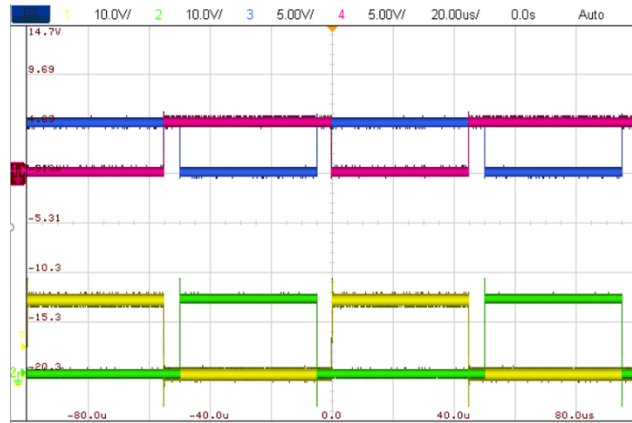


Figure 6. Interlock Architecture



CH1: HS\_OUT, CH2: LS\_OUT, CH3: HS\_PWM, CH4: LS\_PWM

Figure 7. Interlock PWM input and output waveform

**Under Voltage Lockout (UVLO)**

The SLMi350 integrates the UVLO protection on the  $V_{CC}$  to prevent an under driven condition on IGBTs and MOSFETs. When  $V_{CC}$  is lower than  $UVLO_R$  during start up or lower than  $UVLO_F$  after start up, the UVLO feature holds the  $V_{OUT}$  low, regardless of the input forward current. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply. When  $V_{CC}$  drops below  $UVLO_F$ , a recovery delay ( $t_{UVLO\_REC}$ ) occurs on the output when the supply voltage rises above  $UVLO_R$  again.

**Typical Input Configuration Circuit**

The circuit in Figure 8 and Figure 9 show two typical input configuration circuits for SLMi350 to driver IGBT.

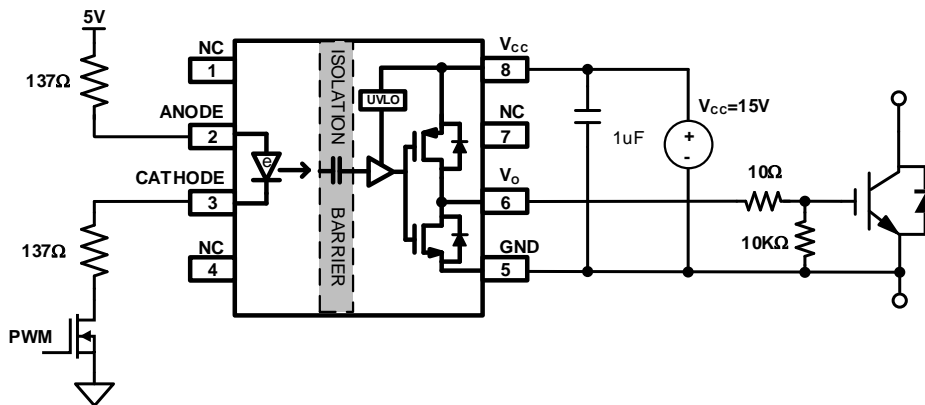


Figure 8. Single MOSFET Circuit as Input Drive of SLMi350 to Drive IGBT

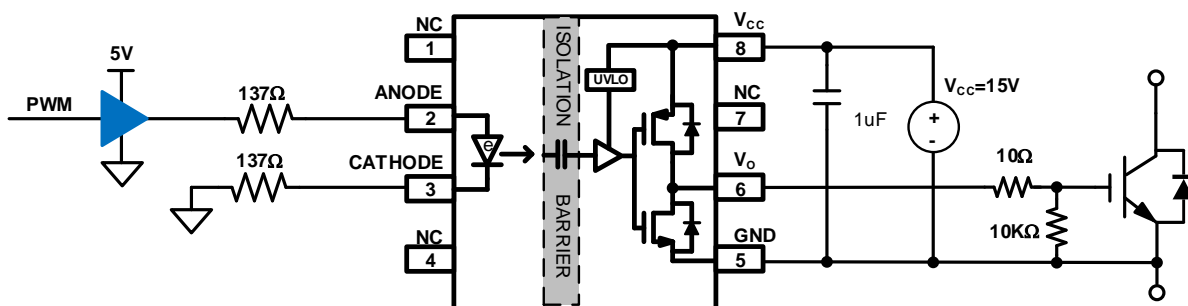


Figure 9. Buffer Circuit as Input Drive of SLMi350 to Drive IGBT

**Layout**

In order to achieve optimum performance for the SLMi350, some suggestions on PCB layout.

Component placement:

- Low ESR and low ESL capacitors must be connected close to the device between the  $V_{CC}$  and GND pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the GND pin connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

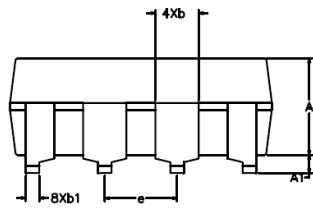
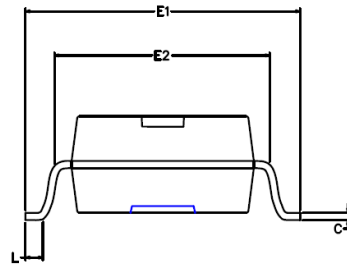
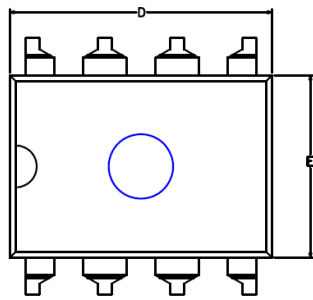
Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

**PACKAGE CASE OUTLINES**



Dimension	MIN	NOM	MAX
A	3.20	3.40	3.60
A1	0.105	0.315	0.525
b	1.524 BSC		
b1	0.380	0.475	0.570
c	0.203	0.254	0.330
D	9.00	9.20	9.40
E	6.20	6.40	6.60
E1	9.30	9.55	9.80
E2	7.27	7.52	7.77
e	2.54 BSC		
L	0.450	0.700	0.950

Unit : mm

Figure 10. DIP8GW Package Outline Dimensions

**REVISION HISTORY**

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 1.0 datasheet: 2021-12-30</b>	
Whole document	Initial release