Single-Channel, High-Speed, Low-Side Gate Driver

GENERAL DESCRIPTION

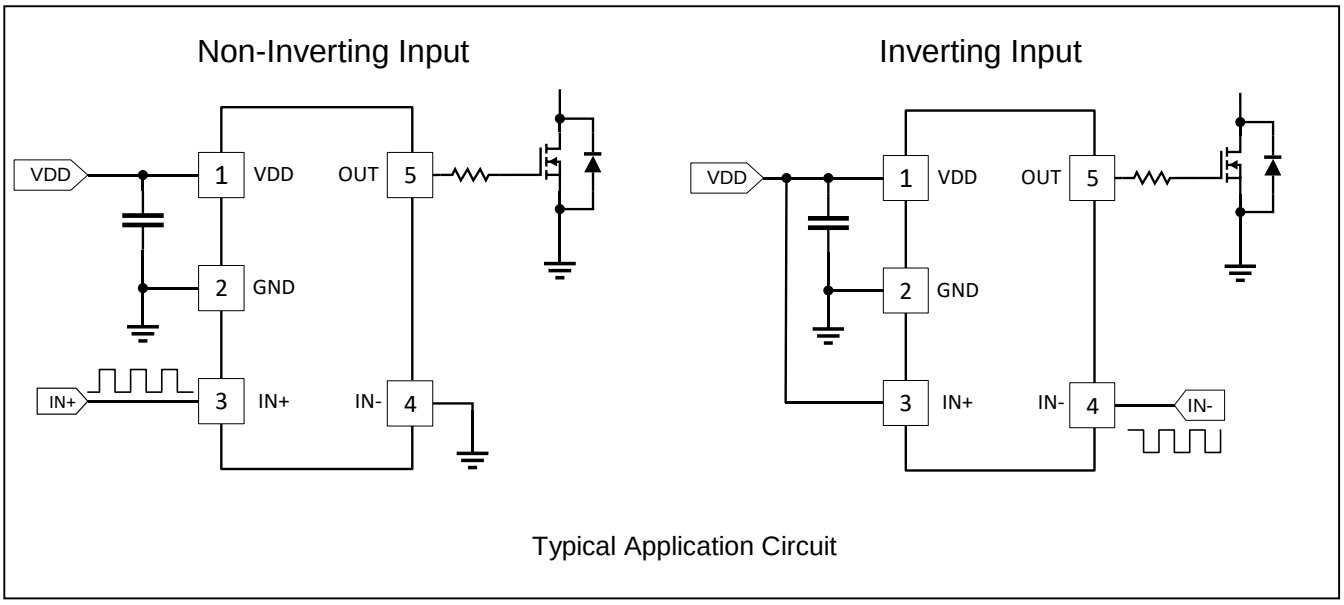
The SLM27517 series single-channel, high-speed, low-side gate driver devices can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, SLM27517 series products can source and sink high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 18ns.

The SLM27517 can provide 4 A source, 5 A sink peak-drive current capability at 12 V VDD supply.

FEATURES

- Low-cost gate-driver device offering superior replacement of NPN and PNP discrete solutions
- 4 A peak source and 5 A peak sink current
- Fast propagation delay (18ns typical)
- Fast rise and fall time (7 ns typical)
- 4.5 to 20V single supply range
- Under-voltage lockout
- TTL and CMOS compatible input logic threshold
- Dual input design (choice of an inverting or non-inverting driver configuration)
- Output held low when input pins are floating
- Operating temperature range of -40℃ to 140℃
- SOT23-5, package

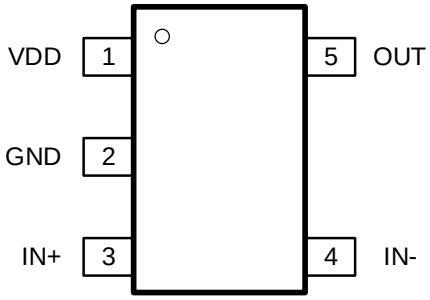
TYPICAL APPLICATION CIRCUIT



Typical Application Circuit

Table of Contents

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOT23-5	

PIN DESCRIPTION

No.	Name	Function Description
4	IN-	Inverting Input: When the driver is used in noninverting configuration, connect IN- to GND in order to enable output. OUT held LOW if IN- is unbiased or floating.
2	GND	Ground: All signals referenced to this pin.
1	VDD	Bias supply input.
5	OUT	Sourcing/sinking current output of driver
3	IN+	Noninverting Input: When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output. OUT held LOW if IN+ is unbiased or floating.

ORDERING INFORMATION

Order Part No.	Package	QTY
SLM27517AD-7G	SOT23-5	3000/Reel

FUNCTIONAL BLOCK DIAGRAM

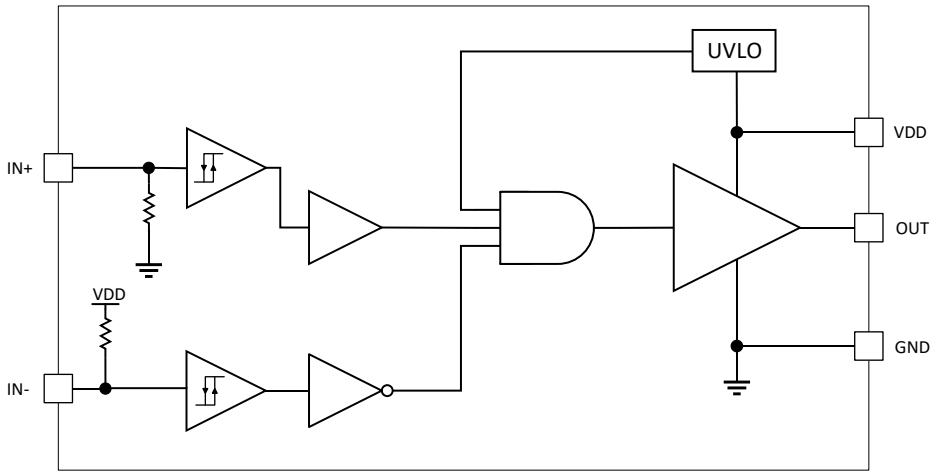


Figure 1. Function Block

ABSOLUTE MAXIMUM RATINGS[1,2,3]

Over operating free-air temperature range (unless otherwise noted)

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage	-0.3	25	V
V_O	Continuous voltage on OUT	0.3	V_{DD}+0.3	
	Repetitive pulse less than 200ns[4]	-2	V_{DD}+0.3	
I_O	Source Continuous Current on OUT		0.3	A
	Source Pulsed Current on OUT (0.5 µs)[4]		-4.5	
	Sink Pulsed Current on OUT (0.5 µs)[4]		5.7	
IN+, IN-	Voltage on the IN+, IN-[5]	-6	25	V
T_J	Junction temperature	-40	150	℃
T_L	Lead temperature (soldering, 10 seconds)		300	
T_S	Storage temperature	-65	150	

1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal.
3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.
4) Values are verified by characterization on bench.
5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

RECOMMENDED OPERATION CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Definition	Min	Max	Unit
V_{DD}	Supply voltage range	4.5	20	V
IN+, IN-	Input voltage	-5	20	
T_J	Operation junction temperature range	-40	140	°C

DYNAMIC ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{D1}	IN+ (or EN) to output propagation delay	V_{DD}=12V, 5V input pulse, C_{LOAD}=1.8nF		18	23	ns
		V_{DD}=4.5V, 5V input pulse, C_{LOAD}=1.8nF		21	28	
t_{D2}	IN- to output propagation delay	V_{DD}=12V, 5V input pulse, C_{LOAD}=1.8nF		18	23	
		V_{DD}=4.5V, 5V input pulse, C_{LOAD}=1.8nF		21	28	
t_R (1)	Turn-on rise time	V_{DD}=12V, C_{LOAD}=1.8nF		7	10	
		V_{DD}=4.5V, C_{LOAD}=1.8nF		6	11	
t_F (1)	Turn-off fall time	V_{DD}=12V, C_{LOAD}=1.8nF		5	8	
		V_{DD}=4.5V, C_{LOAD}=1.8nF		5	12	

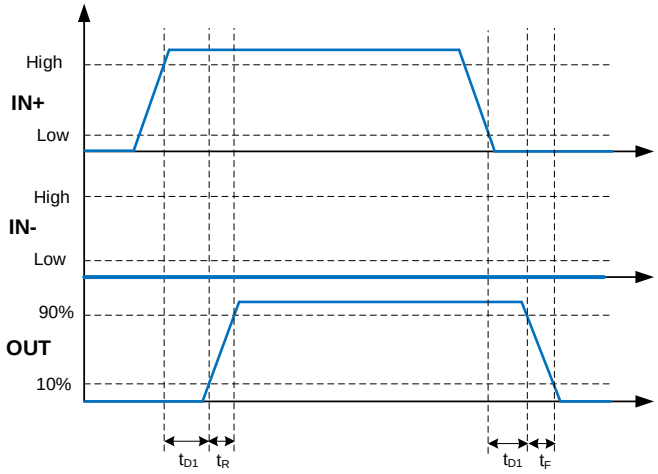
Note1: only bench test

STATIC ELECTRICAL CHARACTERISTICS

V_{DD}= 12 V,10uF capacitor from VDD to GND. T_A = 25°C unless otherwise specified.

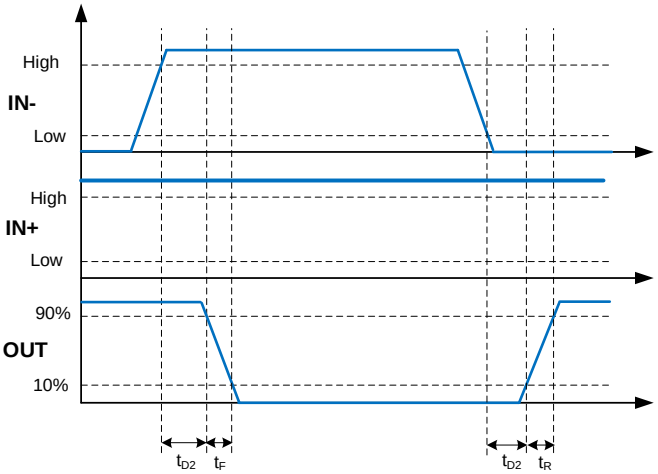
Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage	Output high for IN+ pin Output low for IN- pin			2	2.2	V
V_{IL}	Logic “0” input voltage	Output low for IN+ pin Output high for IN- pin		1.07	1.3		
V_{OH}	High level output voltage, V_{DD} - V_O	V_{DD}=12V I_O = -10 mA			8.7	12	mV
		V_{DD}=4.5V I_O = -10 mA			9.8	14.6	
V_{OL}	Low level output voltage, V_O	V_{DD}=12V I_O = 10 mA			4.8	7.4	
		V_{DD}=4.5V I_O = 10 mA			5.2	9.4	
$I_{DD(off)}$	Startup current	V_{DD} =3.4V	IN+ = V_{DD}, IN- = GND or IN+ = IN- = GND	45	75	120	uA
			IN+ = GND, IN- = V_{DD} or IN+ = IN- = V_{DD}	35	60	110	
V_{DDUV+}	Undervoltage positive going threshold			4.03	4.2	4.45	V
V_{DDUV-}	Undervoltage negative going threshold			3.7	3.9	4.12	
V_{DD_H}	Supply voltage hysteresis				0.3		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_O	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = Logic “1”, PW ⩽ 10 µs		-4		A
	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = Logic “0”, PW ⩽ 10 µs		5		



(PWM input to IN+ pin, IN- pin tied to GND)

Figure 2. Noninverting Configuration



(PWM input to IN- pin, IN+ pin tied to VDD)

Figure 3. Inverting Configuration

FEATURE DESCRIPTION

Overview

The SLM27517 single-channel, high-speed, low-side gate-driver device can effectively drive MOSFET and IGBT power switches. The device can source and sink high peak-current pulses into capacitive loads, offering rail-to-rail drive capability and extremely small propagation delay of 18ns (typical). The SLM27517 device provides 4A source, 5A sink peak drive current capability. The SLM27517 is designed to operate over a wide V_{DD} range of 4.5 to 20 V, and a wide temperature range of -40°C to 140°C.

Internal UVLO circuitry on the VDD pin holds the output low when V_{DD} is outside the operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The SLM27517 device features a dual-input design which offers flexibility of implementing both inverting (IN- pin) and noninverting (IN+ pin) configuration with the same device. Either the IN+ or IN- pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pull up and pull down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore, the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation. The input pin threshold of the device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

VDD and Under-Voltage Lockout

The SLM27517 devices have internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{DDUV+} during power up and when V_{DD} voltage is less than V_{DDUV-} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltage has noise from the power supply and also when there are droops in the VDD bias voltage when the system starts switching and there is a sudden increase in I_{DD}.

For example, at power up, the SLM27517 driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady state V_{DD} is reached. In the noninverting operation (PWM signal applied to IN+ pin), the output remains LOW until the UVLO threshold is reached, and then the output is in phase with the input. In the inverting operation (PWM signal applied to IN- pin), the output remains LOW until the UVLO threshold is reached, and then the output is out phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface- mount components is highly recommended. A 0.1μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1μF or higher value) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors characteristic for the expected current levels and switching frequencies in the application.

Input Stage

The input pins of the SLM27517 series products are based on a TTL/CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typical high threshold 2V and typical low threshold 1.3V, the logic level thresholds can be conveniently driven with PWM-control signals derived from 3.3V and 5V digital-power controllers. These devices also feature tight control of the input pin threshold voltage levels which eases system-design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pull-up resistors on all the inverting inputs (IN- pin) or GND-pull-down resistors on all the noninverting input pins (IN+ pin).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a noninverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins. Once an input pin has been chosen for PWM drive, the other input pin (the unused input pin) must be properly biased in order to enable the

output. As mentioned earlier, the unused input pin cannot remain in a floating condition because, whenever any input pin is left in a floating condition, the output is disabled for safety purposes. Alternatively, the unused input pin can effectively be used to implement an enable and disable function, as explained below.

- To drive the device in a noninverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the unused input pin, IN-, must be biased low (for example tied to GND) in order to enable the output. Alternately, the IN- pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low.

- To drive the device in an inverting configuration, apply the PWM-control input signal to IN- pin. In this case, the unused input pin, IN+, must be biased high (for example tied to VDD) in order to enable the output. Alternately, the IN+ pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.

- Finally, note that the output pin is driven into a high state only when IN+ pin is biased high and IN- input is biased low.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly-varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitic causes ground bounce. Because the device features just one GND pin, which may be referenced to the power ground, the differential voltage between input pins and GND is modified and triggers an unintended change of output state. Because of fast 15ns propagation delay, high-frequency oscillations ultimately occur, which increases power dissipation and poses risk of damage.

- 0.7V input-threshold hysteresis boosts noise immunity compared to most other industry-standard drivers.

- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor(1nF) between input pin and ground very close to the driver device is necessary. This helps to convert the differential mode noise with respect to the input logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring the gate driver into the external resistor.

Output Stage

The SLM27517 device output stage delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). It is capable of supplying 4A peak source and 5A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation.

Power Supply Recommendations

The bias supply voltage ranges for which the SLM27517 series products are rated to operate is from 4.5 V to 20 V. The lower end of this range is governed by the internal UVLO protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{DDUV+} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 25 V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 5 V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 20 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD\_H(hys)}$. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device, to avoid triggering a device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_{DDUV-} threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the V_{DDUV+} threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Keep in mind that the charge for source current pulses delivered by the OUT pin is also supplied through the

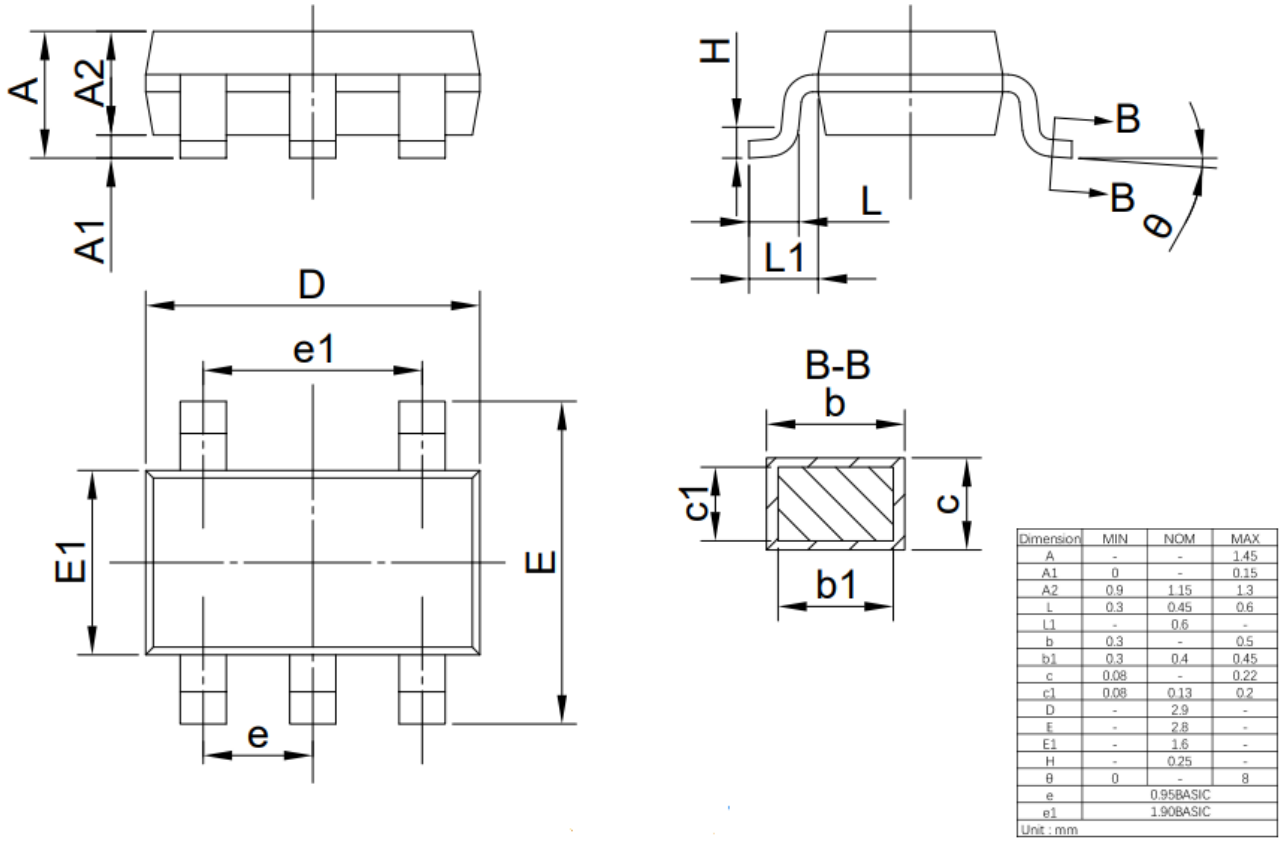
same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V_{DD} and GND pins, and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. SLM27517 recommends using two capacitors: a 100nF ceramic surface-mount capacitor which can be placed very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The SLM27517 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high- current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turning on the power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current-loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances, during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch or the ground of PWM controller at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, connecting the unused input pin of SLM27517 to VDD (in case of IN+) or GND (in case of IN-) using short traces to ensure that the output is enabled and to prevent noise from causing malfunction in the output is necessary.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.45
A1	0	-	0.15
A2	0.9	1.15	1.3
L	0.3	0.45	0.6
L1	-	0.6	-
b	0.3	-	0.5
b1	0.3	0.4	0.45
c	0.08	-	0.22
c1	0.08	0.13	0.2
D	-	2.9	-
E	-	2.8	-
E1	-	1.6	-
H	-	0.25	-
θ	0	-	8
e	0.95BASIC		
e1	1.90BASIC		
Unit : mm			

Figure 4. SOT23-5 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 0.1 Preliminary datasheet, 2021-08-03	
Whole document	Preliminary datasheet released
Rev 0.2 Preliminary datasheet, 2022-05-29	
Page 6	Update the dynamic electrical characteristics and static electrical characteristics
Page 11	Update the package case outlines
Rev 1.0 Datasheet, 2022-07-01	
Whole document	Removed preliminary datasheet watermark.
Rev 1.1 Datasheet, 2022-12-19	
Page 11	Update the SOT23-5 outline dimensions: A, A2, c, c1, D