

600V 3-Phase Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- $I_{\text{O+/-}}$ 200 mA / 350 mA
- V_{OUT} 10 V - 20 V
- $t_{\text{on/off (typ.)}}$ 480 ns / 370 ns
- **Deadtime (typ.)** 290 ns

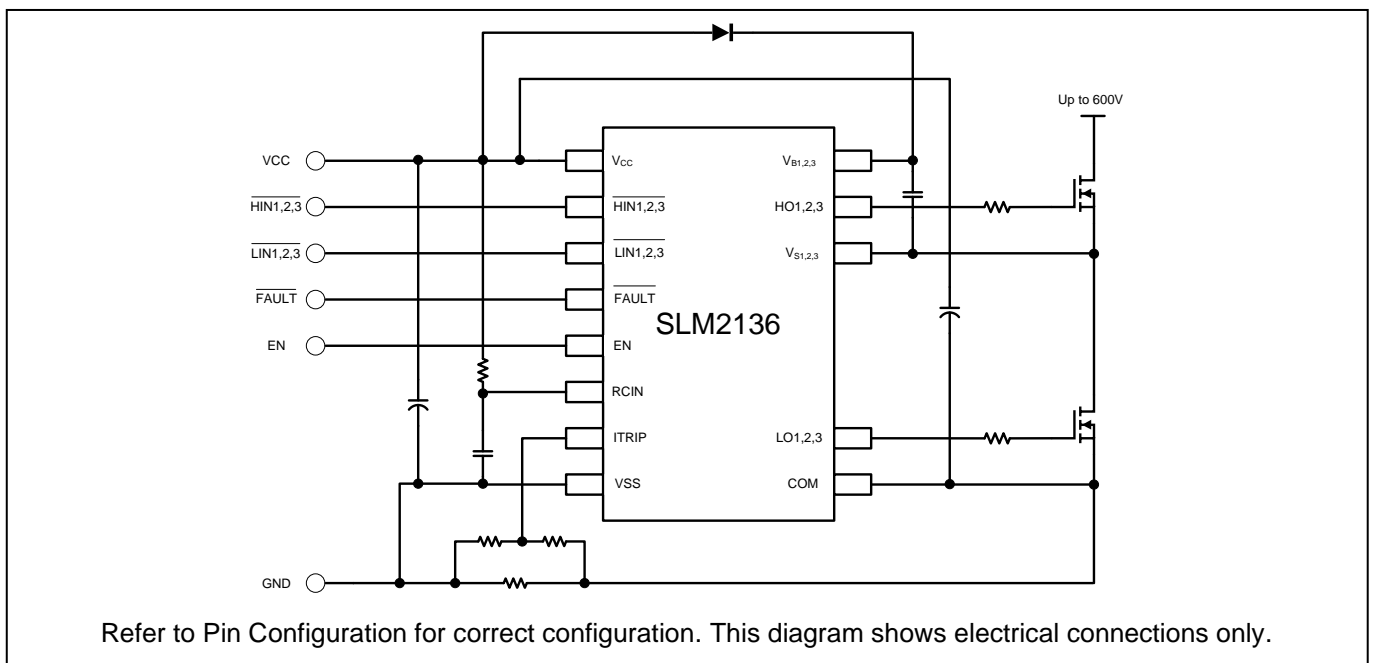
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Low/high side output out of phase with inputs
- 3.3 V, 5 V, and 15 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Externally programmable delay for automatic fault clear
- SOP28W package

GENERAL DESCRIPTION

The SLM2136 is a high voltage, high speed power MOSFET and IGBT drivers for 3-phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

Package	Pin Configuration (Top View)																																																								
SOP28W	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1</td> <td>V_{CC}</td> <td>V_{B1}</td> <td>28</td> </tr> <tr> <td>2</td> <td>HIN1</td> <td>HO1</td> <td>27</td> </tr> <tr> <td>3</td> <td>HIN2</td> <td>V_{S1}</td> <td>26</td> </tr> <tr> <td>4</td> <td>HIN3</td> <td></td> <td>25</td> </tr> <tr> <td>5</td> <td>LIN1</td> <td>V_{B2}</td> <td>24</td> </tr> <tr> <td>6</td> <td>LIN2</td> <td>HO2</td> <td>23</td> </tr> <tr> <td>7</td> <td>LIN3</td> <td>V_{S2}</td> <td>22</td> </tr> <tr> <td>8</td> <td>FAULT</td> <td></td> <td>21</td> </tr> <tr> <td>9</td> <td>ITRIP</td> <td>V_{B3}</td> <td>20</td> </tr> <tr> <td>10</td> <td>EN</td> <td>HO3</td> <td>19</td> </tr> <tr> <td>11</td> <td>RCIN</td> <td>V_{S3}</td> <td>18</td> </tr> <tr> <td>12</td> <td>V_{SS}</td> <td></td> <td>17</td> </tr> <tr> <td>13</td> <td>COM</td> <td>LO1</td> <td>16</td> </tr> <tr> <td>14</td> <td>LO3</td> <td>LO2</td> <td>15</td> </tr> </table>	1	V _{CC}	V _{B1}	28	2	HIN1	HO1	27	3	HIN2	V _{S1}	26	4	HIN3		25	5	LIN1	V _{B2}	24	6	LIN2	HO2	23	7	LIN3	V _{S2}	22	8	FAULT		21	9	ITRIP	V _{B3}	20	10	EN	HO3	19	11	RCIN	V _{S3}	18	12	V _{SS}		17	13	COM	LO1	16	14	LO3	LO2	15
1	V _{CC}	V _{B1}	28																																																						
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PIN DESCRIPTION

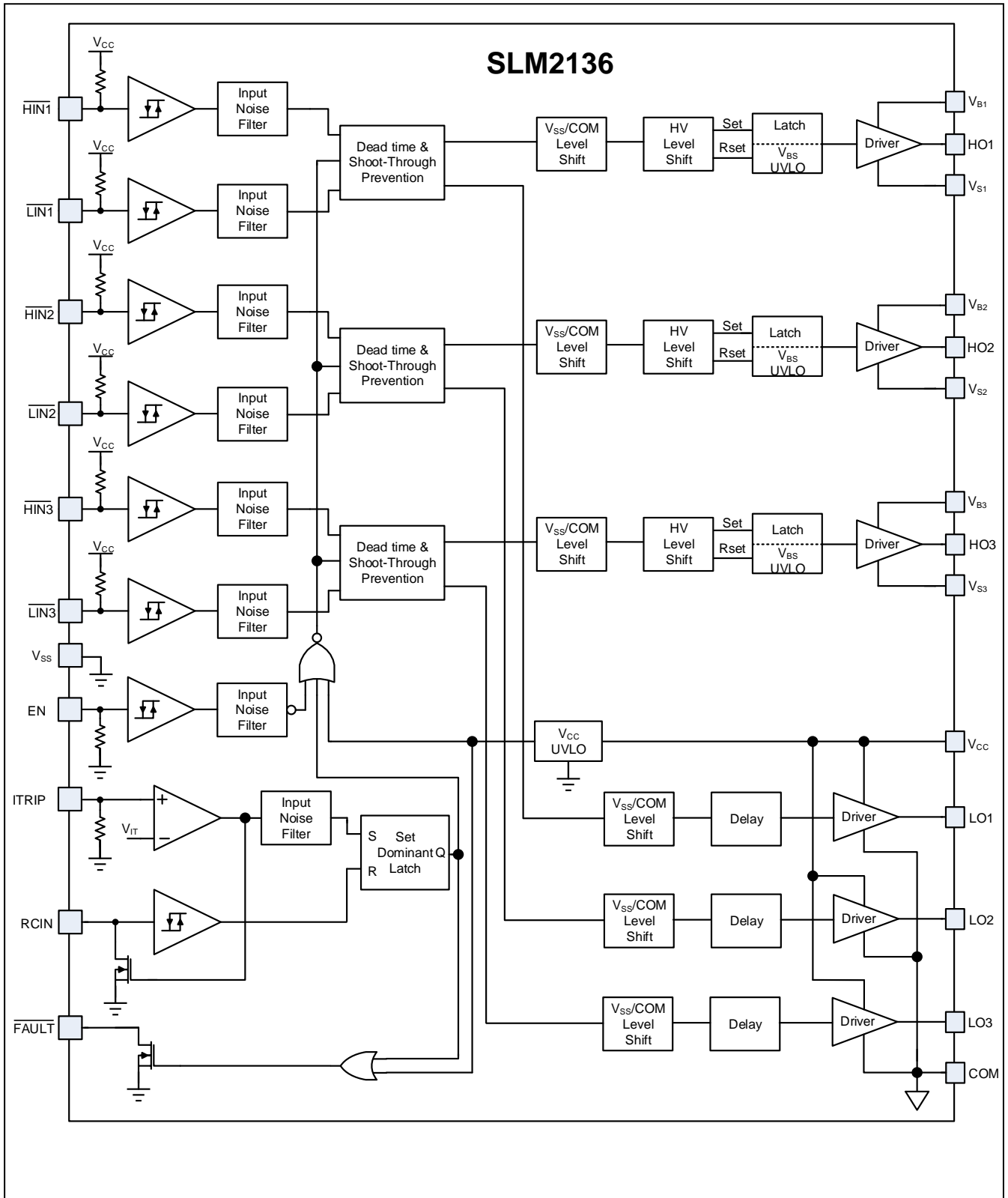
No.	Pin	Description
1	V _{CC}	Low-side and logic fixed supply.
2, 3, 4	HIN1, 2, 3	Logic input for high-side gate driver output (HO), out of phase.
5, 6, 7	LIN1, 2, 3	Logic input for low-side gate driver output (LO), out of phase.
8	FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output.
9	ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T _{FLTCLR} , then automatically becomes inactive (open-drain high impedance).
10	EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. No effect on FAULT and not latched.
11	RCIN	External RC network input used to define FAULT CLEAR delay, T _{FLTCLR} , approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into open-drain high-impedance.
12	V _{SS}	Logic ground.
13	COM	Low-side gate drivers return.
14, 15, 16	LO1, 2, 3	Low-side gate driver outputs.
18, 22, 26	V _{S1, 2, 3}	High-side floating supply return.
19, 23, 27	HO1, 2, 3	High-side gate driver outputs.
20, 24, 28	V _{B1, 2, 3}	High-side floating supply.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2136CF-DG	SOP28W, Pb-Free	1000/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	-0.3	625	V
V _S	High-side floating supply offset voltage	V _{B1,2,3} - 25	V _{B1,2,3} + 0.3	
V _{HO}	High-side floating output voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3	
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V _{SS}	Logic ground	-5	+5	
V _{IN}	Logic input voltage (LIN, HIN, ITRIP, EN, RCIN)	V _{SS} - 0.3	Lower of (V _{SS} + 25) or (V _{CC} + 0.3)	
V _{LO1,2,3}	Low-side output voltage	-0.3	V _{CC} + 0.3	
V _{RCIN}	RCIN input voltage	V _{SS} - 0.3	V _{CC} + 0.3	
V _{FLT}	$\overline{\text{FAULT}}$ output voltage	V _{SS} - 0.3	Lower of (V _{SS} + 25) or (V _{CC} + 0.3)	
dV _S /dt	Allowable offset supply voltage transient	---	50	
P _D	Package power dissipation @ T _A ≤ +25°C	---	1.6	W
θ _{JA}	Thermal resistance, junction to ambient	---	75	°C/W
T _J	Junction temperature	---	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _{B1,2,3}	High-side floating supply voltage	V _{S1,2,3} + 10	V _{S1,2,3} + 20	V
V _{S1,2,3}	High-side floating supply offset voltage		600	
V _{HO1,2,3}	High-side floating output voltage	V _{S1,2,3}	V _{B1,2,3}	
V _{LO1,2,3}	Low-side output voltage	0	V _{CC}	
V _{CC}	Low-side and logic fixed supply voltage	10	20	
V _{SS}	Logic ground	-5	5	
V _{FLT}	$\overline{\text{FAULT}}$ output voltage	V _{SS}	V _{CC}	
V _{RCIN}	RCIN input voltage	V _{SS}	V _{CC}	
V _{ITRIP}	ITRIP input voltage	V _{SS}	V _{SS} + 20V	
V _{IN}	Logic input voltage $\overline{\text{LIN1, 2, 3}}$, $\overline{\text{HIN1, 2, 3}}$	V _{SS}	V _{SS} + 20V	
T _A	Ambient temperature	- 40	125	°C

Note: Logic operational for V_S of (COM - 5V) to (COM + 600V). Logic state held for V_S of (COM-5V) to (COM - V_{BS}).

DYNAMIC ELECTRICAL CHARACTERISTICS
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $V_{S1,2,3} = V_{SS} = \text{COM}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0\text{ V}$	300	480	600	ns
t_{off}	Turn-off propagation delay	$V_S = 600\text{ V}$	250	370	550	
t_r	Turn-on rise time		---	125	190	
t_f	Turn-off fall time		---	50	75	
t_{EN}	Enable low to output shutdown propagation delay	$V_{IN}, V_{EN} = 0\text{ V or }5\text{ V}$	300	450	600	
t_{ITRIP}	ITRIP to output shutdown propagation delay	$V_{ITRIP} = 5\text{ V}$	450	650	850	
t_{bl}	ITRIP blanking time	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 5\text{ V}$	100	150	---	
t_{FLT}	ITRIP to $\overline{\text{FAULT}}$ propagation delay	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 5\text{ V}$	400	630	800	
t_{FILIN}	Input filter time (HIN, LIN)	$V_{IN} = 0\text{ V \& }5\text{ V}$	200	300	---	
t_{FLTCLR}	FAULT clear time RCIN: R = 2 M Ω , C = 1nF	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 0\text{ V}$	1.3	1.8	2	ms
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	$V_{IN} = 0\text{ V \& }5\text{ V}$	200	290	450	ns
MT	Matching delay, HS & LS turn-on/off	External dead time > 400 ns	---	30	90	
PM	Output pulse width matching (pwin - pwout) (Figure 2)		---	40	75	

STATIC ELECTRICAL CHARACTERISTICS
 $V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to V_{SS} and are applicable to all 6 channels ($\overline{\text{LIN1, 2, 3}}$ and $\overline{\text{HIN1, 2, 3}}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "0" input voltage ($\overline{\text{LIN1, 2, 3}}$ and $\overline{\text{HIN1, 2, 3}}$)	$V_{CC} = 10\text{ V to }20\text{ V}$	---	---	2.5	V
V_{IL}	Logic "1" input voltage ($\overline{\text{LIN1, 2, 3}}$ and $\overline{\text{HIN1, 2, 3}}$)		0.8	---	---	
$V_{EN, TH+}$	Enable positive going threshold		---	---	1.7	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{EN, TH-}	Enable negative going threshold		1.0	---	---	V
V _{IT, TH+}	ITRIP positive going threshold		0.39	0.47	0.55	
V _{IT, HYS}	ITRIP input hysteresis		---	0.1	---	
V _{RCIN, TH+}	RCIN positive going threshold		---	8	---	
V _{RCIN, HYS}	RCIN input hysteresis		---	1	---	
V _{OH}	High level output voltage, V _{BIAS} - V _O	I _O = 20 mA	---	0.5	1.0	
V _{OL}	Low level output voltage, V _O		---	0.3	0.6	
V _{CCUV+} V _{BSUV+}	V _{CC} and V _{BS} supply undervoltage positive going threshold		8.0	8.9	9.8	
V _{CCUV-} V _{BSUV-}	V _{CC} and V _{BS} supply undervoltage negative going threshold		7.4	8.2	9.0	
V _{CCUVH} V _{BSUVH}	V _{CC} and V _{BS} supply undervoltage lockout hysteresis		0.3	0.7	---	
V _{IN_CLAMP}	Input clamp voltage (HIN, LIN, ITRIP and EN)	I _{IN} = 100 μA	---	6.8	---	
I _{LK}	Offset supply leakage current	V _{B1,2,3} = V _{S1,2,3} = 600 V	---	---	50	μA
I _{QBS}	Quiescent V _{BS} supply current	V _{IN} = 0 V	---	60	75	
I _{QCC}	Quiescent V _{CC} supply current		---	1.6	2.3	mA
I _{IN+}	Logic “1” input bias current	$\overline{\text{HIN1, 2, 3}} = 0 \text{ V,}$ $\overline{\text{LIN1, 2, 3}} = 0 \text{ V}$	---	250	300	μA
I _{IN-}	Logic “0” input bias current	$\overline{\text{HIN1, 2, 3}} = 5 \text{ V,}$ $\overline{\text{LIN1, 2, 3}} = 5 \text{ V}$	---	150	200	
I _{ITRIP+}	“High” ITRIP input bias current	V _{ITRIP} = 5 V	---	36	100	
I _{ITRIP-}	“Low” ITRIP input bias current	V _{ITRIP} = 0 V	---	0	1	
I _{EN+}	“High” ENABLE input bias current	V _{ENABLE} = 5 V	---	40	100	
I _{EN-}	“Low” ENABLE input bias current	V _{ENABLE} = 0 V	---	0	1	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{RCIN}	RCIN input bias current	$V_{RCIN} = 0\text{ V or }15\text{ V}$	---	0	1	
I_{O+}	Output high short circuit pulsed current	$V_O = 0\text{ V}, V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$	120	200	---	mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15\text{ V}, V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$	250	350	---	
R_{on_RCIN}	RCIN low on resistance		---	25	50	Ω
R_{on_FAULT}	\overline{FAULT} low on resistance		---	120	200	

FUNCTIONAL TABLE

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
< UVCC	X	X	X	0 (note 2)	0	0
15 V	< UVBS	0 V	5 V	High imp	LIN1,2,3	0
15 V	15 V	0 V	5 V	High imp	LIN1,2,3 (note 1)	HIN1,2,3 (note 1)
15 V	15 V	> V_{ITRIP}	5 V	0 (note 3)	0	0
15 V	15 V	0 V	0 V	High imp	0	0

Note:

1. A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
2. U_{VCC} is not latched, when $V_{CC} > U_{VCC}$, FAULT returns to high impedance.
3. When $ITRIP < V_{ITRIP}$, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ $V_{CC} = 15\text{ V}$).

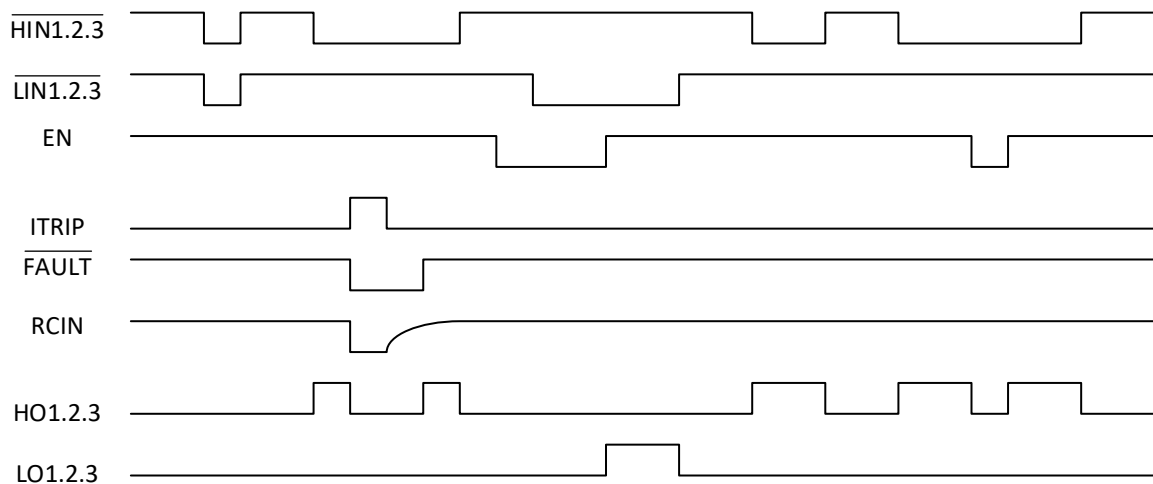


Figure 1. Input/output Timing Diagram

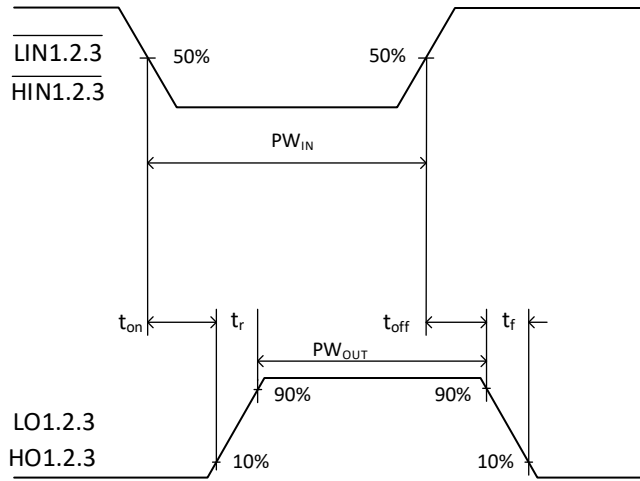


Figure 2. Switching Time Waveforms

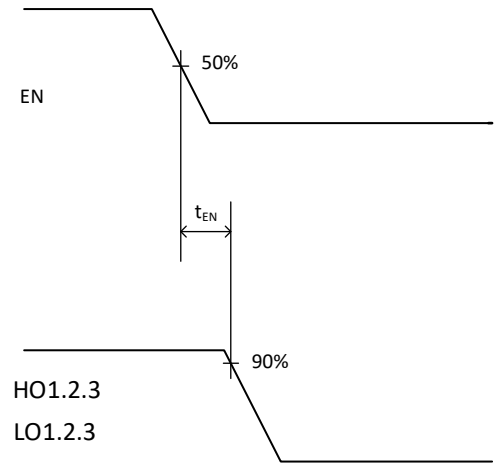


Figure 3. Output Enable Timing Waveform

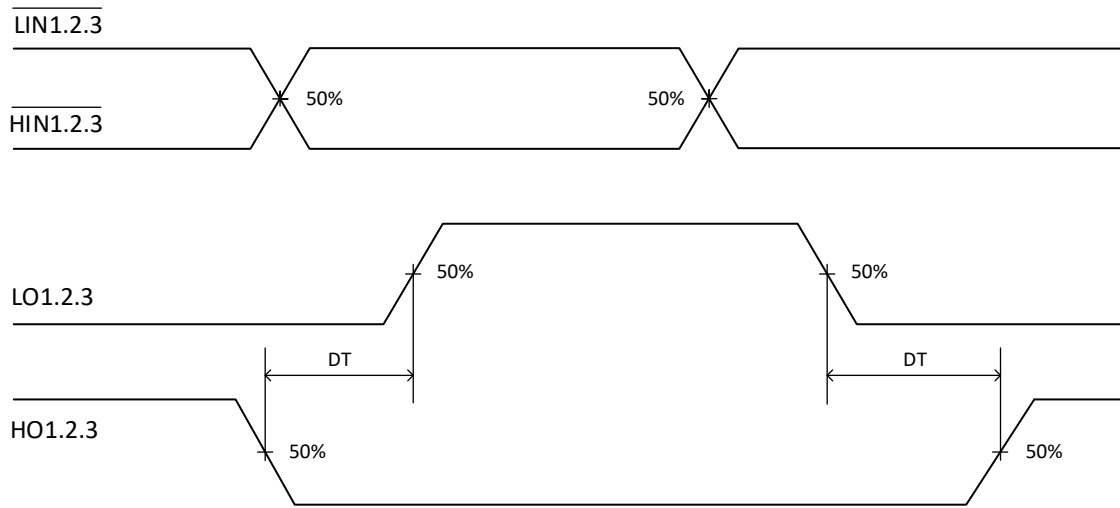


Figure 4. Internal Deadtime Timing Waveforms

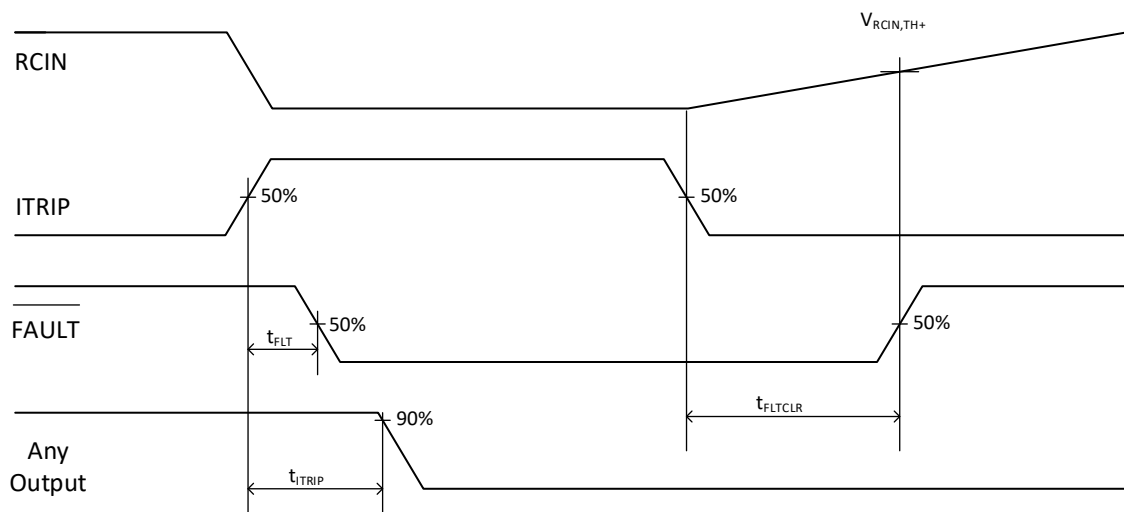


Figure 5. ITRIP/RCIN Timing Waveforms

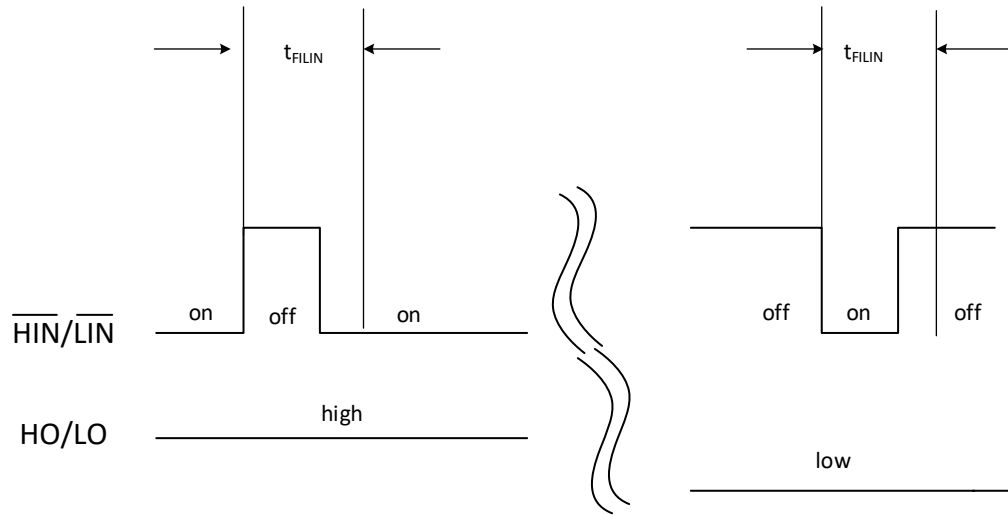
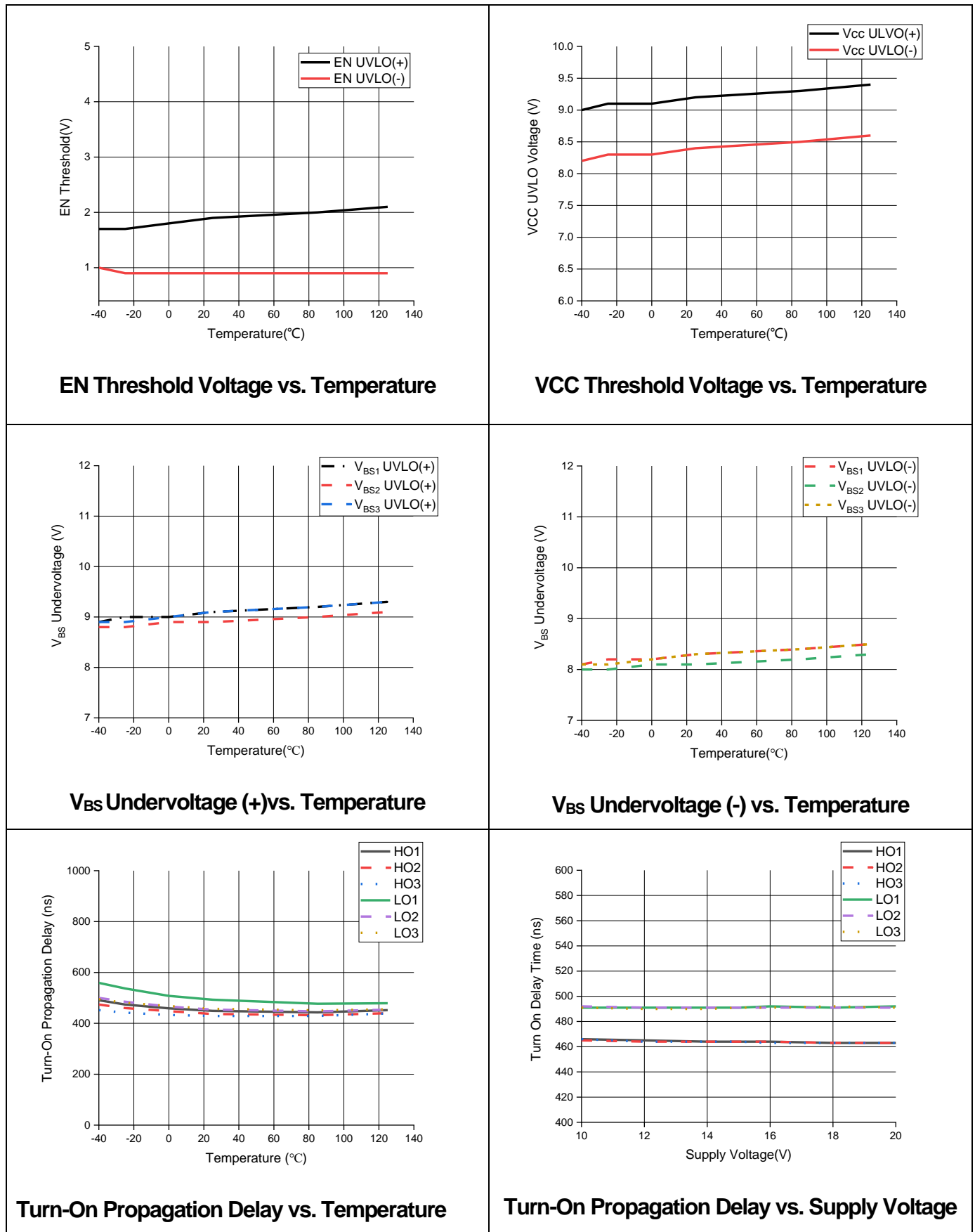
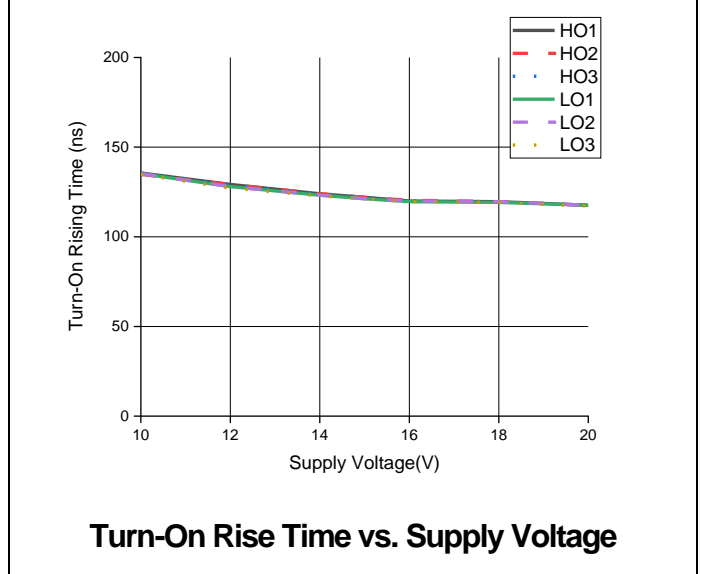
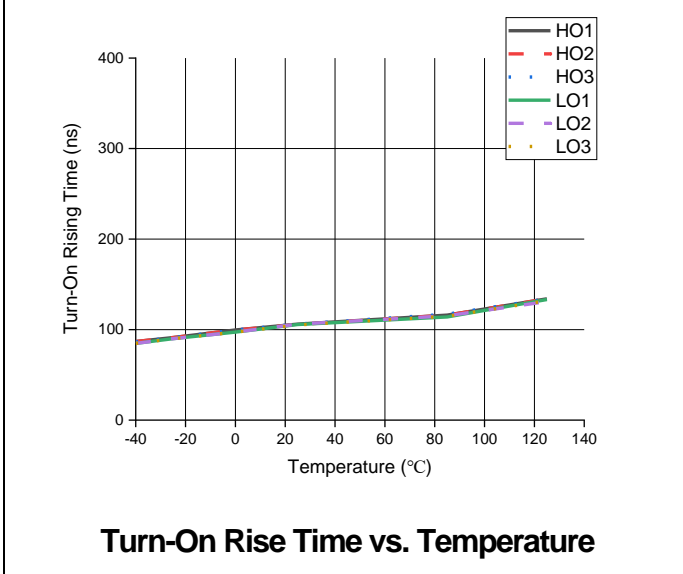
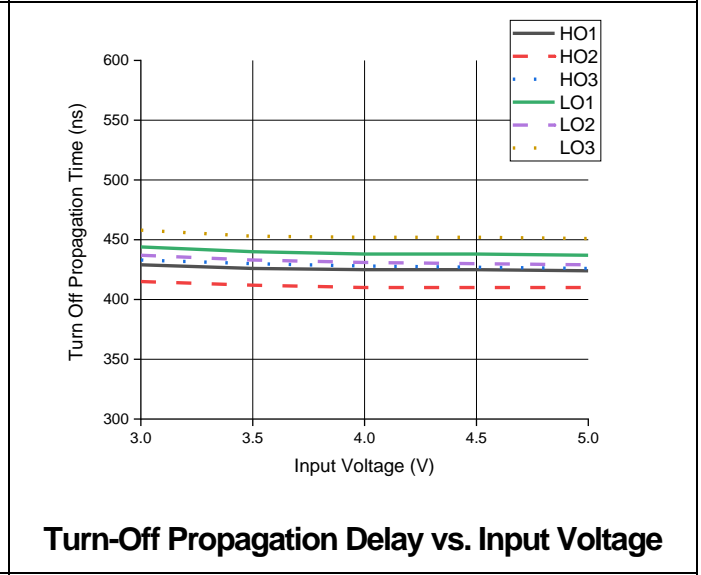
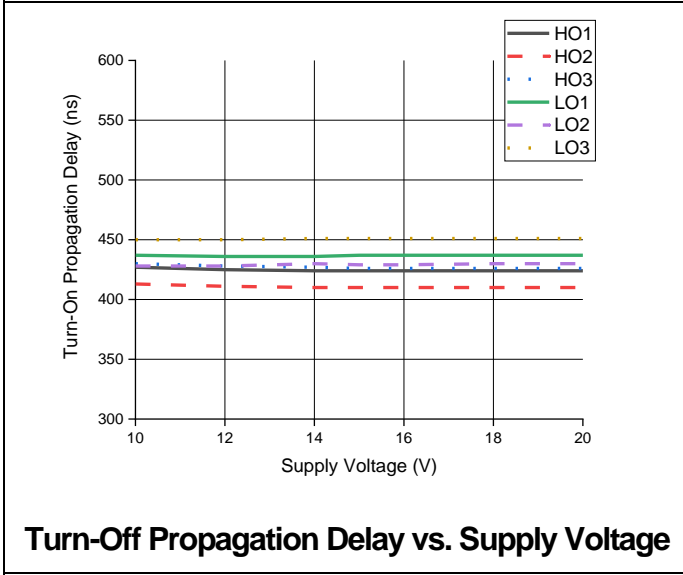
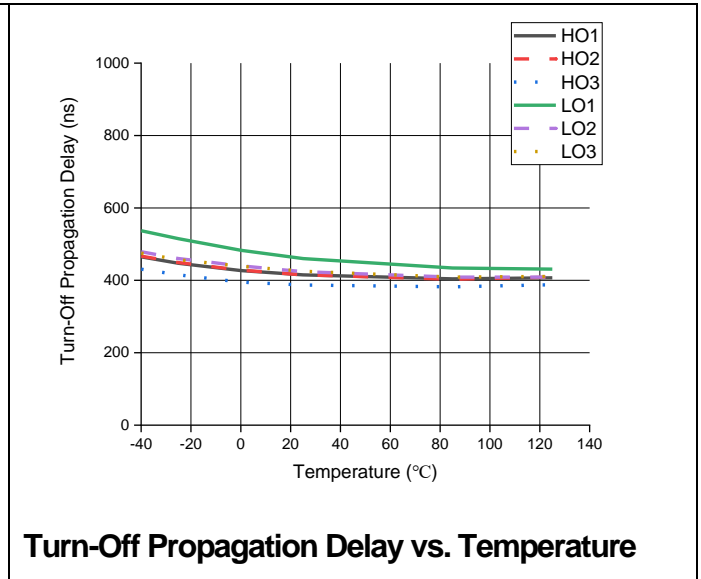
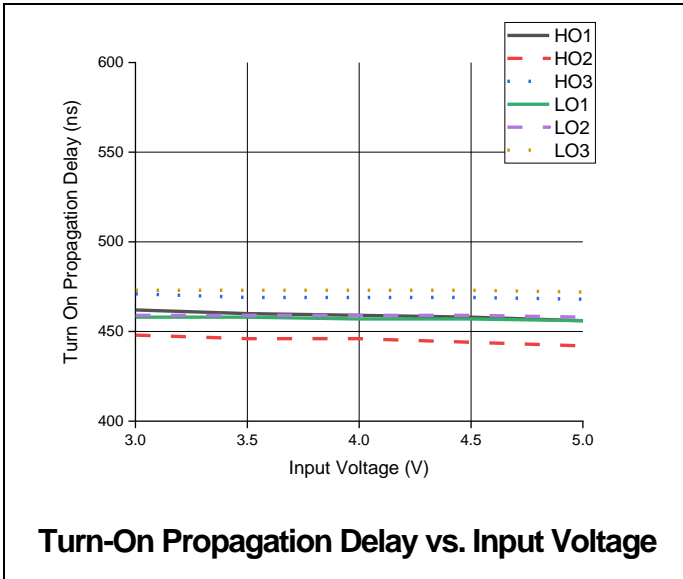
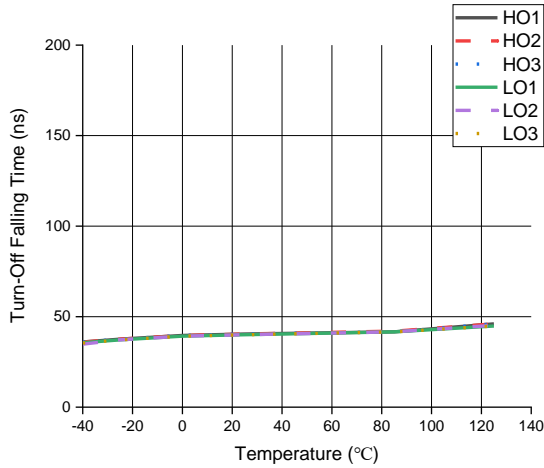


Figure 6. Input Filter Function

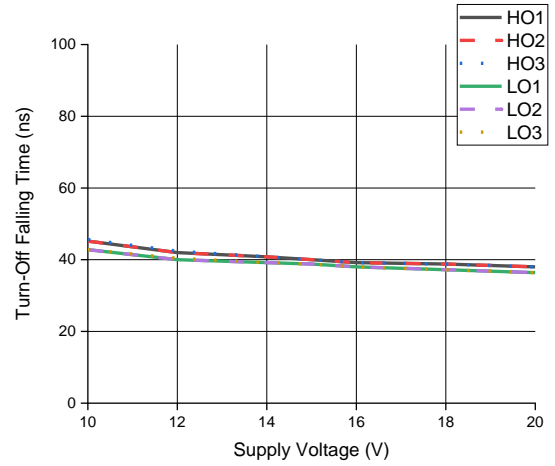
TYPICAL PERFORMANCE CHARACTERISTICS



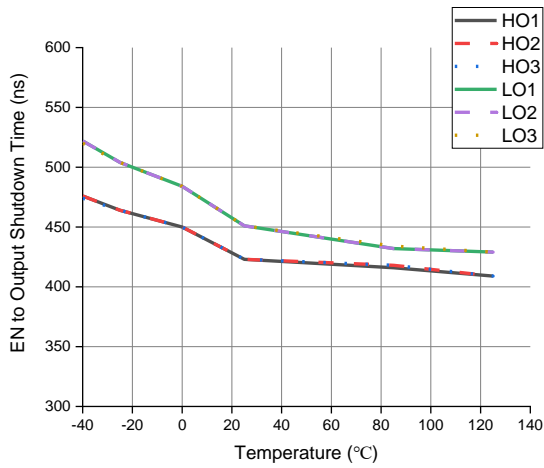




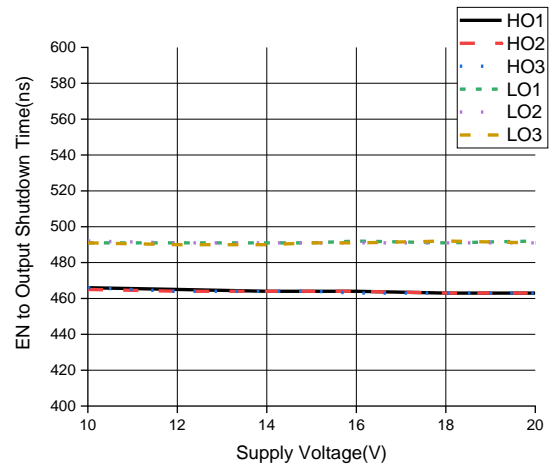
Turn-Off Fall Time vs. Temperature



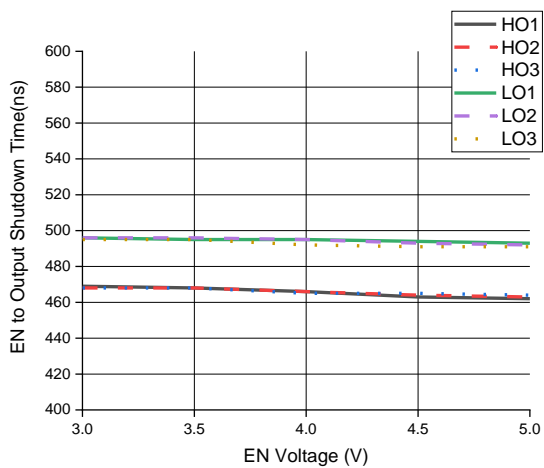
Turn-Off Fall Time vs. Supply Voltage



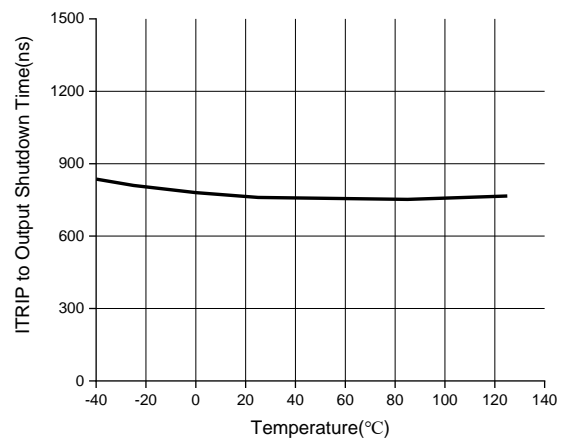
EN to Output Shutdown Time vs. Temperature



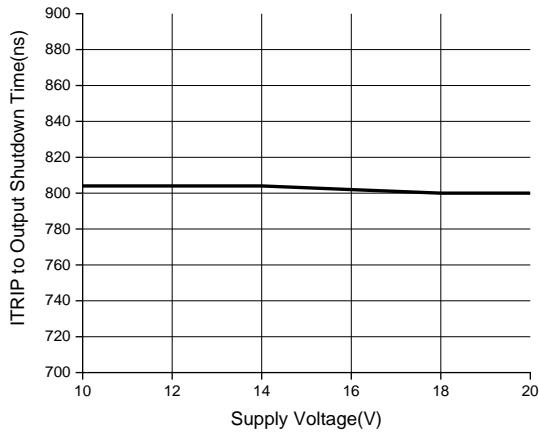
EN to Output Shutdown Time vs. Supply Voltage



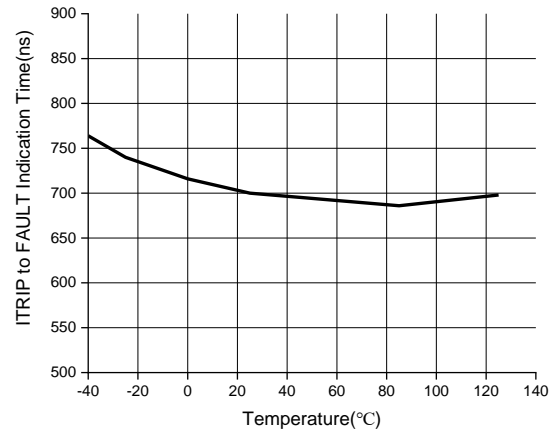
EN To Output Shutdown Time vs. EN Voltage



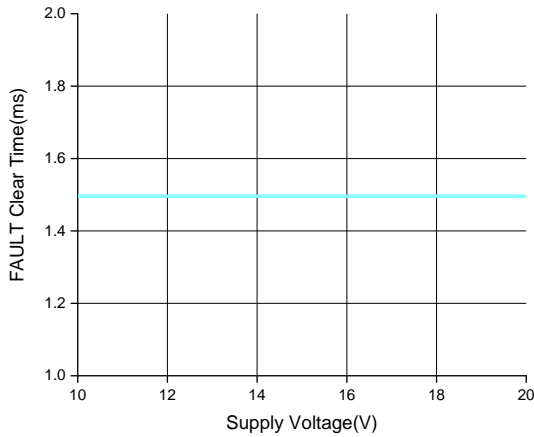
ITRIP To Output Shutdown Time vs. Temperature



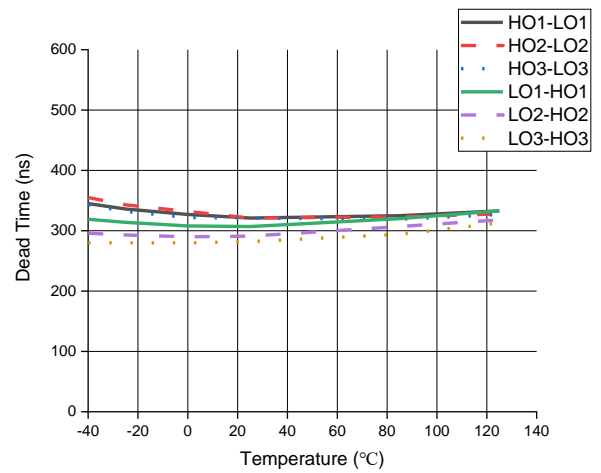
ITRIP To Output Shutdown Time vs. Supply Voltage



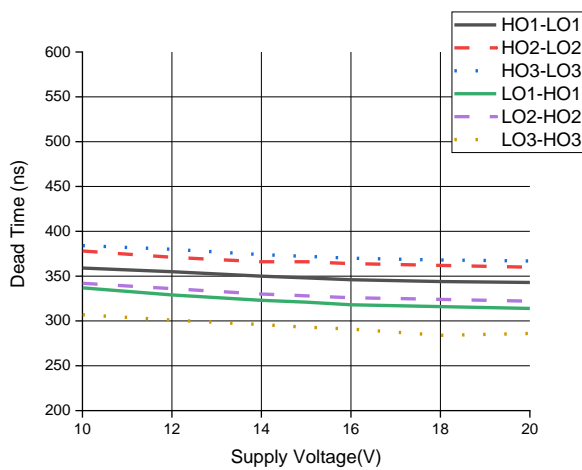
ITRIP To FAULT Indication Time vs. Temperature



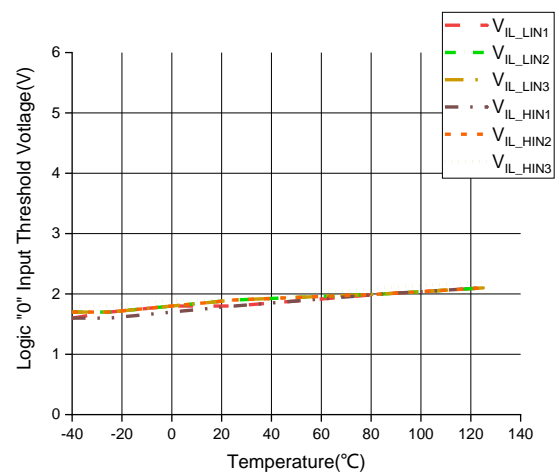
FAULT Clear Time vs. Supply Voltage



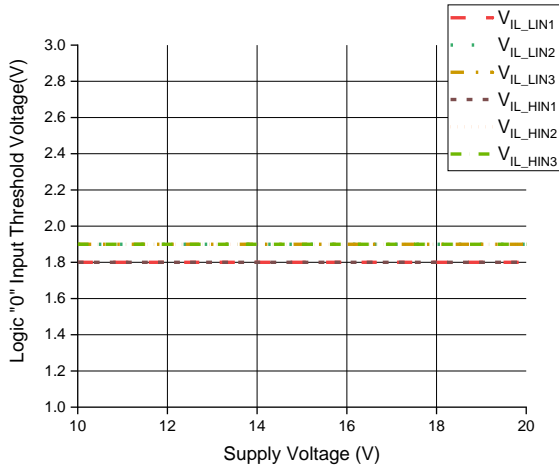
Deadtime vs. Temperature



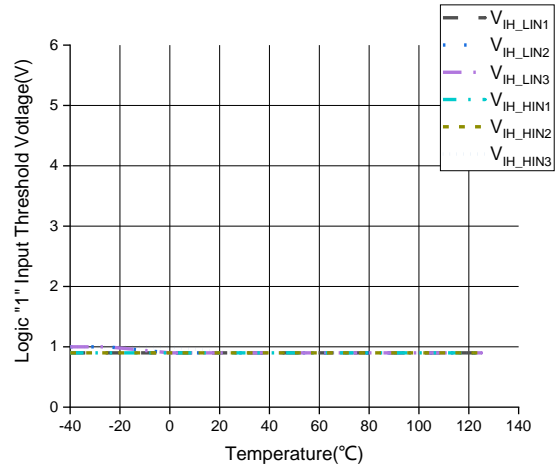
Deadtime vs. Supply voltage



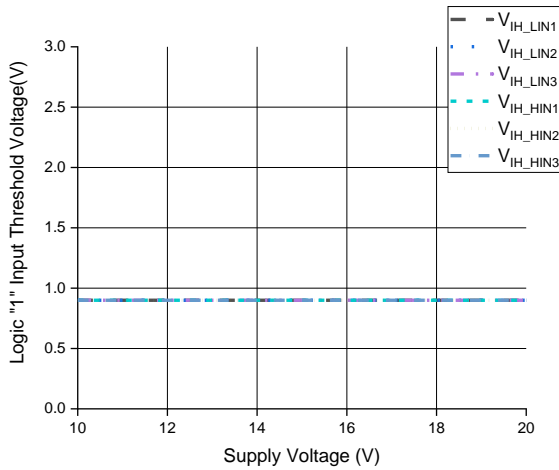
Logic "0" Input Threshold Voltage vs. Temperature



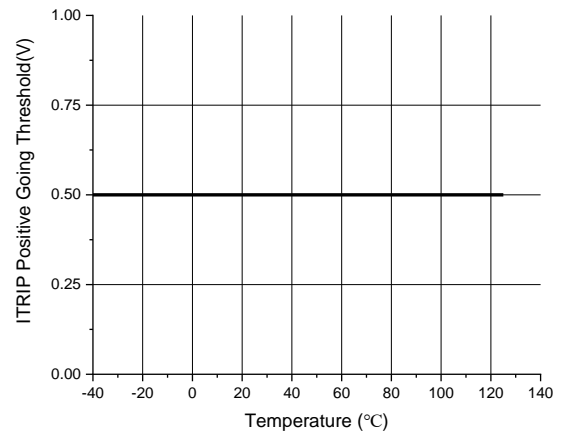
Logic "0" Input Threshold vs. Supply Voltage



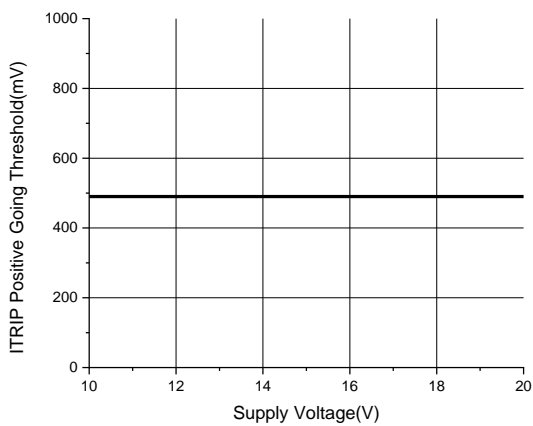
Logic "1" Input Threshold Voltage vs. Temperature



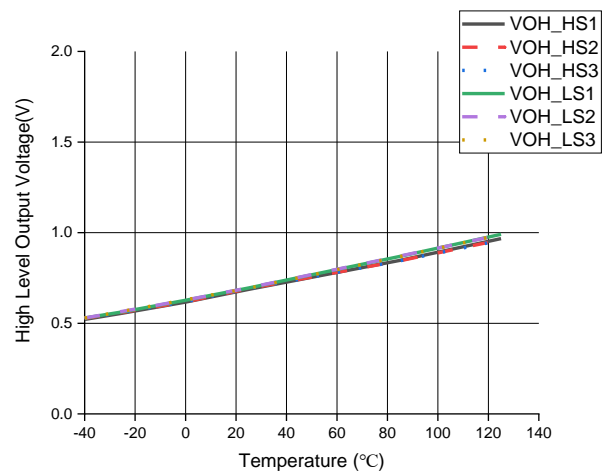
Logic "1" Input Threshold vs. Supply Voltage



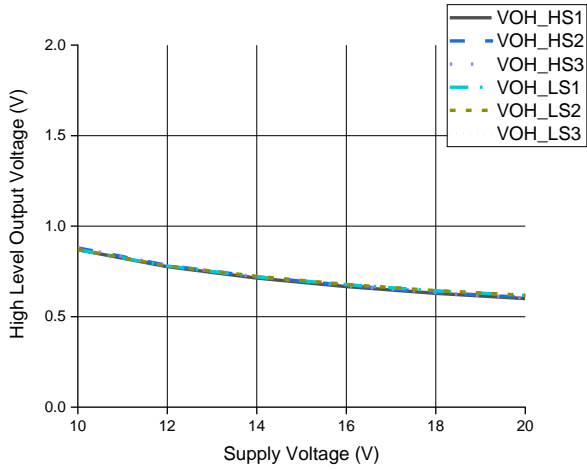
ITRIP Positive Going Threshold vs. Temperature



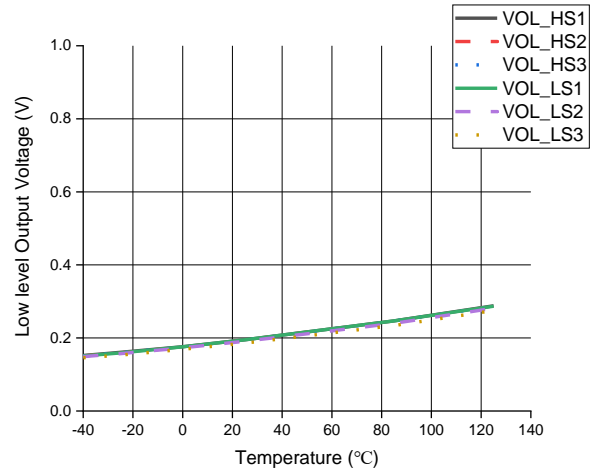
ITRIP Positive Going Threshold vs. Supply Voltage



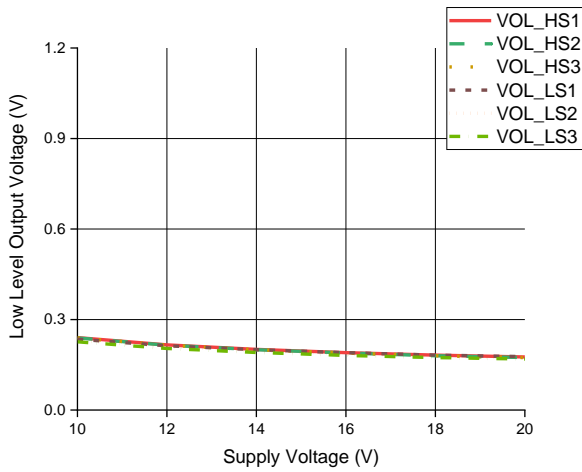
Output High Voltage vs. Temperature



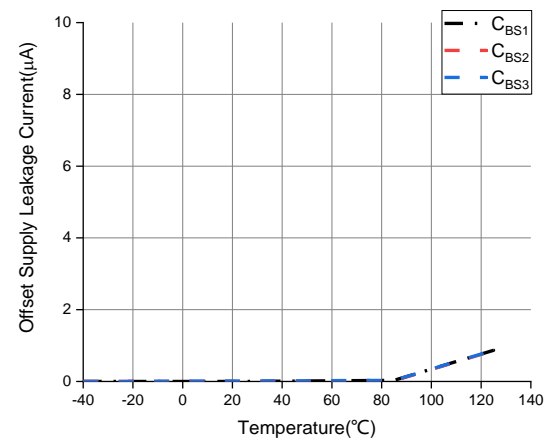
Output High Voltage vs. Supply Voltage



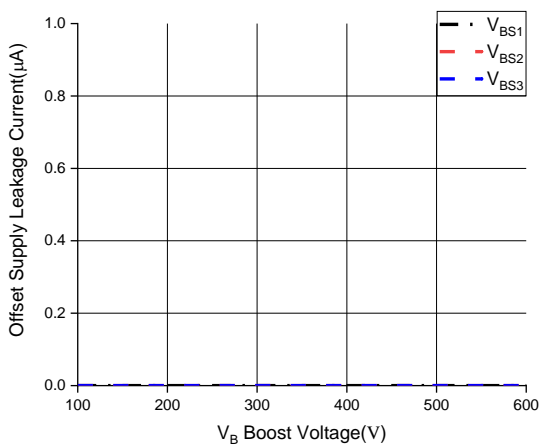
Output Low Voltage vs. Temperature



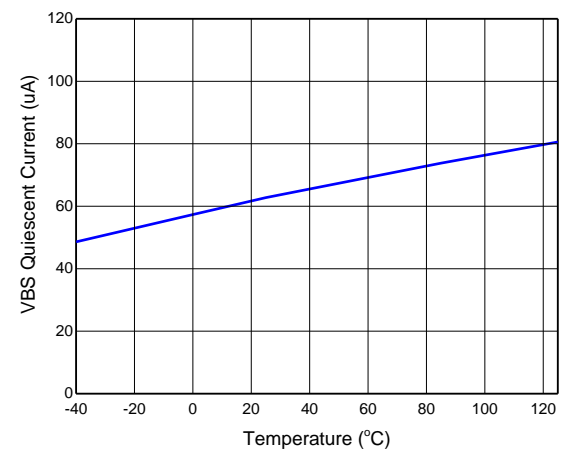
Output Low Voltage vs. Supply Voltage



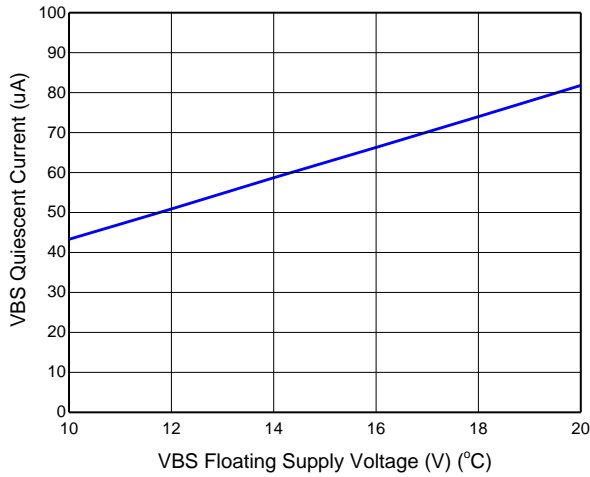
Offset Supply Leakage Current vs. V_B Temperature



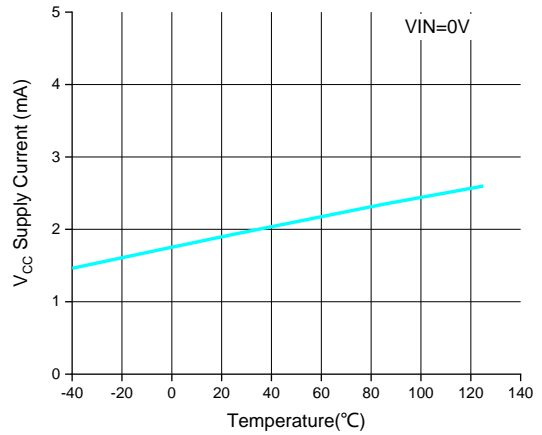
Offset Supply Leakage Current vs. V_B Boost Voltage



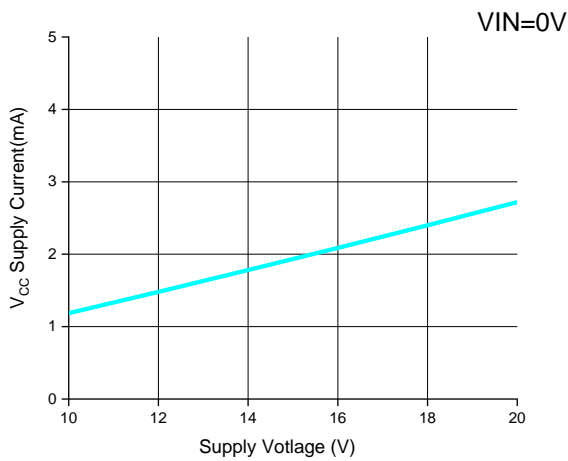
V_{BS} Supply Current vs. Temperature



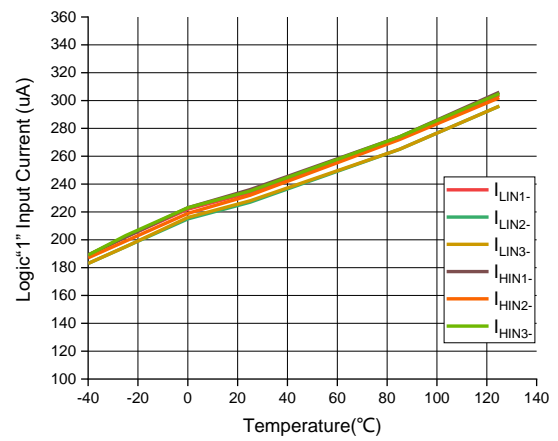
VBS Supply Current vs. Supply Voltage



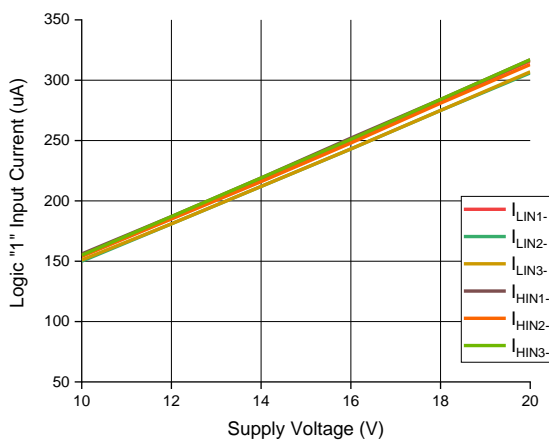
VCC Supply Current vs. Temperature



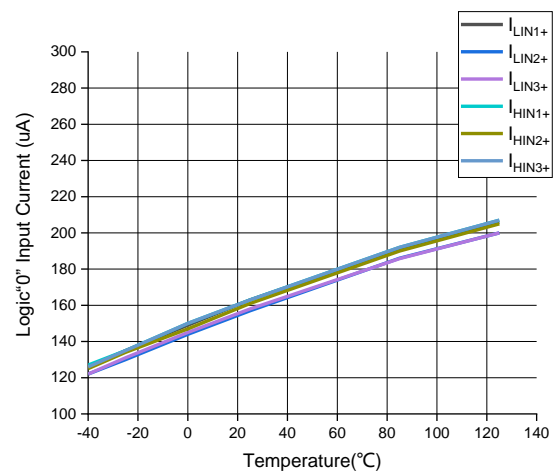
VCC Supply Current vs. Supply Voltage



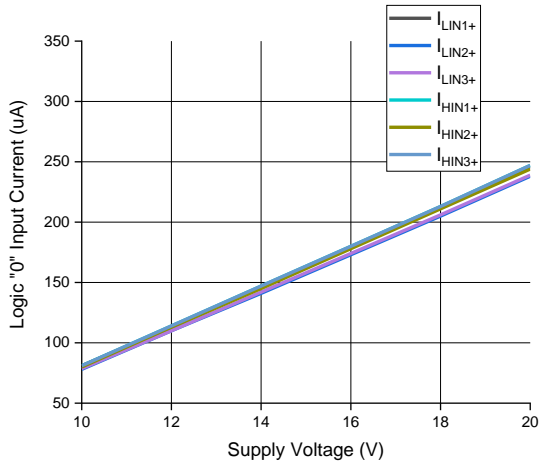
Logic "1" Input Current vs. Temperature



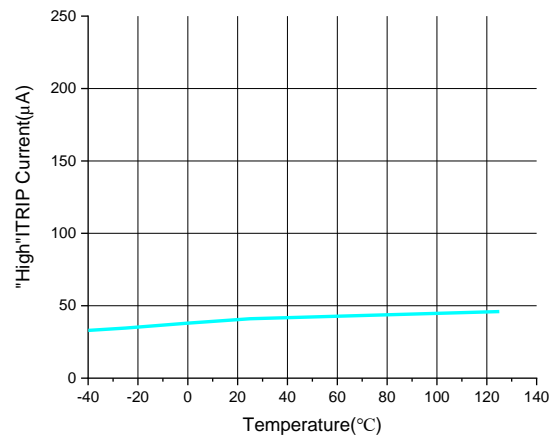
Logic "1" Input Current vs. Supply Voltage



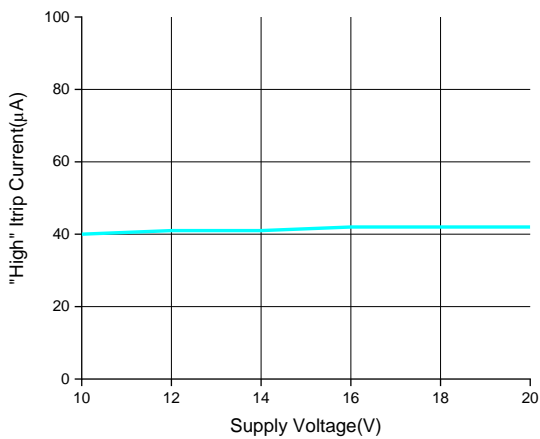
Logic "0" Input Current vs. Temperature



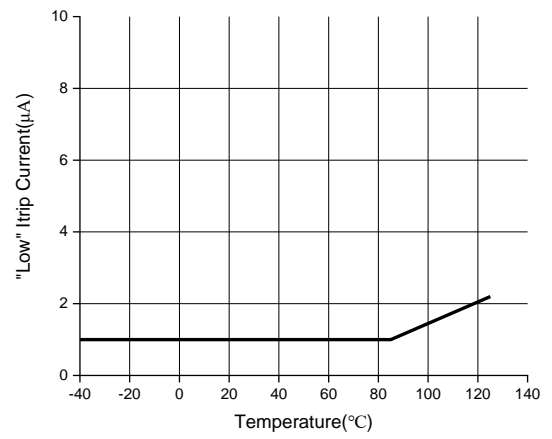
Logic "0" Input Current vs. Supply Voltage



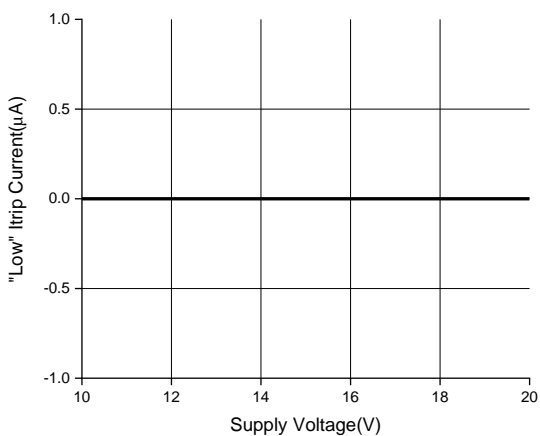
"High" ITRIP Current vs. Temperature



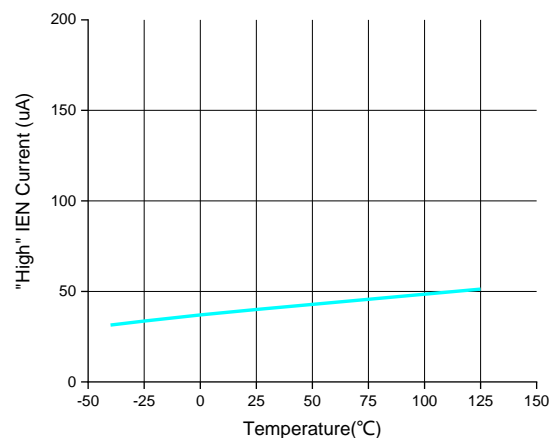
"High" ITRIP Current vs. Supply Voltage



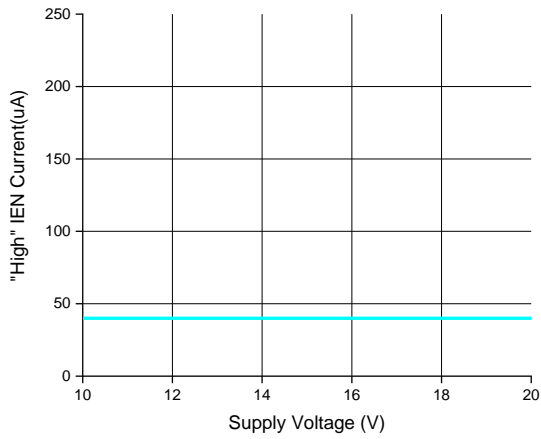
"Low" ITRIP Current vs. Temperature



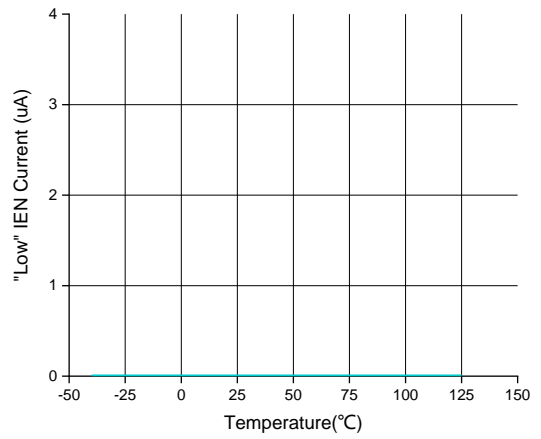
"Low" ITRIP Current vs. Voltage



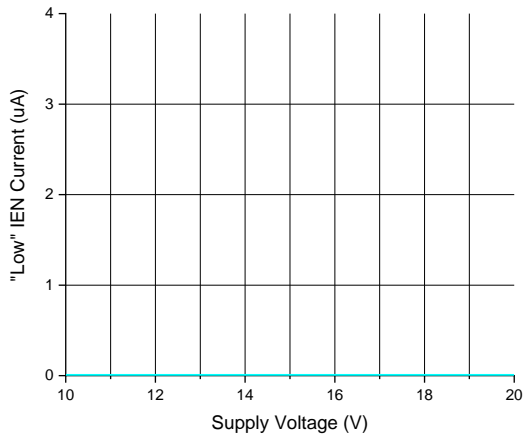
"High" IEN Current vs. Temperature



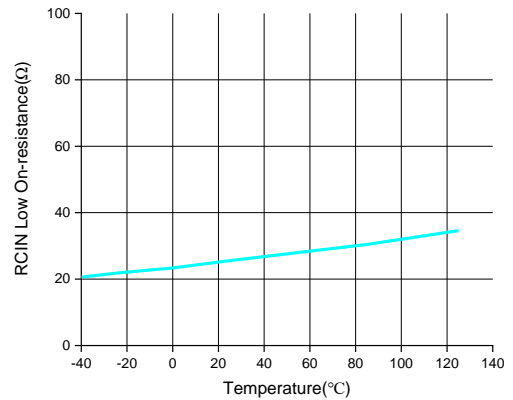
"High" IEN Current Vs Supply Voltage



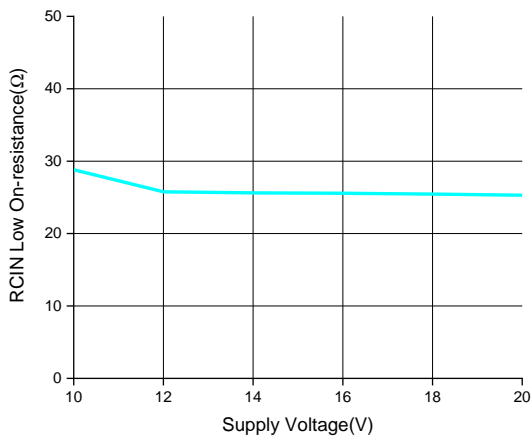
"Low" IEN Current Vs Temperature



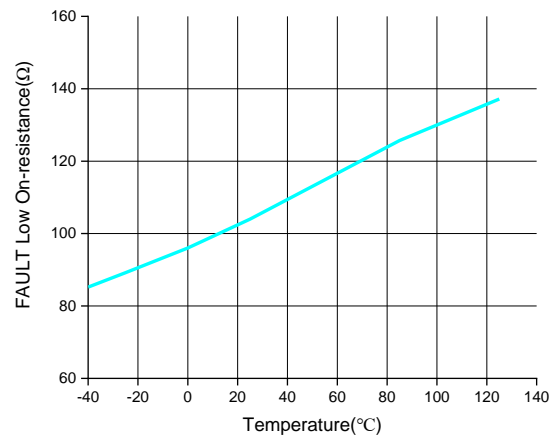
"Low" IEN current vs Supply Voltage



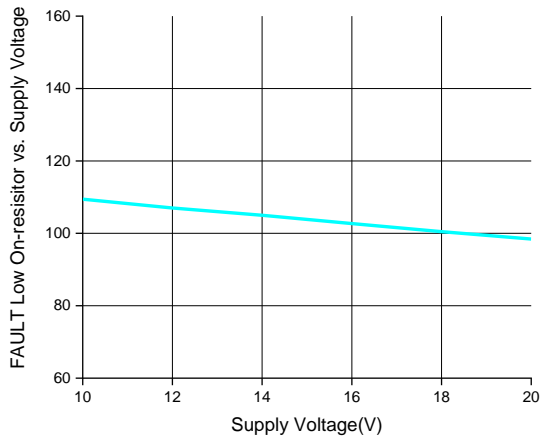
RCIN Low On-resistance vs. Temperature



RCIN Low On-resistance vs. Supply Voltage



FAULT Low On-resistance vs. Temperature



FAULT Low On-resistance vs. Supply Voltage

PACKAGE CASE OUTLINES

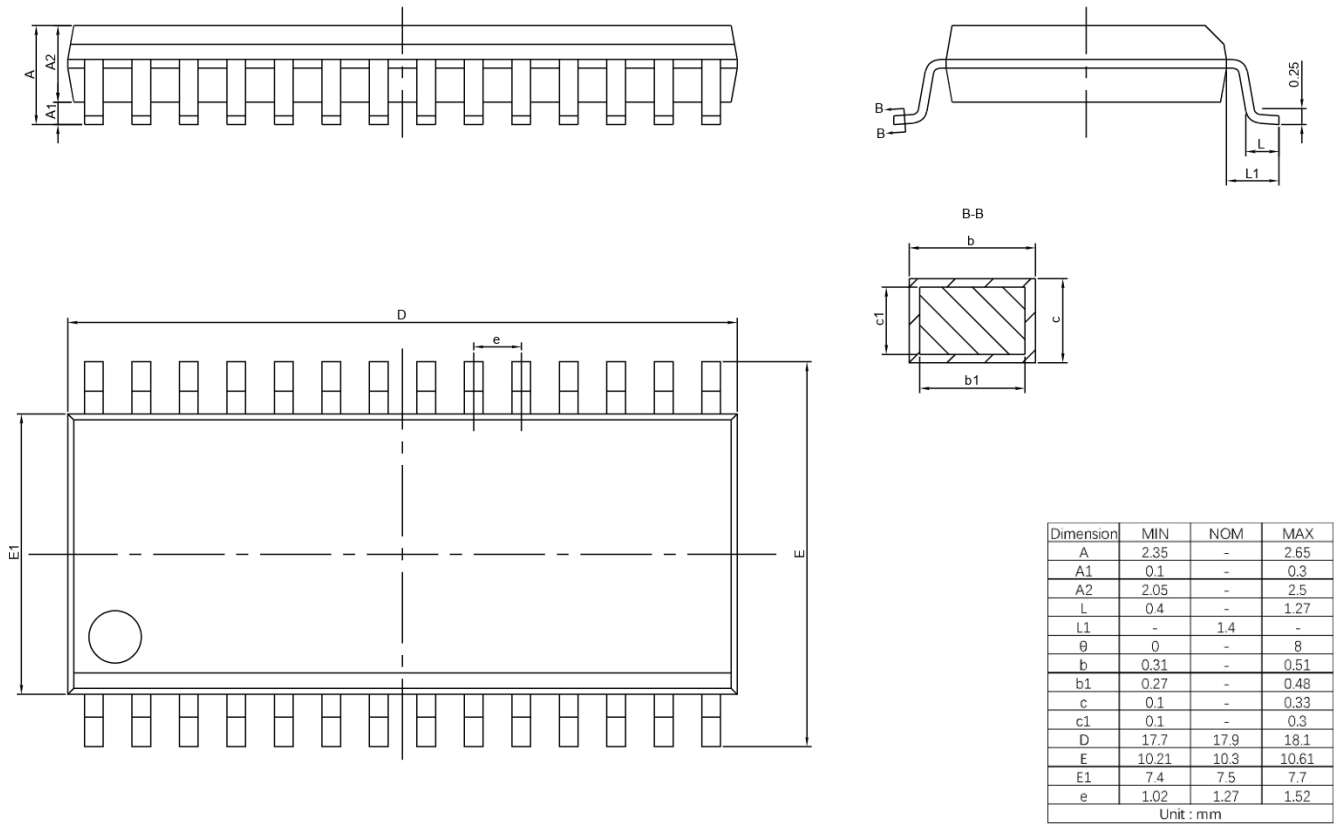


Figure 7. SOP28W Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “Figure1” and “June 2019”
Page 6	Revise $V_{RCIN,HYS}$ parameter
Rev 1.1 datasheet, 2019-11-27	
Page 1	Remove a typo
Page 2	Change order information
Rev 1.2 datasheet, 2020-10-15	
Page 3	Block diagram modified
Page 10-Page 19	Update characteristic chart
Rev 1.3 datasheet, 2022-8-2	
Whole datasheet	Update the logo and format
Page 6, 7,8	Update t_{on} , t_{off} , t_{ITRIP} , t_{FLT} , t_{FILIN} , t_{FLTCLR} , DT, MT in the dynamic electrical characteristics Update V_{IH} , V_{IL} , $V_{IT,TH+}$, V_{IN_CLAMP} , I_{IN+} , I_{IN-} , I_{ITRIP+} , I_{EN+} , R_{on_FAULT} in the static electrical characteristic.
Page 21	Change the package name from SOIC28 to SOP28W